

Octal-Bus Transceiver, Three-State, Non-Inverting

Features

- **Buffered Inputs**
- **Typical Propagation Delay**
- 4ns at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 50pF$
- **Exceeds 2kV ESD Protection per MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
- Fanout to 15 FAST™ ICs
- Drives 50Ω Transmission Lines

Description

The 'AC245 and 'ACT245 are octal-bus transceivers that utilize Advanced CMOS Logic technology. They are non-inverting three-state bidirectional transceiver-buffers intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A". The logic level present on the direction input (DIR) determines the data direction. When the output enable input (\overline{OE}) is HIGH, the outputs are in the high-impedance state.

Ordering Information

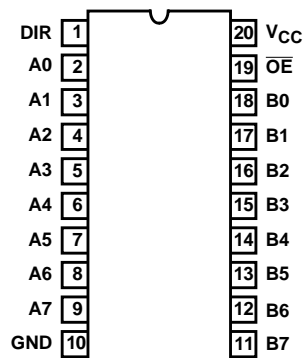
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---------------|------------------|--------------|
| CD54AC245F3A | -55 to 125 | 20 Ld CERDIP |
| CD74AC245E | -55 to 125 | 20 Ld PDIP |
| CD74AC245M | -55 to 125 | 20 Ld SOIC |
| CD74AC245SM | -55 to 125 | 20 Ld SSOP |
| CD54ACT245F3A | -55 to 125 | 20 Ld CERDIP |
| CD74ACT245E | -55 to 125 | 20 Ld PDIP |
| CD74ACT245M | -55 to 125 | 20 Ld SOIC |
| CD74ACT245SM | -55 to 125 | 20 Ld SSOP |

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

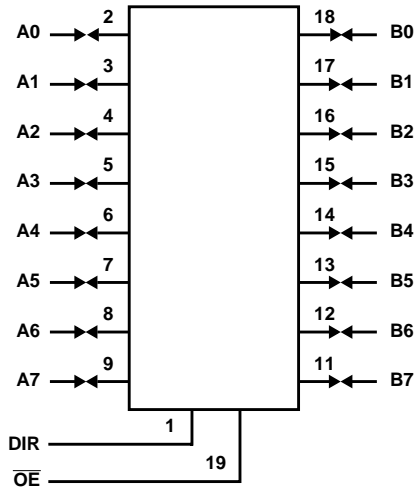
Pinout

CD54AC245, CD54ACT245
(CERDIP)
CD74AC245, CD74ACT245
(PDIP, SOIC, SSOP)
TOP VIEW



CD54/74AC245, CD54/74ACT245

Functional Diagram



TRUTH TABLE

| CONTROL INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B Data to A Bus |
| L | H | A Data to B Bus |
| H | X | Isolation |

H = High Level, L = Low Level, X = Irrelevant

To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

CD54/74AC245, CD54/74ACT245

Absolute Maximum Ratings

| | |
|---|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 6V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 50mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 50mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3) | $\pm 100mA$ |

Thermal Information

| | |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 5) | θ_{JA} ($^{\circ}C/W$) |
| E Package | 69 |
| M Package | 58 |
| SM Package | 70 |
| Maximum Junction Temperature (Plastic Package) | $150^{\circ}C$ |
| Maximum Storage Temperature Range | $-65^{\circ}C$ to $150^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | $300^{\circ}C$ |

Operating Conditions

| | |
|---|----------------------------------|
| Temperature Range, T_A | $-55^{\circ}C$ to $125^{\circ}C$ |
| Supply Voltage Range, V_{CC} (Note 4) | |
| AC Types | 1.5V to 5.5V |
| ACT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I , V_O | 0V to V_{CC} |
| Input Rise and Fall Slew Rate, dt/dv | |
| AC Types, 1.5V to 3V | 50ns (Max) |
| AC Types, 3.6V to 5.5V | 20ns (Max) |
| ACT Types, 4.5V to 5.5V | 10ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS |
|---------------------------|----------|----------------------|--------------------|--------------|----------------|------|-----------------------------------|------|------------------------------------|------|-------|
| | | V_I (V) | I_O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| AC TYPES | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 1.5 | 1.2 | - | 1.2 | - | 1.2 | - | V |
| | | | | 3 | 2.1 | - | 2.1 | - | 2.1 | - | V |
| | | | | 5.5 | 3.85 | - | 3.85 | - | 3.85 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 1.5 | - | 0.3 | - | 0.3 | - | 0.3 | V |
| | | | | 3 | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | | | 5.5 | - | 1.65 | - | 1.65 | - | 1.65 | V |
| High Level Output Voltage | V_{OH} | V_{IH} or V_{IL} | -0.05 | 1.5 | 1.4 | - | 1.4 | - | 1.4 | - | V |
| | | | -0.05 | 3 | 2.9 | - | 2.9 | - | 2.9 | - | V |
| | | | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -4 | 3 | 2.58 | - | 2.48 | - | 2.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |

CD54/74AC245, CD54/74ACT245

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|------------------|---|---------------------|---------------------|------|------|---------------|------|----------------|------|-------|
| | | V _I (V) | I _O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 1.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 3 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 12 | 3 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| ACT TYPES | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | V _{OH} | V _{IH} or V _{IL} | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State or Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load | ΔI _{CC} | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 2.4 | - | 2.8 | - | 3 | mA |

NOTES:

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

CD54/74AC245, CD54/74ACT245

ACT Input Load Table

| INPUT | UNIT LOAD |
|-----------------|-----------|
| An, Bn | 0.83 |
| \overline{OE} | 0.64 |
| DIR | 0.25 |

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input $t_r, t_f = 3ns, C_L = 50pF$ (Worst Case)

| PARAMETER | SYMBOL | V_{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|---|---------------------------|--------------|---------------|-----------|------|----------------|-----------|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| AC TYPES | | | | | | | | | |
| Propagation Delay, Data to Output | t_{PLH}, t_{PHL} | 1.5 | - | - | 96 | - | - | 106 | ns |
| | | 3.3 (Note 9) | 3.2 | - | 10.8 | 3 | - | 11.9 | ns |
| | | 5 (Note 10) | 2.2 | - | 7.7 | 2.1 | - | 8.5 | ns |
| Propagation Delay, Output Disable to Output | t_{PLZ}, t_{PHZ} | 1.5 | - | - | 159 | - | - | 175 | ns |
| | | 3.3 | 4.7 | - | 15.9 | 4.4 | - | 17.5 | ns |
| | | 5 | 3.7 | - | 12.7 | 3.5 | - | 14 | ns |
| Propagation Delay, Output Enable to Output | t_{PZL}, t_{PZH} | 1.5 | - | - | 159 | - | - | 175 | ns |
| | | 3.3 | 5.6 | - | 19 | 5.3 | - | 21 | ns |
| | | 5 | 3.7 | - | 12.7 | 3.5 | - | 14 | ns |
| Minimum (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OHV} See Figure 1 | 5 | - | 4 at 25°C | - | - | 4 at 25°C | - | V |
| Maximum (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OLP} See Figure 1 | 5 | - | 1 at 25°C | - | - | 1 at 25°C | - | V |
| Three-State Output Capacitance | C_O | - | - | 15 | - | - | 15 | - | pF |
| Input Capacitance | C_I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C_{PD} (Note 11) | - | - | 57 | - | - | 57 | - | pF |
| ACT TYPES | | | | | | | | | |
| Propagation Delay, Data to Output | t_{PLH}, t_{PHL} | 5 (Note 10) | 2.7 | - | 9.1 | 2.5 | - | 10 | ns |
| Propagation Delay, Output Disable to Output | t_{PLZ}, t_{PHZ} | 5 | 3.7 | - | 12.7 | 3.5 | - | 14 | ns |
| Propagation Delay, Output Enable to Output | t_{PZL}, t_{PZH} | 5 | 3.8 | - | 13.1 | 3.6 | - | 14.4 | ns |
| Minimum (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OHV} See Figure 1 | 5 | - | 4 at 25°C | - | - | 4 at 25°C | - | V |
| Maximum (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OLP} See Figure 1 | 5 | - | 1 at 25°C | - | - | 1 at 25°C | - | V |

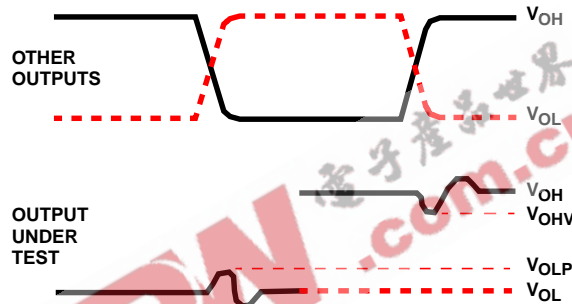
CD54/74AC245, CD54/74ACT245

Switching Specifications Input $t_r, t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case) (Continued)

| PARAMETER | SYMBOL | V_{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|--------------------------------|-----------------------|--------------|---------------|-----|-----|----------------|-----|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Three-State Output Capacitance | C_O | - | - | 15 | - | - | 15 | - | pF |
| Input Capacitance | C_I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C_{PD} (Note 11) | - | - | 57 | - | - | 57 | - | pF |

NOTES:

8. Limits tested 100%
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per channel.
 AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
 ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

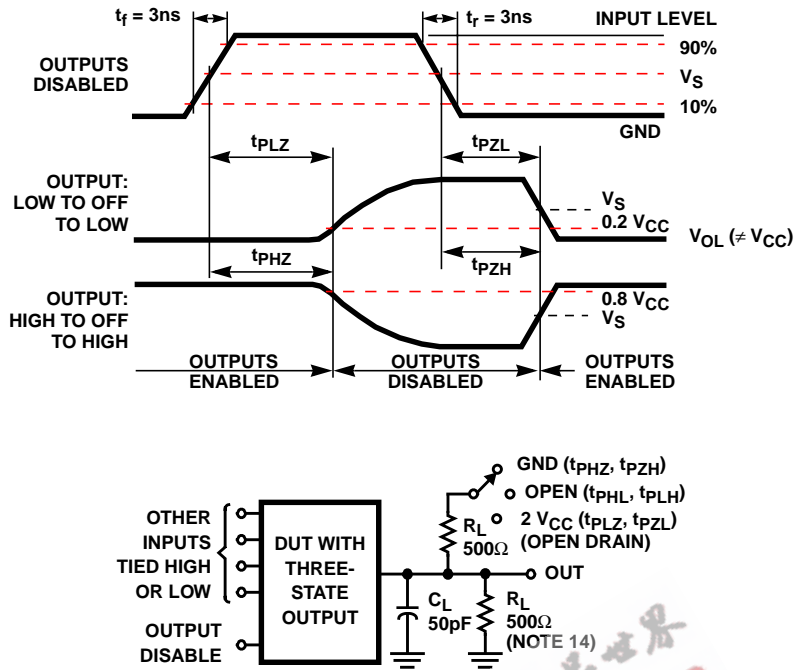


NOTES:

12. Input pulses have the following characteristics: $PRR \leq 1\text{MHz}$, $t_r = 3\text{ns}$, SKEW 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with $0.1\mu\text{F}$ capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 1. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

CD54/74AC245, CD54/74ACT245



NOTE:

14. For AC Series only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

FIGURE 2. THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT

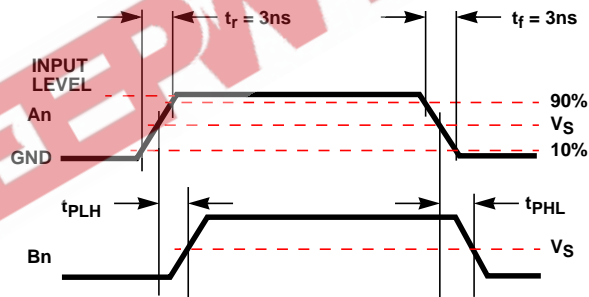
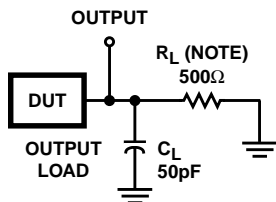


FIGURE 3. PROPAGATION DELAY TIMES



NOTE: For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

| | AC | ACT |
|---------------------------------|--------------|--------------|
| Input Level | V_{CC} | 3V |
| Input Switching Voltage, V_S | $0.5 V_{CC}$ | 1.5V |
| Output Switching Voltage, V_S | $0.5 V_{CC}$ | $0.5 V_{CC}$ |

FIGURE 4. PROPAGATION DELAY TIMES

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD54AC245F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD54ACT245F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD74AC245E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC245EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC245M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC245M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC245M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC245ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC245SM | OBSOLETE | SSOP | DB | 20 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC245SM96 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC245SM96E4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT245E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT245EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT245M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT245M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT245M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT245ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT245SM | OBSOLETE | SSOP | DB | 20 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT245SM96 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT245SM96E4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



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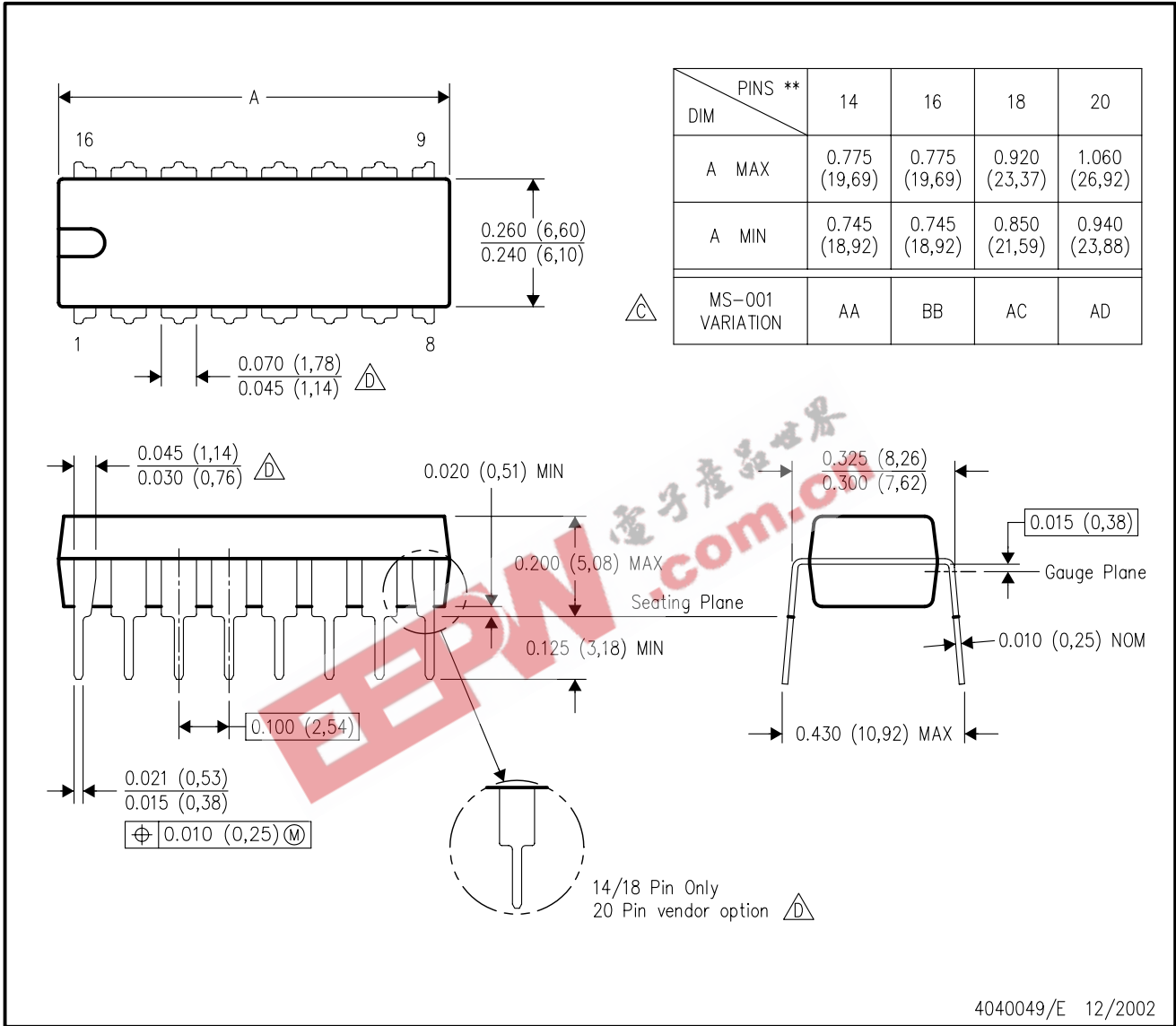
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

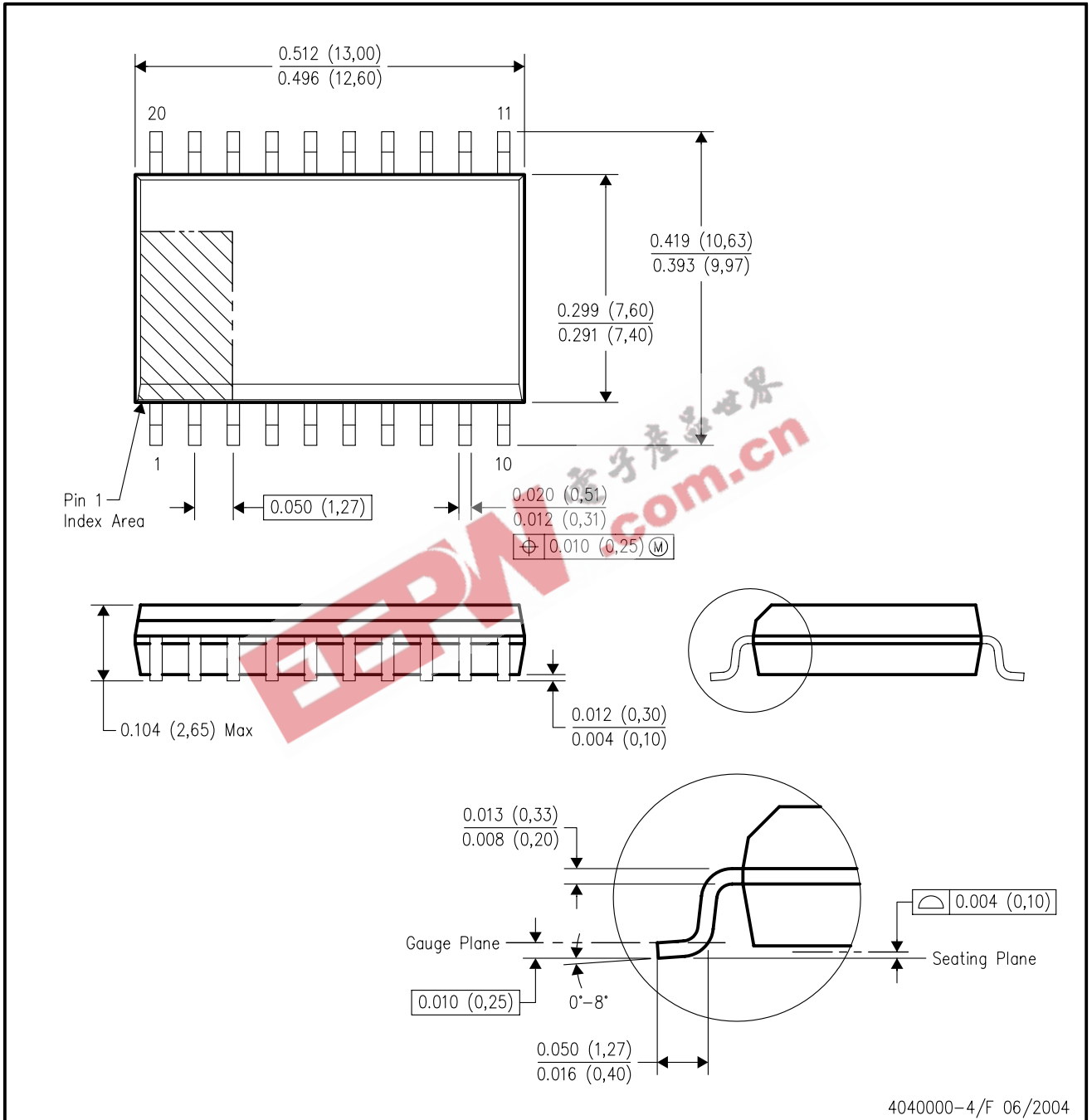


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

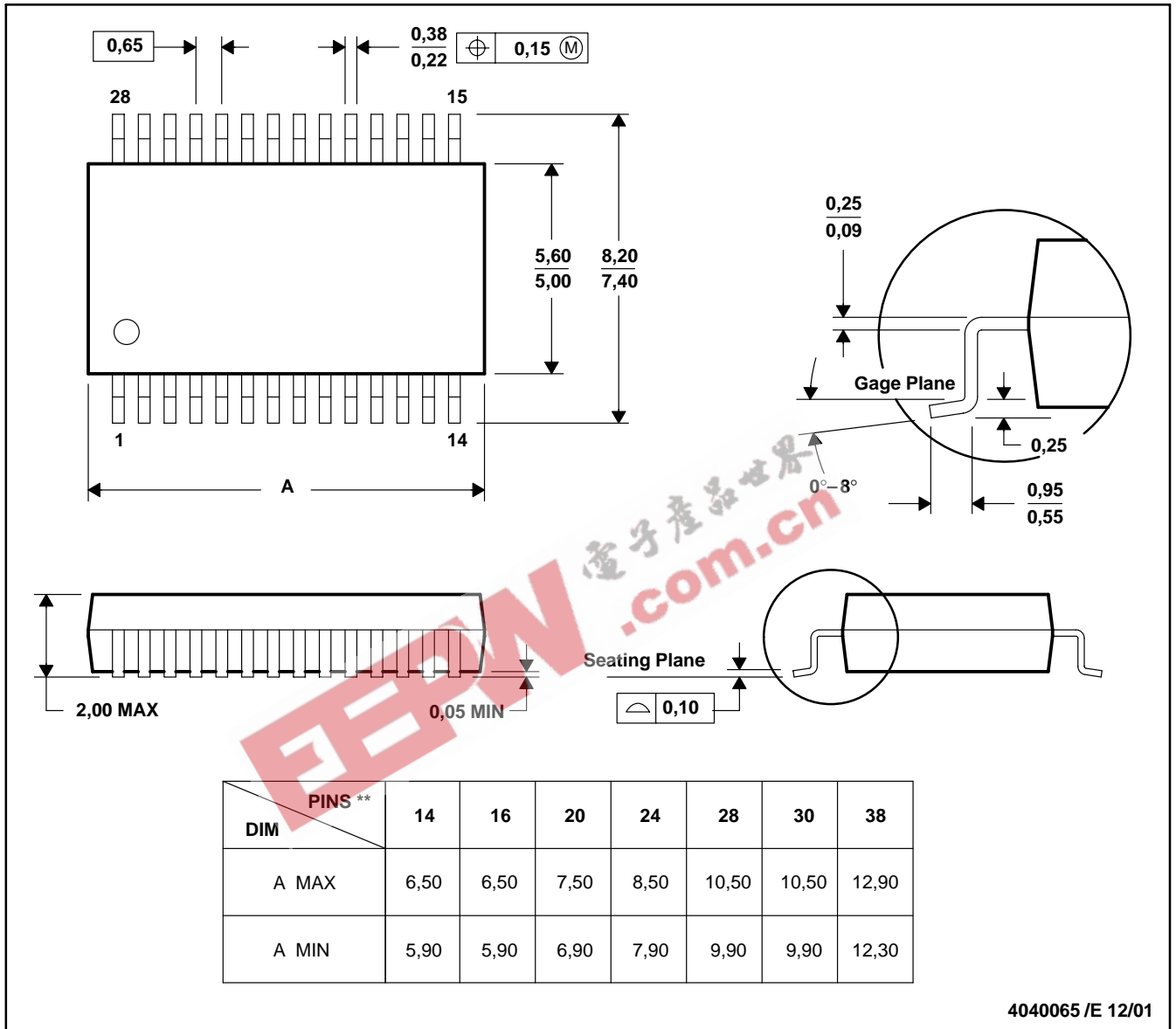
MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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