

# CD54HC4060, CD74HC4060, CD54HCT4060, CD74HCT4060

Data sheet acquired from Harris Semiconductor SCHS207G

#### February 1998 - Revised October 2003

# High-Speed CMOS Logic 14-Stage Binary Counter with Oscillator

#### Features

- Onboard Oscillator
- Common Reset
- Negative-Edge Clocking
- Fanout (Over Temperature Range)
  - Standard Outputs................ 10 LSTTL Loads
  - Bus Driver Outputs ...... 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N<sub>IL</sub> = 30%, N<sub>IH</sub> = 30% of V<sub>CC</sub> at V<sub>CC</sub> = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
     V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility,  $I_1 \le 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

#### Description

The 'HC4060 and 'HCT4060 each consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on

the negative transition of  $\phi I$  (and  $\phi O$ ). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse-line permits unlimited rise and fall times.

In order to achieve a symmetrical waveform in the oscillator section the HCT4060 input pulse switch points are the same as in the HC4060; only the MR input in the HCT4060 has TTL switching levels.

#### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4060F3A	-55 to 125	16 Ld CERDIP
CD54HCT4060F3A	-55 to 125	16 Ld CERDIP
CD74HC4060E	-55 to 125	16 Ld PDIP
CD74HC4060M	-55 to 125	16 Ld SOIC
CD74HC4060MT	-55 to 125	16 Ld SOIC
CD74HC4060M96	-55 to 125	16 Ld SOIC
CD74HC4060PW	-55 to 125	16 Ld TSSOP
CD74HC4060PWR	-55 to 125	16 Ld TSSOP
CD74HC4060PWT	-55 to 125	16 Ld TSSOP
CD74HCT4060E	-55 to 125	16 Ld PDIP
CD74HCT4060M	-55 to 125	16 Ld SOIC
CD74HCT4060MT	-55 to 125	16 Ld SOIC
CD74HCT4060M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

#### **Pinout**

CD54HC4060, CD54HCT4060 (CERDIP) CD74HC4060 (PDIP, SOIC, TSSOP) CD74HCT4060 (PDIP, SOIC) TOP VIEW Q12 1 16 V<sub>CC</sub> Q13 2 15 Q10 14 Q8 Q14 3 13 Q9 Q6 4 12 MR Q5 5 11 ∮I Q7 6 10 ∳O 9 ¢0 GND 8

#### Functional Diagram Q4 5 Q5 4 12 . Q6 MR -Q7 14-STAGE RIPPLE COUNTER Q8 13 AND OSCILLATOR Q9 15 Q10 Q12 2 Q13 Q14 фΟ **GND** = 8 10 V<sub>CC</sub> = 16 φo. øo 0 Ø4 Q4 Ø14 Q14 Ø1 Q1 ≅o o 10 ø1 o 11 FF14 FF4 ■ FF5 - FF13 ■ Q13 Q4 ø5 $\overline{\mathbf{R}}$ $\overline{\textbf{R}}$ MR 0 12 Q4 5, 4, 6, 14, 13, 15, 1 Q13 Q5 - Q10, Q12 Q14

FIGURE 1. LOGIC BLOCK DIAGRAM

TRUTH TABLE

øl	MR	OUTPUT STATE
1	L	No Change
$\downarrow$	L	Advance to Next State
Х	Н	All Outputs are Low

#### **Absolute Maximum Ratings Thermal Information** DC Supply Voltage, VCC $\,$ -0.5V to 7V $\,$ $\theta_{JA}$ (°C/W) Thermal Resistance (Typical, Note 1) DC Input Diode Current, I<sub>IK</sub> M (SOIC) Package..... 73 DC Output Diode Current, $I_{OK}$ PW (TSSOP) Package ..... 108 DC Drain Current, per Output, IO Maximum Storage Temperature Range .....-65°C to 150°C Maximum Lead Temperature (Soldering 10s).....300°C (SOIC - Lead Tips Only) **Operating Conditions** Temperature Range, $T_{\Delta}$ ......55°C to 125°C Supply Voltage Range, V<sub>CC</sub> DC Input or Output Voltage, $V_{\mbox{\scriptsize I}},\,V_{\mbox{\scriptsize O}}$ Input Rise and Fall Time

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE

1. The package thermal impedance is calculated in accordance with JESD 51-7.

#### **DC Electrical Specifications**

		TES CONDIT		V <sub>CC</sub>		25°C		-40°C 1	O 85°C	-55°C TO 125°C																
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MłN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS														
HC TYPES																										
High Level Input	V <sub>IH</sub>	1		2	1.5	-	-	1.5	-	1.5	-	V														
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V														
			6	4.2	-	-	4.2	-	4.2	-	V															
Low Level Input	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V														
Voltage			4.5	-	-	1.35	-	1.35	-	1.35	V															
				6	-	-	1.8	-	1.8	-	1.8	V														
High Level Output	V <sub>OH</sub>	$V_{\text{IH}}$ or $V_{\text{IL}}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V														
Voltage Q Outputs CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V														
OMOG Loddo				-0.02	6	5.9	-	-	5.9	-	5.9	-	V													
High Level Output	1		-	-	-	-	-	-	-	-	-	V														
Voltage Q Outputs TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V														
TTE Edad3			-5.2	6	5.48	-	-	5.34	-	5.2	-	V														
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V														
Voltage Q Outputs CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V														
OWOC Loads		, <b> </b>						-					-			F	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output			-	-	-	-	-	-	-	-	-	V														
Voltage Q Outputs TTL Loads				4	4.5	-	-	0.26	-	0.33	-	0.4	V													
112 20003			5.2	6	-	-	0.26	-	0.33	-	0.4	V														
High-Level Output		V <sub>CC</sub> or	-0.02	2	1.9	-	-	1.9	-	1.9	-	V														
Voltage			GND	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V													
CMOS Loads			-0.02	6	5.9	-	-	5.9	-	5.9	-	V														

# DC Electrical Specifications (Continued)

		TES CONDI		v <sub>cc</sub>		25°C		-40°C T	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
High-Level Output	VoH	V <sub>CC</sub> or	-2.6	4.5	3.98	-	-	3.84	-	3.7	-	V
Voltage		GND	-3.3	6	5.48	-	-	5.34	-	5.2	-	V
Low-Level Output	V <sub>OL</sub>	V <sub>CC</sub> or	0.02	2	•	-	0.1	-	0.1	-	0.1	V
Voltage $\overline{\phi}$ O Output (Pin 10)		GND	0.02	4.5	•	-	0.1	-	0.1	-	0.1	V
CMOS Loads			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low-Level Output	V <sub>OL</sub>	V <sub>CC</sub> or	2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
Voltage		GND	3.3	6	-	-	0.26	-	0.33	-	0.4	V
High-Level Output	V <sub>OH</sub>	V <sub>IL</sub> or V <sub>IH</sub>	-3.2	4.5	3.98	-	-	3.84	-	3.7	-	V
Voltage $\phi$ O Output (Pin 9) TTL Loads			-4.2	6	5.48	-	-	5.34	-	5.2	-	V
Low-Level Output	V <sub>OL</sub>	V <sub>IL</sub> or V <sub>IH</sub>	-2.6	4.5	-	-	0.26	1/4	0.33	-	0.4	V
Voltage $\phi$ O Output (Pin 9) TTL Loads			-3.3	6	20	37	0.26	CI	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> or GND	-	6	7.5	CC	±0.1	-	±1	-	±1	μΑ
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6		_	8	-	80	-	160	μА
HCT TYPES						•						
High Level Input Voltage	V <sub>IH</sub>	1		4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>		-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage Q Outputs CMOS Loads	V <sub>ОН</sub>	V <sub>IH</sub> or V <sub>IL</sub> (Note 3)	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage Q Outputs TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage Q Outputs CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> (Note 3)	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage Q Outputs TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage ∳O Output (Pin 10) CMOS Loads	V <sub>OH</sub>	V <sub>CC</sub> or GND	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>CC</sub> or GND	-2.6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low-Level Output Voltage ∳O Output (Pin 10) CMOS Loads	V <sub>OL</sub>	V <sub>CC</sub> or GND	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V

## DC Electrical Specifications (Continued)

		TES CONDI		v <sub>cc</sub>		25°C		-40°C T	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Low-Level Output Voltage ŌO Output (Pin 10) TTL Loads	V <sub>OL</sub>	V <sub>CC</sub> or GND	2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage φΟ Output (Pin 9) TTL Loads	V <sub>ОН</sub>	V <sub>IL</sub> or V <sub>IH</sub>	-3.2	4.5	3.98	-	-	3.84	-	3.7	-	V
Low-Level Output Voltage $\phi$ O Output (Pin 9) TTL Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> (Note 3)	3.2	4.5	-		0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	Any Voltage Between V <sub>CC</sub> and GND	-	5.5	-		±0.1	9	±1	-	±1	μА
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	- 35	8	; / <sup>13</sup>	80	-	160	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 4)	V <sub>CC</sub> - 2.1	-	4.5 to 5.5	3	100	360	C	450	-	490	μА

#### NOTES:

- 2. Limits not valid when pin 12 (instead of pin 11) is used as control input.
- 3. For pin 11  $V_{IH}$  = 3.15V,  $V_{IL}$  = 0.9V.
- 4. For dual-supply systems theoretical worst case ( $V_1 = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

#### **HCT Input Loading Table**

INPUT	UNIT LOADS
MR	0.35

NOTE: Unit Load is  $\Delta l_{CC}$  limit specified in DC Electrical Specifications Table, e.g. 360  $\mu A$  max at  $25^{o}C.$ 

## **Prerequisite for Switching Specifications**

			25°C		-40°C TO 85°C			-55°C TO 125°C				
PARAMETER	SYMBOL	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
HC TYPES											•	•
Maximum Input Pulse	f <sub>max</sub>	2	6	-	-	5	-	-	4	-	-	MHz
Frequency		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Input Pulse Width	t <sub>W</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Reset Removal Time	t <sub>REM</sub>	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns

# Prerequisite for Switching Specifications (Continued)

				25°C		-40	°C TO 85	5°C	-55 <sup>0</sup>	C TO 12	5°C	
PARAMETER	SYMBOL	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Reset Pulse Width	t <sub>W</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
HCT TYPES												
Maximum Input, Pulse Frequency	f <sub>max</sub>	4.5	30	-	-	25	-	-	20	-	-	MHz
Input Pulse Width	t <sub>W</sub>	4.5	16	-	-	20	-	-	24	-	-	ns
Reset Removal Time	t <sub>REM</sub>	4.5	26	-	-	33	-	-	39	-	-	ns
Reset Pulse Width	t <sub>W</sub>	4.5	25	-	-	31	-	-	38	-	-	ns

## **Switching Specifications** Input $t_r$ , $t_f = 6ns$

		TEST			25°C			C TO °C	-55 <sup>0</sup> 12	C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES	•				36	12	-10			•	
Propagation Delay	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	20 2	130	300	-	375	-	450	ns
φI to Q4			4.5		.0	60	-	75	-	90	ns
		C <sub>L</sub> = 15pF	5	-	25	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	51	-	64	-	78	ns
Q <sub>n</sub> to Q <sub>n+1</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	80	-	100	-	120	ns
			4.5	-	-	16	-	20	-	24	ns
		C <sub>L</sub> = 15pF	5	-	6	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	14	-	17	-	20	ns
MR to Q <sub>n</sub>	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	30	-	37	-	45	ns
Output Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C <sub>I</sub> (TBD)										
Propagation Dissipation Capacitance (Notes 5, 6)	C <sub>PD</sub>	-	-	-	40	-	-	-	-	-	pF
HCT TYPES	•										
Propagation Delay	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	-	-	-	-	-	-ns
φl to Q4			4.5	i	-	66	-	83	ı	100	ns
		C <sub>L</sub> = 15pF	5	-	25	-	-	-	·	-	-ns
		C <sub>L</sub> = 50pF	6	-	-	-	-	-	-	-	-ns

## Switching Specifications Input $t_r$ , $t_f = 6ns$ (Continued)

	TEST				25°C			С ТО °С		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Q <sub>n</sub> to Q <sub>n+1</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	-	-	-	-	-	ns
			4.5	-	-	16	-	20	-	24	ns
		C <sub>L</sub> = 15pF	5	-	6	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	-	-	-	-	-	ns
MR to Q <sub>n</sub>	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	-	-	-	-	-	ns
			4.5	-	-	44	-	55	-	66	ns
		C <sub>L</sub> = 15pF	5	-	17	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	-	-	-	-	-	ns
Output Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF	2	-	-	-	-	=	-	-	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	32.		-	-	-	ns
Input Capacitance	C <sub>I</sub> (TBD)			-3	卷	13.	SI				
Propagation Dissipation Capacitance (Notes 5, 6)	C <sub>PD</sub>	-		<b>E</b>	40	14.	-	-	-	-	pF

#### NOTES:

- 5. C<sub>PD</sub> is used to determine the dynamic power consumption, per package.
- 6.  $P_D = C_{PD} V_{CC}^2 f_i \Sigma (C_L V_{CC}^2 f_i/M)$  where  $M = 2^1, 2^2, 2^3, ...2^{14}, f_i = input$  frequency,  $C_L = output$  load capacitance.

10<sup>2</sup>

10

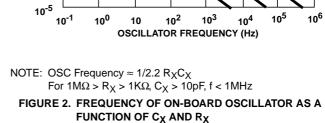
© 10<sup>-1</sup>

10<sup>-3</sup>

10<sup>-4</sup>

## TYPICAL LIMIT VALUES FOR RX AND CX

PARAMETER	TEST CONDITIONS	VOLTAGE	TYPICAL MAXIMUM LIMITS
R <sub>X</sub> Minimum	C <sub>X</sub> > 1000pF	2	1ΚΩ
	C <sub>X</sub> > 10pF	4.5	
	C <sub>X</sub> > 10pF	6	
R <sub>X</sub> Maximum	C <sub>X</sub> > 10pF	2	20ΜΩ
	C <sub>X</sub> > 10pF	4.5	
	C <sub>X</sub> > 10pF	6	
C <sub>X</sub> Minimum	R <sub>X</sub> > 10KΩ	2	10pF
	R <sub>X</sub> > 10KΩ	4.5	
	R <sub>X</sub> > 10KΩ	6	
	$R_X = 1K\Omega$	2	1000pF
	$R_X = 1K\Omega$	4.5	10pF
	$R_X = 1K\Omega$	6	10pF
Maximum Astable Oscillator	$C_X = 1000 pF$ , $R_X = 1 K\Omega$	2	0.5MHz (Note 7)
Frequency	C <sub>X</sub> = 100pF,	4.5	3MHz
	$R_X = 1K\Omega$		(Note 7)
	$C_X = 100 pF$ , $R_X = 1 K\Omega$	6	3MHz (Note 7)



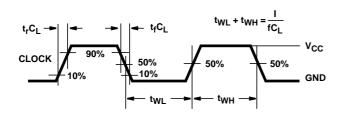
 $T_A = 25^{\circ}C$  $R_X = 1K\Omega$ 

· 10ΚΩ · 100ΚΩ · 100ΚΩ · 10ΜΩ

#### NOTE:

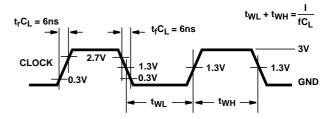
7. At very high frequencies  $f = 1/2.2 R_X C_X$  no longer gives an accurate approximation.

## **Typical Performance Curves**



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 3. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 4. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

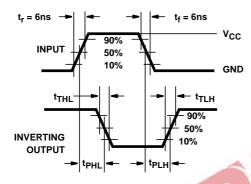


FIGURE 5. HC AND HCT TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC

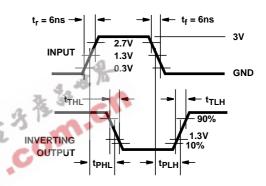


FIGURE 6. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC





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## **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-8768001EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8977101EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC4060F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HCT4060F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC4060E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4060EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4060M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060M96G4	ACTIVE	SOIC	D	16	<b>2</b> 500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT4060EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT4060M	ACTIVE	SOIC	D	16	40	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM



#### PACKAGE OPTION ADDENDUM

24-May-2007

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
CD74HCT4060M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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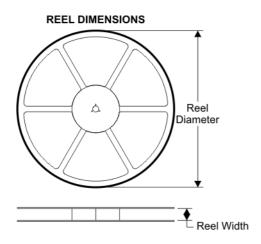
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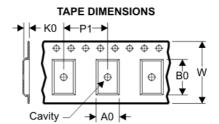


## **PACKAGE MATERIALS INFORMATION**

22-Sep-2007

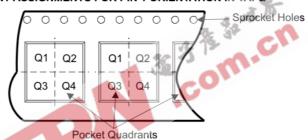
## TAPE AND REEL BOX INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPES

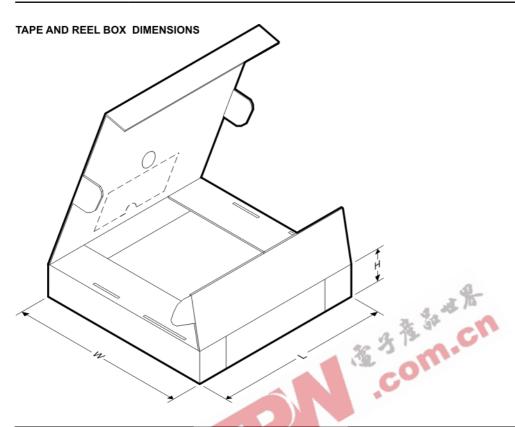


Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4060M96	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1
CD74HC4060PWR	PW	16	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1
CD74HCT4060M96	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1



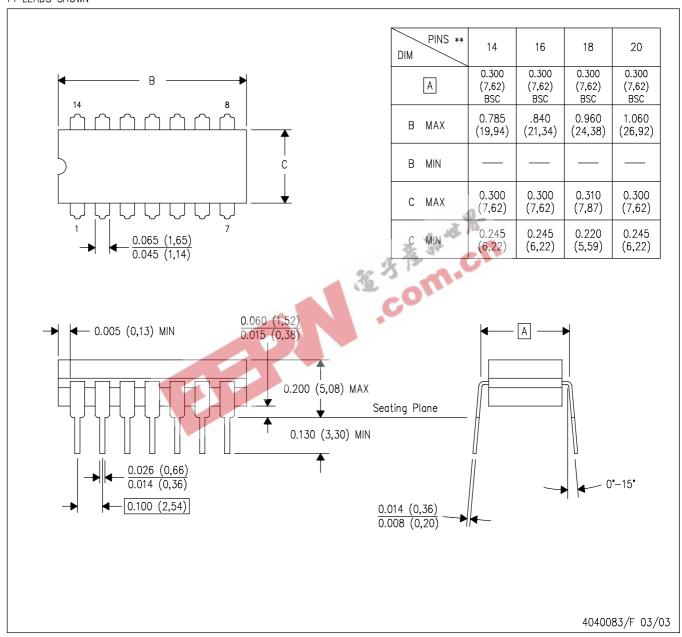


22-Sep-2007



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD74HC4060M96	D i	16	SITE 27	342.9	336.6	0.0
CD74HC4060PWR	PW	16	SITE 41	346.0	346.0	0.0
CD74HCT4060M96	D	16	SITE 27	342.9	336.6	0.0

14 LEADS SHOWN



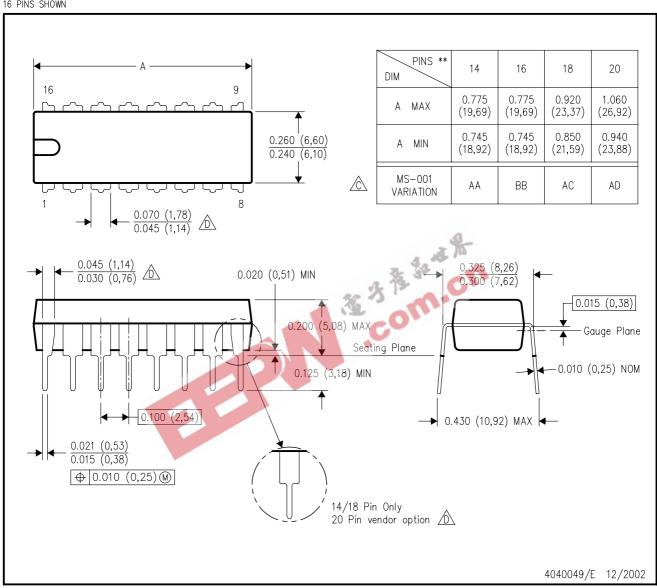
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- $E. \quad \text{Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.} \\$

# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

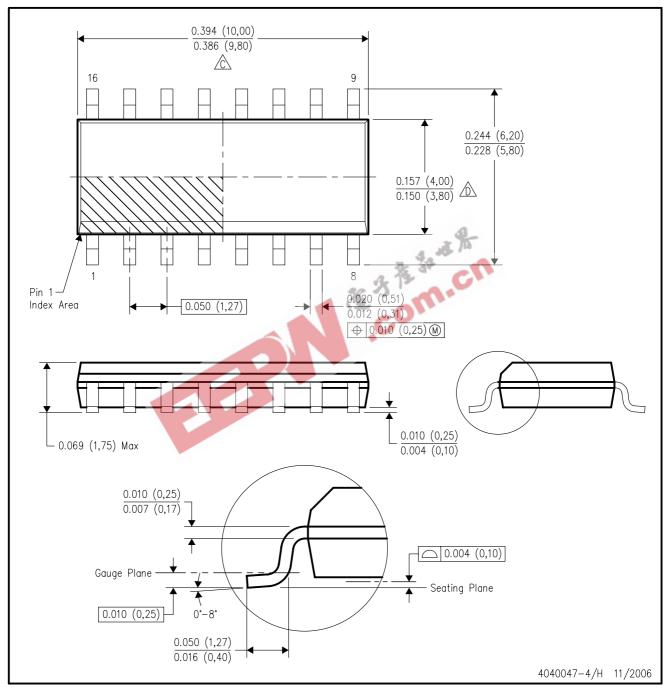


NOTES:

- All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

# D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- A. All linear dimensions are in inches (millimeters).
  B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

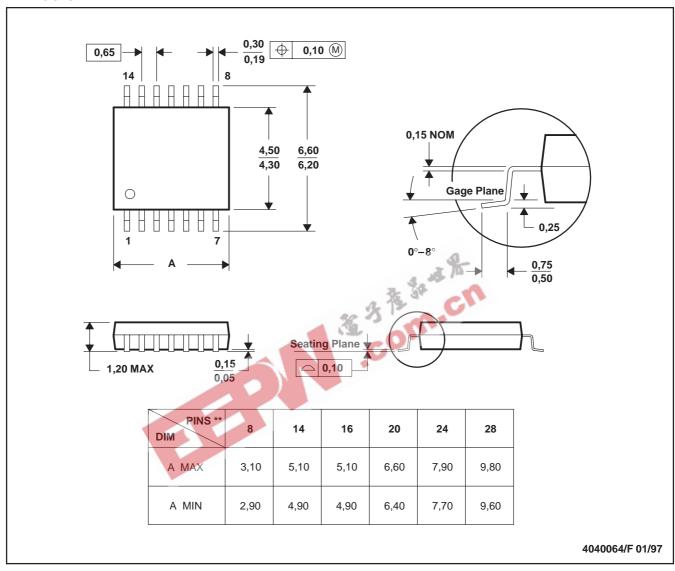
  E. Reference JEDEC MS-012 variation AC.



## PW (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### 14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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