TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS207G

February 1998 - Revised October 2003

CD54HC4060, CD74HC4060, CD54HCT4060, CD74HCT4060

High-Speed CMOS Logic
14-Stage Binary Counter with Oscillator

Features

- **Onboard Oscillator**
- **Common Reset**
- **Negative-Edge Clocking**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
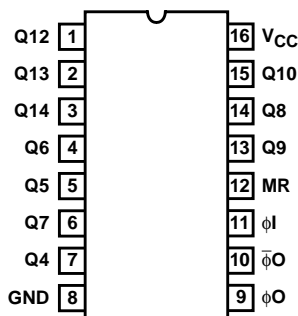 - **CMOS Input Compatibility, $I_I \le 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC4060 and 'HCT4060 each consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of φI (and φO). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse-line permits unlimited rise and fall times.

In order to achieve a symmetrical waveform in the oscillator section the HCT4060 input pulse switch points are the same as in the HC4060; only the MR input in the HCT4060 has TTL switching levels.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4060F3A	-55 to 125	16 Ld CERDIP
CD54HCT4060F3A	-55 to 125	16 Ld CERDIP
CD74HC4060E	-55 to 125	16 Ld PDIP
CD74HC4060M	-55 to 125	16 Ld SOIC
CD74HC4060MT	-55 to 125	16 Ld SOIC
CD74HC4060M96	-55 to 125	16 Ld SOIC
CD74HC4060PW	-55 to 125	16 Ld TSSOP
CD74HC4060PWR	-55 to 125	16 Ld TSSOP
CD74HC4060PWT	-55 to 125	16 Ld TSSOP
CD74HCT4060E	-55 to 125	16 Ld PDIP
CD74HCT4060M	-55 to 125	16 Ld SOIC
CD74HCT4060MT	-55 to 125	16 Ld SOIC
CD74HCT4060M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC4060, CD54HCT4060 (CERDIP)
CD74HC4060 (PDIP, SOIC, TSSOP)
CD74HCT4060 (PDIP, SOIC)
TOP VIEW

Q12	1	16 V_{CC}
Q13	2	15 Q10
Q14	3	14 Q8
Q6	4	13 Q9
Q5	5	12 MR
Q7	6	11 φI
Q4	7	10 $\overline{\phi O}$
GND	8	9 φO

CD54/74HC4060, CD54/74HCT4060

Functional Diagram

14-STAGE RIPPLE COUNTER AND OSCILLATOR

MR — 12

φI — 11

Pin	Output
7	Q4
5	Q5
4	Q6
6	Q7
14	Q8
13	Q9
15	Q10
1	Q12
2	Q13
3	Q14

φO — 9
$\overline{\phi}$O — 10

GND = 8
V_CC = 16

ØO — 9
$\overline{Ø}$O — 10
Ø1 — 11
MR — 12

FF1   FF4   FF5 - FF13   FF14

Q4   5, 4, 6, 14, 13, 15, 1   Q13   Q14
     Q5 - Q10, Q12

7   3
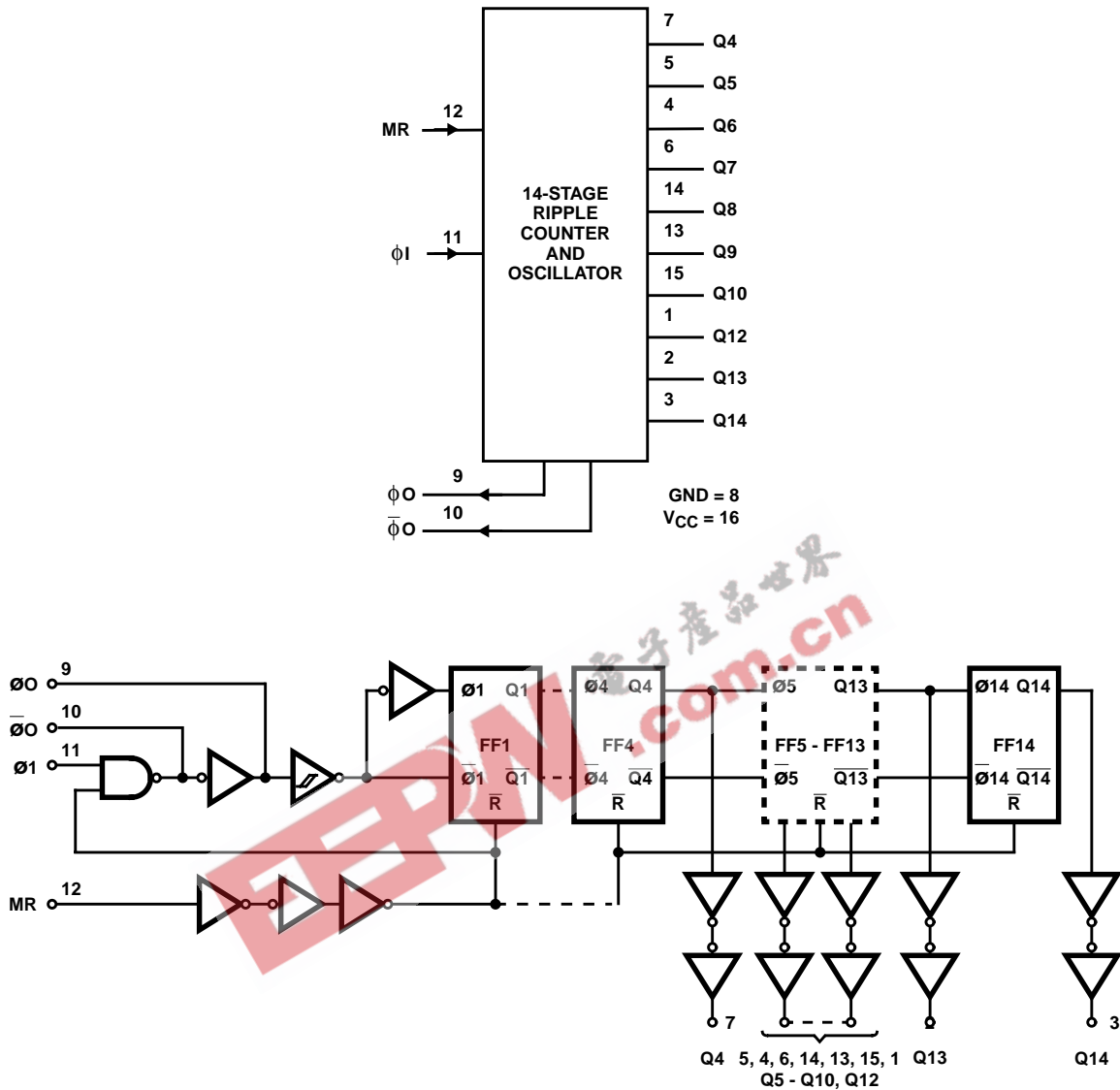
FIGURE 1. LOGIC BLOCK DIAGRAM

TRUTH TABLE

øI	MR	OUTPUT STATE
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs are Low

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CD54/74HC4060, CD54/74HCT4060

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
    For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
    For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
    For -0.5V < V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
    HC Types . . . . .2V to 6V
    HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
    2V . . . . 1000ns (Max)
    4.5V. . . . . 500ns (Max)
    6V . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
    E (PDIP) Package   67
    M (SOIC) Package.   73
    PW (TSSOP) Package 108
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
    (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage Q Outputs CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage Q Outputs TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage Q Outputs CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage Q Outputs TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage φO Output (Pin 10) CMOS Loads	V_{OH}	V_{CC} or GND	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V$_I$ (V)	I$_O$ (mA)	V$_{CC}$ (V)	25°C MIN	TYP	MAX	-40°C TO 85°C MIN	MAX	-55°C TO 125°C MIN	MAX	UNITS
High-Level Output Voltage $\overline{\phi}$O Output (Pin 10) TTL Loads (Note 2)	V$_{OH}$	V$_{CC}$ or GND	-2.6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-3.3	6	5.48	-	-	5.34	-	5.2	-	V
Low-Level Output Voltage $\overline{\phi}$O Output (Pin 10) CMOS Loads	V$_{OL}$	V$_{CC}$ or GND	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low-Level Output Voltage $\overline{\phi}$O Output (Pin 10) TTL Loads	V$_{OL}$	V$_{CC}$ or GND	2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
			3.3	6	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage ϕO Output (Pin 9) TTL Loads	V$_{OH}$	V$_{IL}$ or V$_{IH}$	-3.2	4.5	3.98	-	-	3.84	-	3.7	-	V
			-4.2	6	5.48	-	-	5.34	-	5.2	-	V
Low-Level Output Voltage ϕO Output (Pin 9) TTL Loads	V$_{OL}$	V$_{IL}$ or V$_{IH}$	-2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
			-3.3	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I$_I$	V$_{CC}$ or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I$_{CC}$	V$_{CC}$ or GND	0	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V$_{IH}$	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V$_{IL}$	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage Q Outputs CMOS Loads	V$_{OH}$	V$_{IH}$ or V$_{IL}$ (Note 3)	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage Q Outputs TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage Q Outputs CMOS Loads	V$_{OL}$	V$_{IH}$ or V$_{IL}$ (Note 3)	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage Q Outputs TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage $\overline{\phi}$O Output (Pin 10) CMOS Loads	V$_{OH}$	V$_{CC}$ or GND	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High-Level Output Voltage $\overline{\phi}$O Output (Pin 10) TTL Loads (Note 2)	V$_{OH}$	V$_{CC}$ or GND	-2.6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low-Level Output Voltage $\overline{\phi}$O Output (Pin 10) CMOS Loads	V$_{OL}$	V$_{CC}$ or GND	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V

CD54/74HC4060, CD54/74HCT4060

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V$_I$ (V)	I$_O$ (mA)	V$_{CC}$ (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Low-Level Output Voltage $\overline{\phi}$O Output (Pin 10) TTL Loads	V$_{OL}$	V$_{CC}$ or GND	2.6	4.5	-	-	0.26	-	0.33	-	0.4	V
High-Level Output Voltage ϕO Output (Pin 9) TTL Loads	V$_{OH}$	V$_{IL}$ or V$_{IH}$	-3.2	4.5	3.98	-	-	3.84	-	3.7	-	V
Low-Level Output Voltage ϕO Output (Pin 9) TTL Loads	V$_{OL}$	V$_{IH}$ or V$_{IL}$ (Note 3)	3.2	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I$_I$	Any Voltage Between V$_{CC}$ and GND	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I$_{CC}$	V$_{CC}$ or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI$_{CC}$ (Note 4)	V$_{CC}$ - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

2. Limits not valid when pin 12 (instead of pin 11) is used as control input.

3. For pin 11 V$_{IH}$ = 3.15V, V$_{IL}$ = 0.9V.

4. For dual-supply systems theoretical worst case (V$_I$ = 2.4V, V$_{CC}$ = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
MR	0.35

NOTE: Unit Load is ΔI$_{CC}$ limit specified in DC Electrical Specifications Table, e.g. 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V$_{CC}$ (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C TYP	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C TYP	-55°C TO 125°C MAX	UNITS
HC TYPES												
Maximum Input Pulse Frequency	f$_{max}$	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Input Pulse Width	t$_W$	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Reset Removal Time	t$_{REM}$	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns

Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Reset Pulse Width	t_W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
HCT TYPES												
Maximum Input, Pulse Frequency	f_{max}	4.5	30	-	-	25	-	-	20	-	-	MHz
Input Pulse Width	t_W	4.5	16	-	-	20	-	-	24	-	-	ns
Reset Removal Time	t_{REM}	4.5	26	-	-	33	-	-	39	-	-	ns
Reset Pulse Width	t_W	4.5	25	-	-	31	-	-	38	-	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay φI to Q4	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	51	-	64	-	78	ns
Q_n to Q_{n+1}	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	80	-	100	-	120	ns
			4.5	-	-	16	-	20	-	24	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	14	-	17	-	20	ns
MR to Q_n	t_{PHL}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	30	-	37	-	45	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I (TBD)										
Propagation Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	-	-	40	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay φI to Q4	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	-	-	-	-	-	-ns
			4.5	-	-	66	-	83	-	100	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	-ns
		C_L = 50pF	6	-	-	-	-	-	-	-	-ns

Switching Specifications Input t_r, t_f = 6ns (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Q_n to Q_{n+1}	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	-	-	-	-	-	ns
			4.5	-	-	16	-	20	-	24	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	-	-	-	-	-	ns
MR to Q_n	t_{PHL}	C_L = 50pF	2	-	-	-	-	-	-	-	ns
			4.5	-	-	44	-	55	-	66	ns
		C_L = 15pF	5	-	17	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	-	-	-	-	-	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	-	-	-	-	-	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	-	-	-	-	-	ns
Input Capacitance	C_I (TBD)										
Propagation Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	-	-	-	40	-	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per package.

6. $P_D = C_{PD} V_{CC}^2 f_i \Sigma(C_L V_{CC}^2 f_i/M)$ where M = 2^1, 2^2, 2^3, ...2^{14}, f_i = input frequency, C_L = output load capacitance.

TYPICAL LIMIT VALUES FOR R_X AND C_X

PARAMETER	TEST CONDITIONS	VOLTAGE	TYPICAL MAXIMUM LIMITS
R_X Minimum	C_X > 1000pF	2	1KΩ
	C_X > 10pF	4.5	
	C_X > 10pF	6	
R_X Maximum	C_X > 10pF	2	20MΩ
	C_X > 10pF	4.5	
	C_X > 10pF	6	
C_X Minimum	R_X > 10KΩ	2	10pF
	R_X > 10KΩ	4.5	
	R_X > 10KΩ	6	
	R_X = 1KΩ	2	1000pF
	R_X = 1KΩ	4.5	10pF
	R_X = 1KΩ	6	10pF
Maximum Astable Oscillator Frequency	C_X = 1000pF, R_X = 1KΩ	2	0.5MHz (Note 7)
	C_X = 100pF, R_X = 1KΩ	4.5	3MHz (Note 7)
	C_X = 100pF, R_X = 1KΩ	6	3MHz (Note 7)

NOTE: OSC Frequency ≈ 1/2.2 $R_X C_X$
For 1MΩ > R_X > 1KΩ, C_X > 10pF, f < 1MHz

FIGURE 2. FREQUENCY OF ON-BOARD OSCILLATOR AS A FUNCTION OF C_X AND R_X

NOTE:

7. At very high frequencies f = 1/2.2 $R_X C_X$ no longer gives an accurate approximation.

CD54/74HC4060, CD54/74HCT4060

Typical Performance Curves
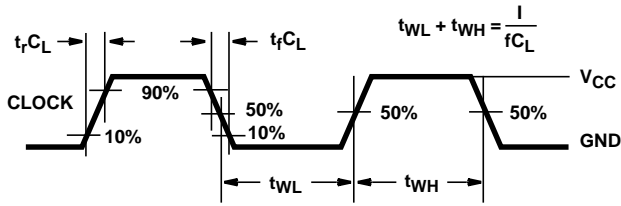
NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 3. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH
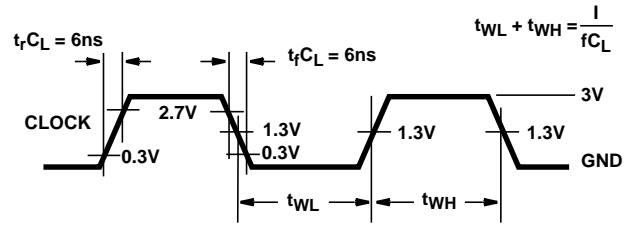
NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 4. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH
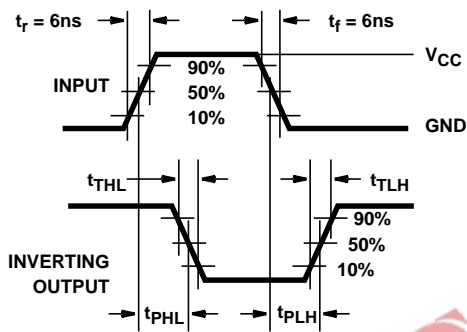
FIGURE 5. HC AND HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
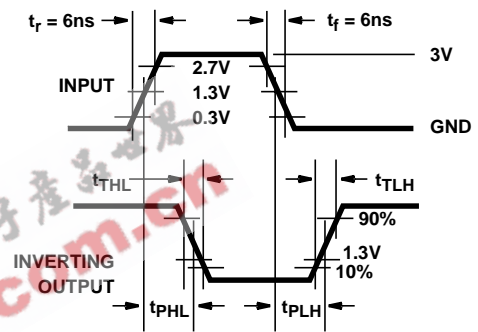
FIGURE 6. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-8768001EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8977101EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC4060F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HCT4060F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC4060E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4060EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4060M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4060PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT4060EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT4060M	ACTIVE	SOIC	D	16	40	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
CD74HCT4060M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4060MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
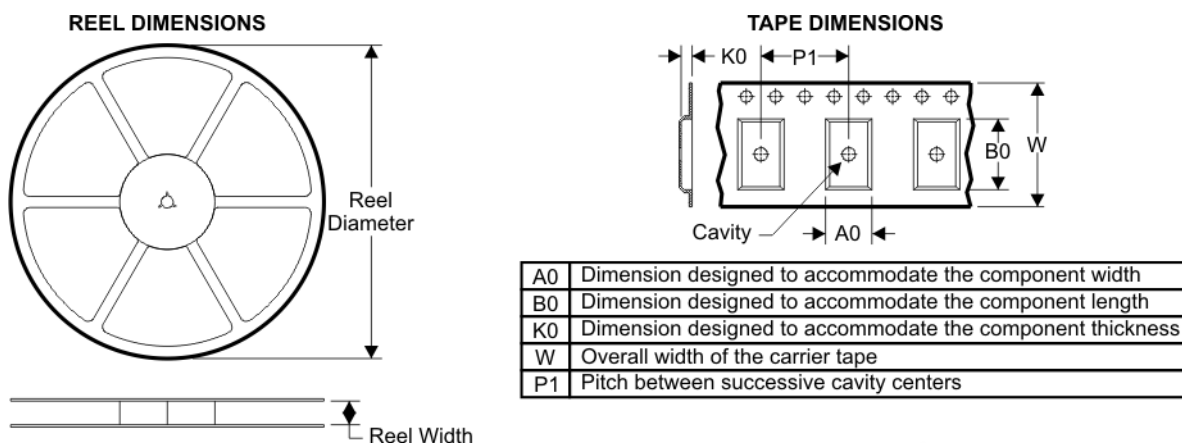
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 Q2
Q3 Q4

Pocket Quadrants
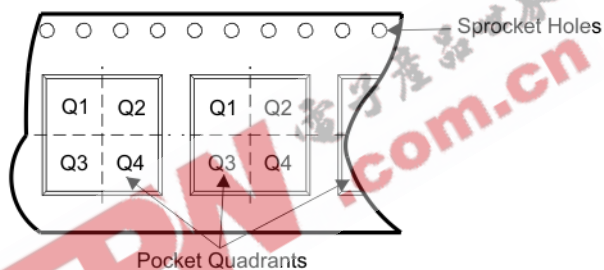
Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4060M96	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1
CD74HC4060PWR	PW	16	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1
CD74HCT4060M96	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1

TAPE AND REEL BOX DIMENSIONS
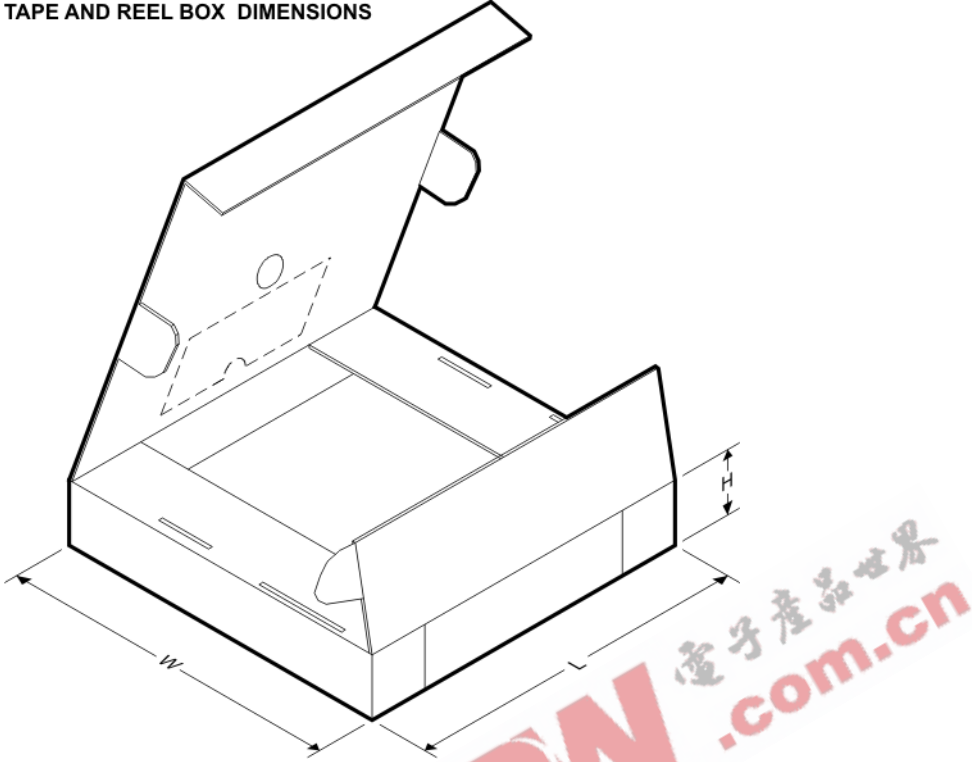
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD74HC4060M96	D	16	SITE 27	342.9	336.6	0.0
CD74HC4060PWR	PW	16	SITE 41	346.0	346.0	0.0
CD74HCT4060M96	D	16	SITE 27	342.9	336.6	0.0

DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65) / 0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52) / 0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66) / 0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36) / 0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN
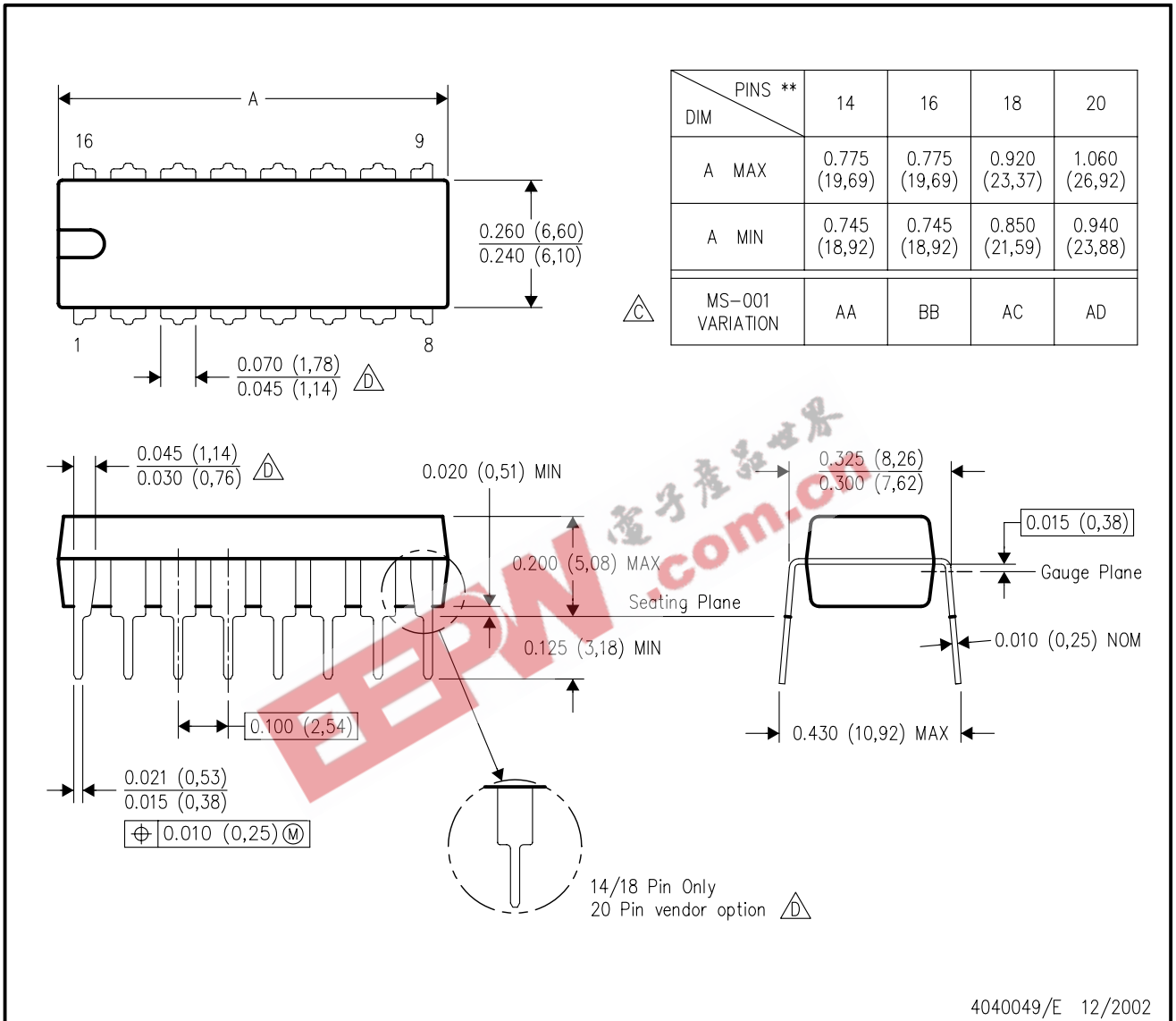
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
C.   Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
www.ti.com

D (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)
Ⓒ

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
Ⓓ

Pin 1
Index Area

1   8

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)
⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
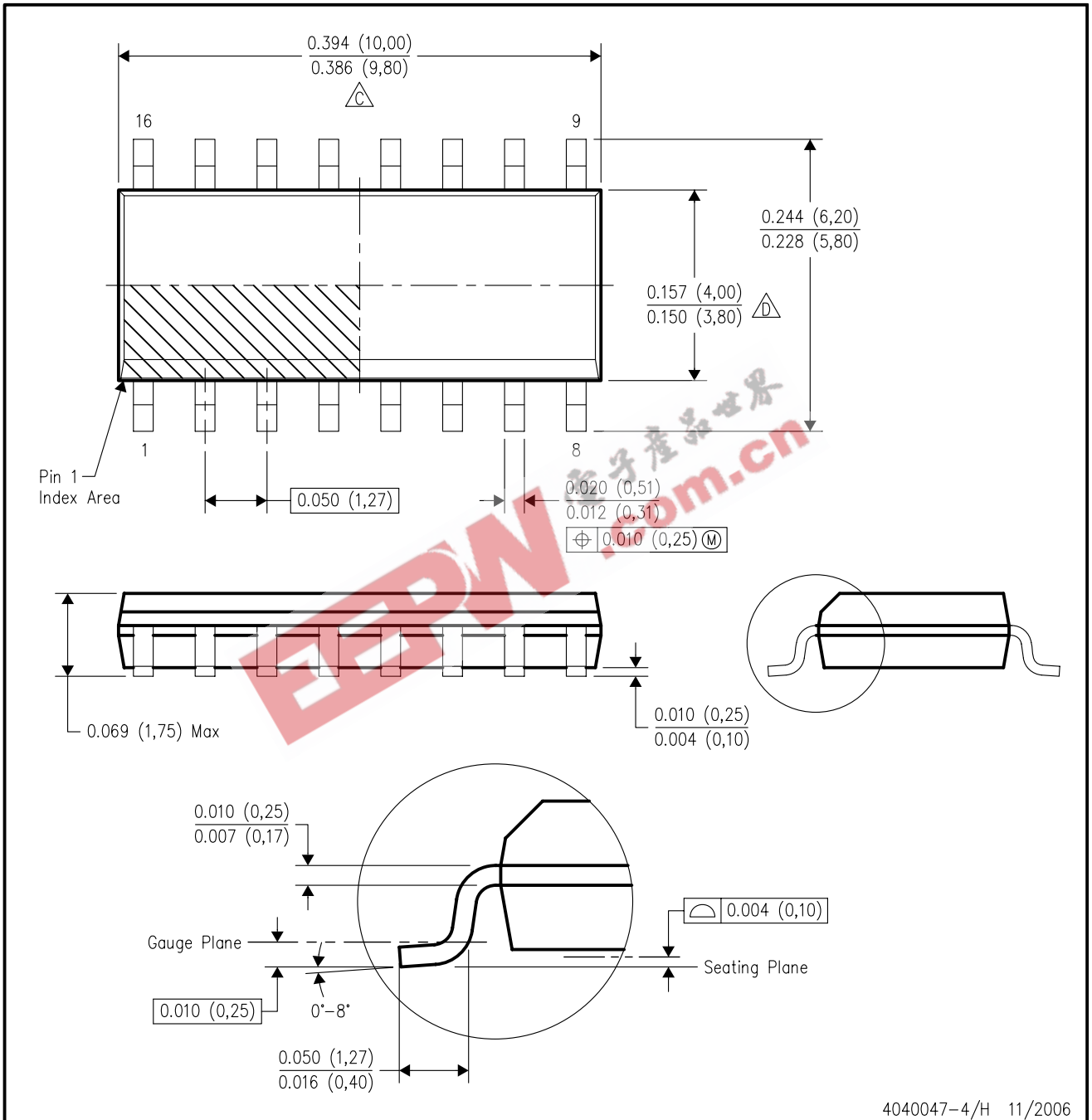
4040047−4/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed .006 (0,15) per end.
         Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E. Reference JEDEC MS−012 variation AC.

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153