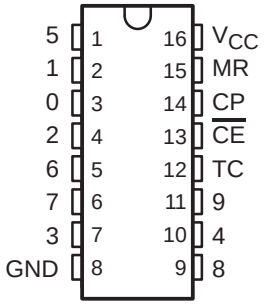
CD54HC4017
DECADE COUNTER/DIVIDER WITH TEN DECODED OUTPUTS

SGDS011 – MAY 1999

- **2-V to 6-V Operation**
- **Fully Static Operation**
- **Buffered Inputs**
- **Common Reset**
- **Positive-Edge Clocking**
- **Balanced Propagation Delay and Transition Times**
- **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V**
- **Packaged in Ceramic (F) DIP Package and Also Available in Chip Form (H)**

F PACKAGE
(TOP VIEW)



description

The CD54HC4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each decoded output normally is low and sequentially goes high on the low-to-high transition of the clock (CP) input. Each output stays high for one clock period of the ten-clock-period cycle. The terminal count (TC) output transitions low to high after output ten (9) goes low, and can be used in conjunction with the clock enable ($\overline{CE}$) input to cascade several stages. $\overline{CE}$ disables counting when in the high state. The master reset (MR) input, when taken high, sets all the decoded outputs, except 0, to low.

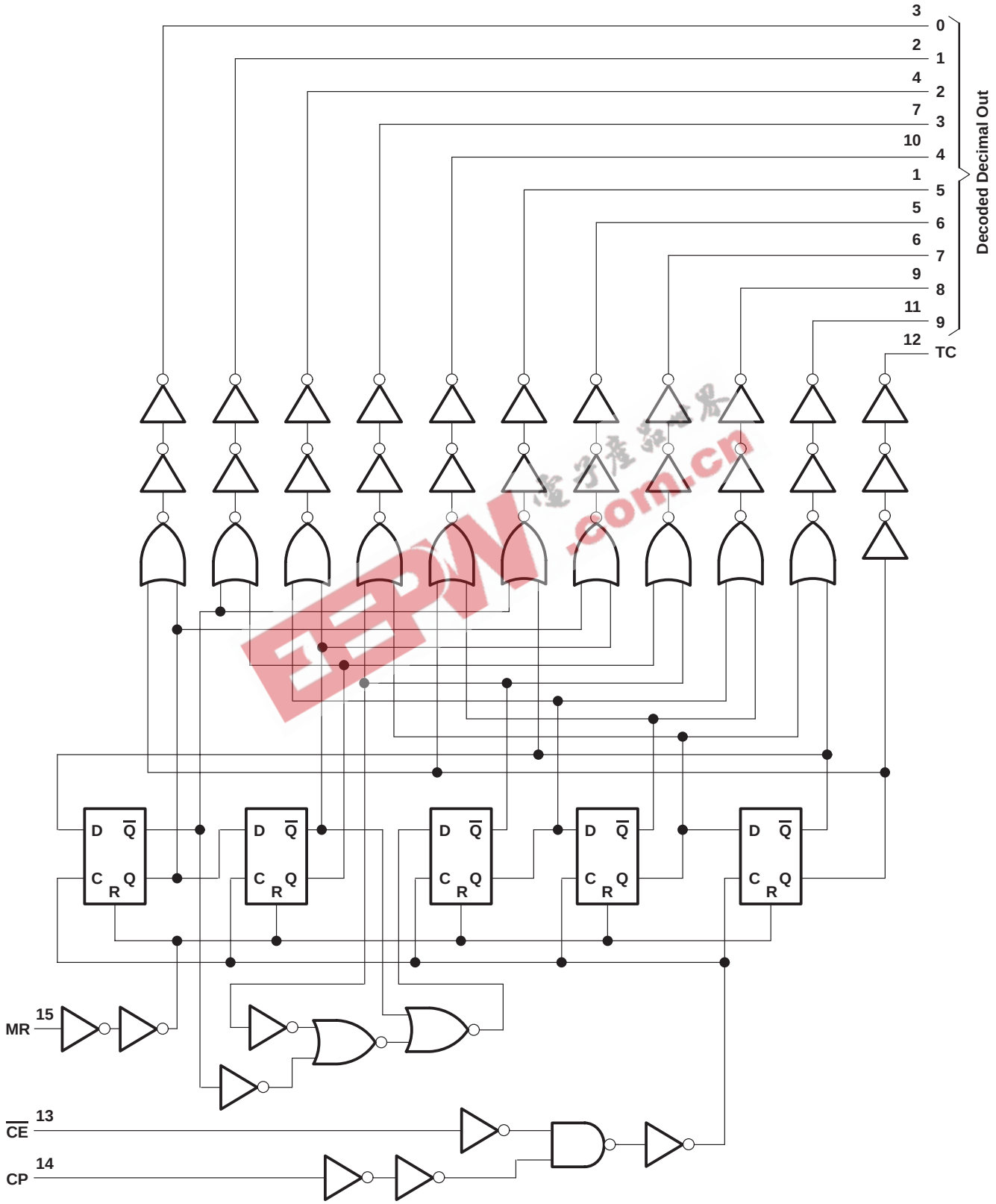
The CD54HC4017 is characterized for operation over the full military temperature range of –55°C to 125°C.

FUNCTION TABLE

INPUTS			OUTPUT STATE†
CP	$\overline{CE}$	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

† If n < 5, TC = H; otherwise, TC = L.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 V or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 V or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, each output pin, I_O (V_O > –0.5 V or V_O < V_{CC} + 0.5 V) . . . . . ±25 mA
V_{CC} or ground current, I_{CC} . . . . . ±50 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating (see Note 1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0	0.5	V
		V_{CC} = 4.5 V	0	1.35	
		V_{CC} = 6 V	0	1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		–55	125	°C

NOTE 1: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

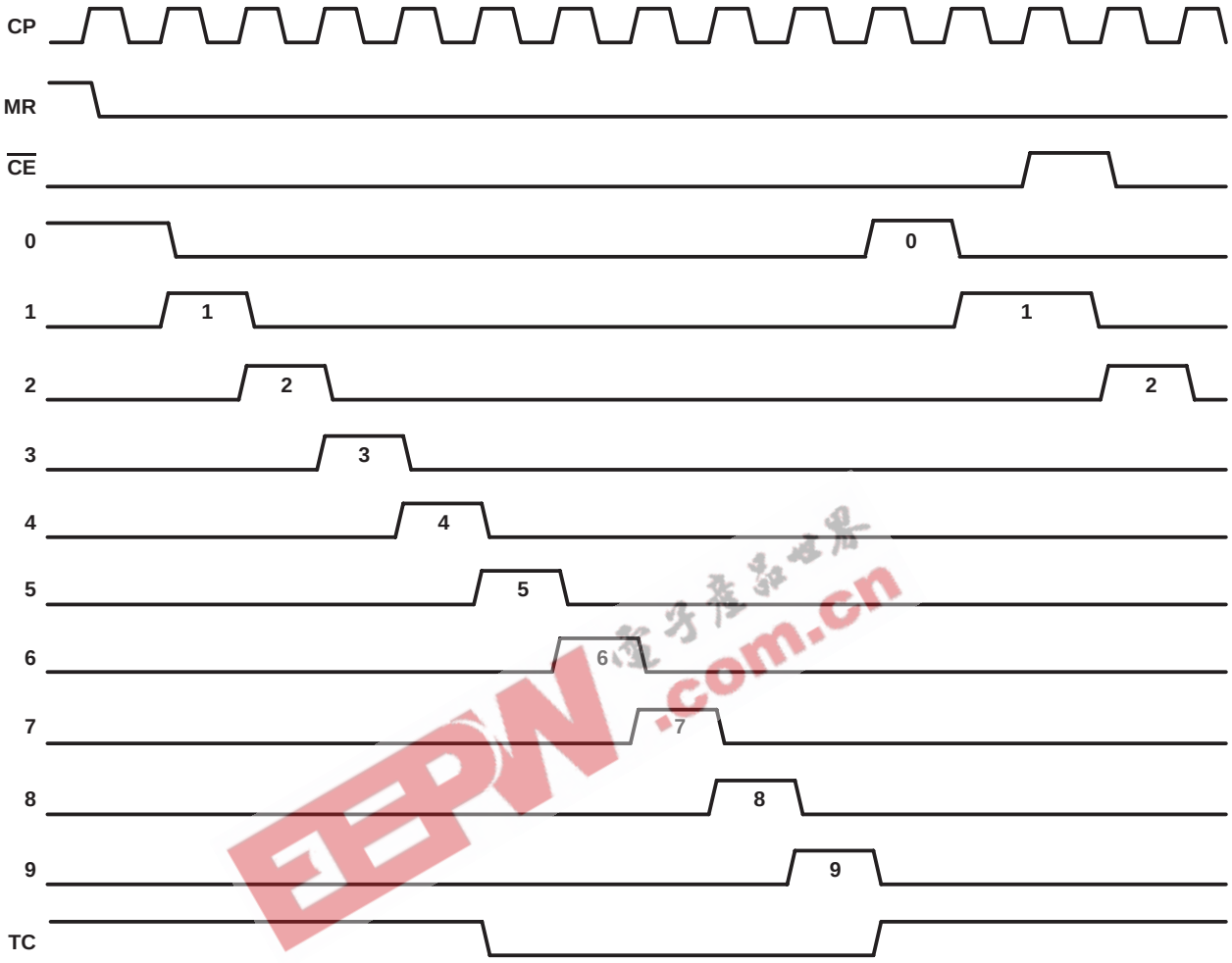
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
					MIN	MAX			
V_{OH}	CMOS loads	V_I = V_{IH} or V_{IL},	I_{OH} = –0.02 mA	2 V	1.9		1.9		V
				4.5 V	4.4		4.4		
				6 V	5.9		5.9		
	TTL loads	V_I = V_{IH} or V_{IL}	I_{OH} = –4 mA	4.5 V	3.98		3.7		
			I_{OH} = –5.2 mA	6 V	5.48		5.2		
V_{OL}	CMOS loads	V_I = V_{IH} or V_{IL},	I_{OL} = 0.02 mA	2 V		0.1		0.1	V
				4.5 V		0.1		0.1	
				6 V		0.1		0.1	
	TTL loads	V_I = V_{IH} or V_{IL}	I_{OL} = 4 mA	4.5 V		0.26		0.4	
			I_{OL} = 5.2 mA	6 V		0.26		0.4	
I_I		V_I = V_{CC} or 0		6 V		±100		±1000	nA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V		8		160	µA
C_i				2 V to 6 V		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f_{clock}	Maximum clock frequency		2 V		6		4	MHz
			4.5 V		30		20	
			6 V		35		23	
t_w	Pulse duration	CP	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
		MR	2 V	80		120		
			4.5 V	16		24		
			6 V	14		20		
t_{su}	Setup time, $\overline{CE}$ to CP		2 V	75		110		ns
			4.5 V	15		22		
			6 V	13		19		
t_h	Hold time, $\overline{CE}$ to CP		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		
t_{rem}	Removal time, MR		2 V	5		5		ns
			4.5 V	5		5		
			6 V	5		5		

timing requirements



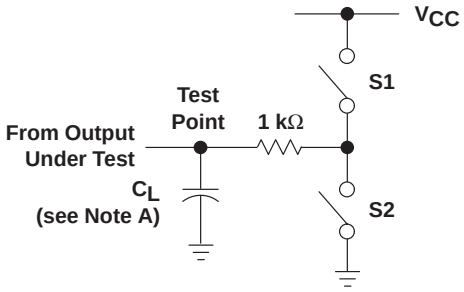
switching characteristics, C_L = 50 pF, T_A = 25°C (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C		T_A = –55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	
f_{max}			2 V	6		4		MHz
			4.5 V	20		20		
			6 V	35		23		
t_{pd}	CP	Any output	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	
t_{pd}		TC	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	
t_{pd}	$\overline{CE}$	Any output	2 V		250		375	ns
			4.5 V		50		75	
			6 V		43		64	
t_{pd}		TC	2 V		250		375	ns
			4.5 V		50		75	
			6 V		43		64	
t_{pd}	MR	Any output	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	
t_{pd}		TC	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	

operating characteristics

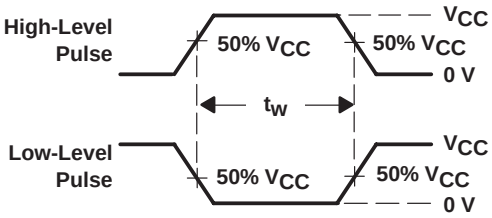
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	39	pF

PARAMETER MEASUREMENT INFORMATION

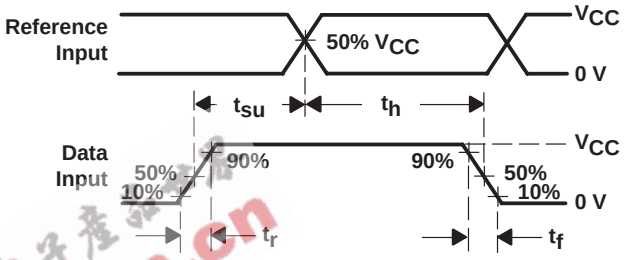


LOAD CIRCUIT

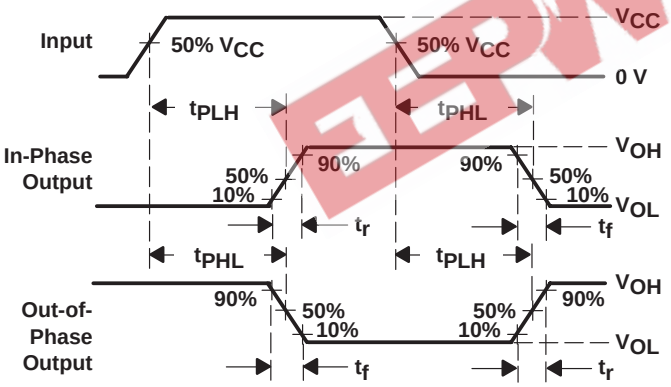
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



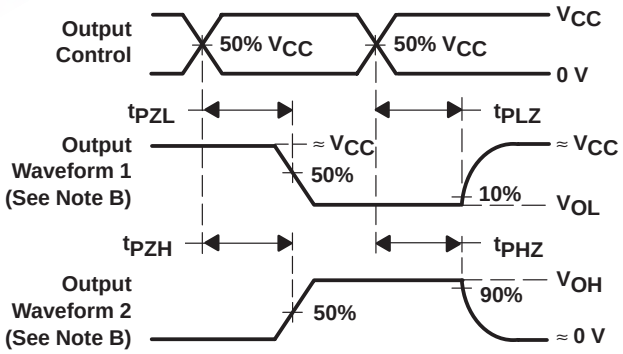
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

INPUT LEVEL	V_{CC}
V_S	0.5 V_{CC}

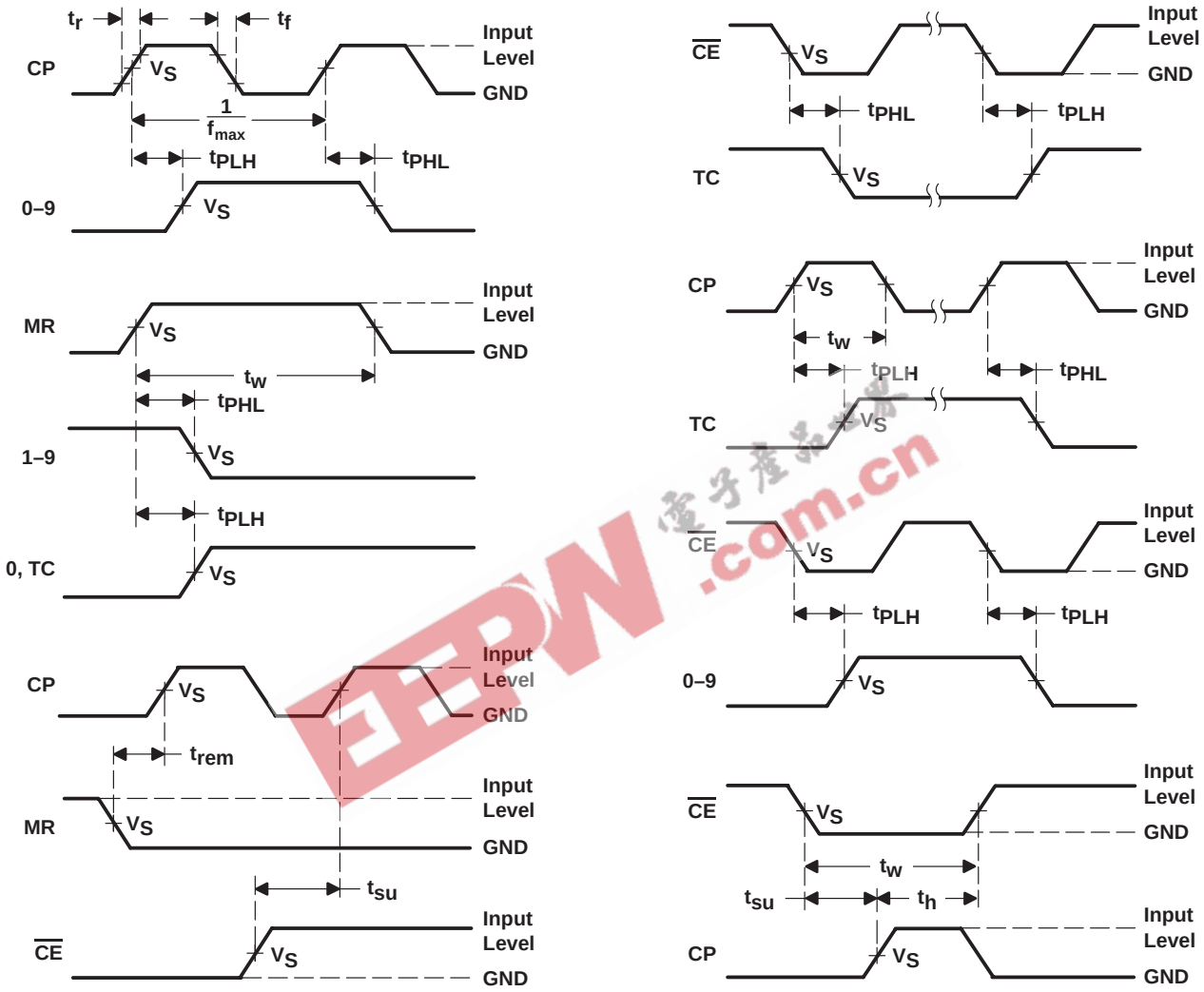


Figure 2. Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.