TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS142F

September 1997 - Revised October 2003

CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

High-Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

Features

- **Overriding Reset Terminates Output Pulse**
- **Triggering From the Leading or Trailing Edge**
- **Q and $\overline{Q}$ Buffered Outputs**
- **Separate Resets**
- **Wide Range of Output-Pulse Widths**
- **Schmitt Trigger on Both $\overline{A}$ and B Inputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC123, 'HCT123, CD74HC423 and CD74HCT423 are dual monostable multivibrators with resets. They are all retriggerable and differ only in that the 123 types can be triggered by a negative to positive reset pulse; whereas the 423 types do not have this feature. An external resistor (R_X) and an external capacitor (C_X) control the timing and the accuracy for the circuit. Adjustment of Rx and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. Pulse triggering on the $\overline{A}$ and B inputs occur at a particular voltage level and is not related to the rise and fall times of the trigger pulses.

Once triggered, the output pulse width may be extended by retriggering inputs $\overline{A}$ and B. The output pulse can be terminated by a LOW level on the Reset (R) pin. Trailing edge triggering ($\overline{A}$) and leading edge triggering (B) inputs are provided for triggering from either edge of the input pulse. If either Mono is not used each input on the unused device ($\overline{A}$, B, and $\overline{R}$) must be terminated high or low.

The minimum value of external resistance, Rx is typically 5kΩ. The minimum value external capacitance, CX, is 0pF. The calculation for the pulse width is t_W = 0.45 $R_X C_X$ at V_{CC} = 5V.

Ordering Information

PART NUMBER	TEMP. RANGE ($^{\circ}$C)	PACKAGE
CD54HC123F3A	-55 to 125	16 Ld CERDIP
CD54HCT123F3A	-55 to 125	16 Ld CERDIP
CD74HC123E	-55 to 125	16 Ld PDIP
CD74HC123M	-55 to 125	16 Ld SOIC
CD74HC123MT	-55 to 125	16 Ld SOIC
CD74HC123M96	-55 to 125	16 Ld SOIC
CD74HC123NSR	-55 to 125	16 Ld SOP
CD74HC123PW	-55 to 125	16 Ld TSSOP
CD74HC123PWR	-55 to 125	16 Ld TSSOP
CD74HC123PWT	-55 to 125	16 Ld TSSOP
CD74HC423E	-55 to 125	16 Ld PDIP
CD74HC423M	-55 to 125	16 Ld SOIC
CD74HC423MT	-55 to 125	16 Ld SOIC
CD74HC423M96	-55 to 125	16 Ld SOIC
CD74HC423NSR	-55 to 125	16 Ld SOP
CD74HCT123E	-55 to 125	16 Ld PDIP
CD74HCT123M	-55 to 125	16 Ld SOIC
CD74HCT123MT	-55 to 125	16 Ld SOIC
CD74HCT123M96	-55 to 125	16 Ld SOIC
CD74HCT423E	-55 to 125	16 Ld PDIP
CD74HCT423MT	-55 to 125	16 Ld SOIC
CD74HCT423M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

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CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

Pinout

TOP VIEW

```
         ┌───┬──┐
  1A  [1 │   U  │16]  VCC
  1B  [2 │      │15]  1RxCx
  1R  [3 │      │14]  1Cx
  1Q  [4 │      │13]  1Q
  2Q  [5 │      │12]  2Q
  2Cx [6 │      │11]  2R
 2RxCx [7│      │10]  2B
 GND  [8 │      │9 ]  2A
         └──────┘
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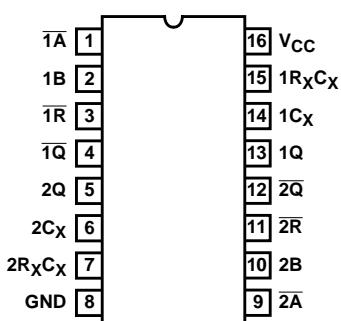
Functional Diagram
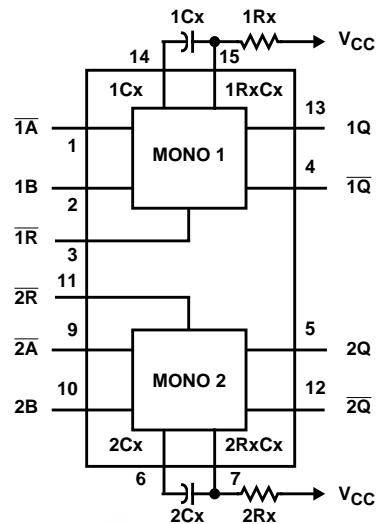
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{A}$	B	$\overline{R}$	Q	$\overline{Q}$
CD74HC/HCT123				
H	X	H	L	H
X	L	H	L	H
L	↑	H	⊓	⊔
↓	H	H	⊓	⊔
X	X	L	L	H
L	H	↑	⊓	⊔
CD74HC/HCT423				
H	X	H	L	H
X	L	H	L	H
L	↑	H	⊓	⊔
↓	H	H	⊓	⊔
X	X	L	L	H

H = High Voltage Level, L = Low Voltage Level,
X = Don't Care.

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CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, $I_{CC \, or} \, I_{GND}$ . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
  HC Types . . . . .2V to 6V
  HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
  E (PDIP) Package . . . . .67°C/W
  M (SOIC) Package. . . . . .73°C/W
  NS (SOP) Package . . . . 64°C/W
  PW (TSSOP) Package . . . . 108°C/W
Maximum Junction Temperature . . . . .150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . .300°C
  (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.35

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g. 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C TYP	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C TYP	-55°C TO 125°C MAX	UNITS
HC TYPES												
Minimum Input, Pulse Width	t_{WL}											
$\overline{A}$		2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns
B	t_{WH}	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns

Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{R}$	t_{WL}	2	100	-	-	125	-	-	150	-	150	ns
		4.5	20	-	-	25	-	-	30	-	30	ns
		6	17	-	-	21	-	-	26	-	26	ns
$\overline{A}$ and B Hold Time	t_H	2	50	-	-	65	-	-	75	-	75	ns
		4.5	10	-	-	13	-	-	15	-	15	ns
		6	9	-	-	11	-	-	13	-	13	ns
Reset Removal Time	t_{REM}	2	50	-	-	65	-	-	75	-	75	ns
		4.5	10	-	-	13	-	-	15	-	15	ns
		6	9	-	-	11	-	-	13	-	13	ns
Retrigger Time Number	t_{rT}	5	-	-	-	-	-	-	-	-	-	ns
R_X = 10KΩ, C_X = 0			-	50	-	-	63	-	-	76	-	ns
Output Pulse Width Q or $\overline{Q}$	t_W	5										
R_X = 10KΩ, C_X = 10nF			40	-	50	38.7	-	51.3	38.2	-	51.8	μs
HCT TYPES												
Minimum Input, Pulse Width	t_{WL}	5										-
$\overline{A}$			20	-	-	25	-	-	30	-	-	ns
B	t_{WH}		20	-	-	25	-	-	30	-	-	ns
$\overline{R}$	t_{WL}		20	-	-	25	-	-	30	-	-	ns
$\overline{A}$ and B Hold Time	t_H	5	10	-	-	13	-	-	15	-	-	ns
Reset Removal Time	t_{REM}	5	10	-	-	13	-	-	15		-	ns
Retrigger Time Number (Note 3) R_X = 10KΩ, C_X = 0	t_{rT}	5	-	50	-	-	63	-	-	76	-	ns
Output Pulse Width Q or Q R_X = 10KΩ, C_X = 10nF	t_W	5	40	-	50	38.7	-	51.3	38.2	-	51.8	μs

NOTE:

3. Time to trigger depends on the values of R_X and C_X. The output pulse width can only be extended when the time between the active-going edges of the trigger input pulses meet the minimum retrigger time requirement.

CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

Switching Specifications Input t_r, t_f = 6ns, R_X = 10KΩ, C_X = 0

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Trigger Propagation Delay $\overline{A}$, B, $\overline{R}$ to Q	t_{PLH}	C_L = 50pF	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	51	-	64	-	76	ns
$\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	2	-	-	320	-	400	-	480	ns
			4.5	-	-	64	-	80	-	96	ns
		C_L = 15pF	5	-	26	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	54	-	68	-	82	ns
Reset Propagation Delay $\overline{R}$ to Q or $\overline{Q}$	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	215	-	270	-	325	ns
			4.5	-	-	43	-	54	-	65	ns
			6	-	-	37	-	46	-	55	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Pulse Width R_X = 10KΩ, C_X = 10nF	-	-	5	-	45	-	-	-	-	-	µs
Pulse Width Match Between Circuits In the Same Package R_X = 10KΩ, C_X = 10pF	-	-	5	-	±2	-	-	-	-	-	%
Power Dissipation Capacitance (Note 4)	C_{PD}	C_L = 15pF	5	-	-	-	-	-	-	-	pF
Input Capacitance	C_{IN}	C_L = 50pF	-	10	-	10	-	10	-	10	pF
HCT TYPES											
Trigger Propagation Delay $\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PLH}	C_L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
$\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	4.5	-	-	68	-	85	-	102	ns
		C_L =15pF	5	-	27	-	-	-	-	-	ns
Reset Propagation Delay $\overline{R}$ to Q or $\overline{Q}$	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	48	-	60	-	72	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Output Pulse Width R_X = 10KΩ, C_X = 10nF	-	-	5	-	45	-	-	-	-	-	µs

CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

Switching Specifications Input t_r, t_f = 6ns, R_X = 10KΩ, C_X = 0 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Pulse Width Match Between Circuits In the Same Package R_X = 10KΩ, C_X = 10pF	-	-	5		±2	-	-	-	-	-	%
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF

NOTE:

4. C_{PD} is used to determine the dynamic power consumption, per multivibrator.

$P_D = (C_{PD} + C_X) V_{CC}^2 f_i \Sigma(C_L V_{CC}^2 f_O)$

Where

f_i = input frequency
f_O = Output Frequency
C_L = Output Load Capacitance
C_X = External Capacitance
V_{CC} = Supply Voltage,
assuming $f_i \ll \dfrac{1}{t_W}$

Test Circuits and Waveforms
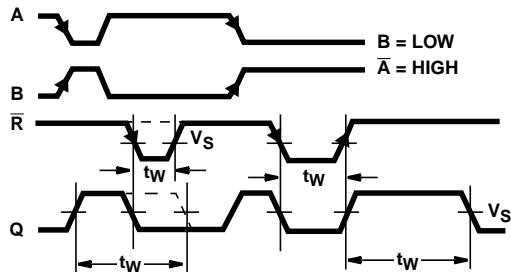
FIGURE 1. OUTPUT PULSE CONTROL USING RESET INPUT ($\overline{R}$) PULSE FOR 123
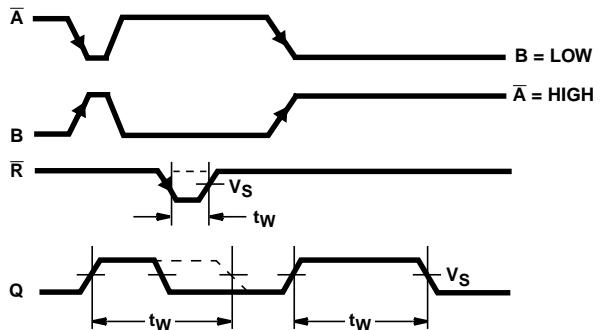
FIGURE 2. OUTPUT PULSE CONTROL USING RESET INPUT ($\overline{R}$) FOR 423
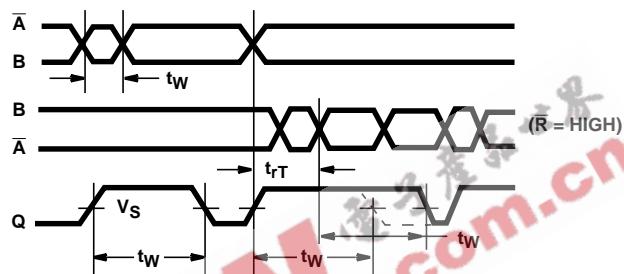
NOTE: Output pulse control using retrigger pulse for 123 and 423.

FIGURE 3. TRIGGERING OF ONE SHOT BY INPUT $\overline{A}$ OR INPUT B FOR A PERIOD t_W
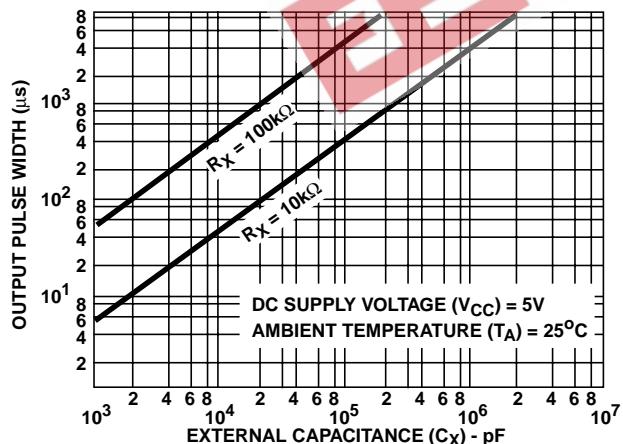
FIGURE 4. TYPICAL OUTPUT PULSE WIDTH AS A FUNCTION OF C_X FOR R_X = 10kΩ AND 100kΩ
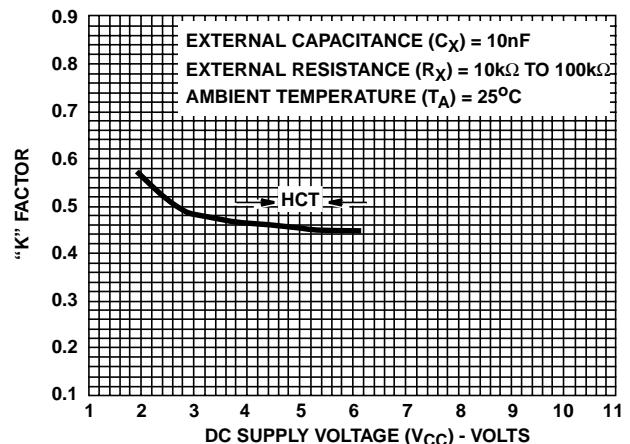
FIGURE 5. TYPICAL "K" FACTOR AS A FUNCTION OF V_{CC}

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-8684701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8970001EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC123F	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC123F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HCT123F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC123E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC123EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC123M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC123PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC423E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC423EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC423M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC423M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC423M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC423ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD74HC423MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC423MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC423NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC423NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT123E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT123EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT123M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT123M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT123M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT123ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT123MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT123MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT423E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT423EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT423M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT423M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT423MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT423MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\dfrac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\dfrac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\dfrac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

A

0°-15°

$\dfrac{0.014\ (0,36)}{0.008\ (0,20)}$
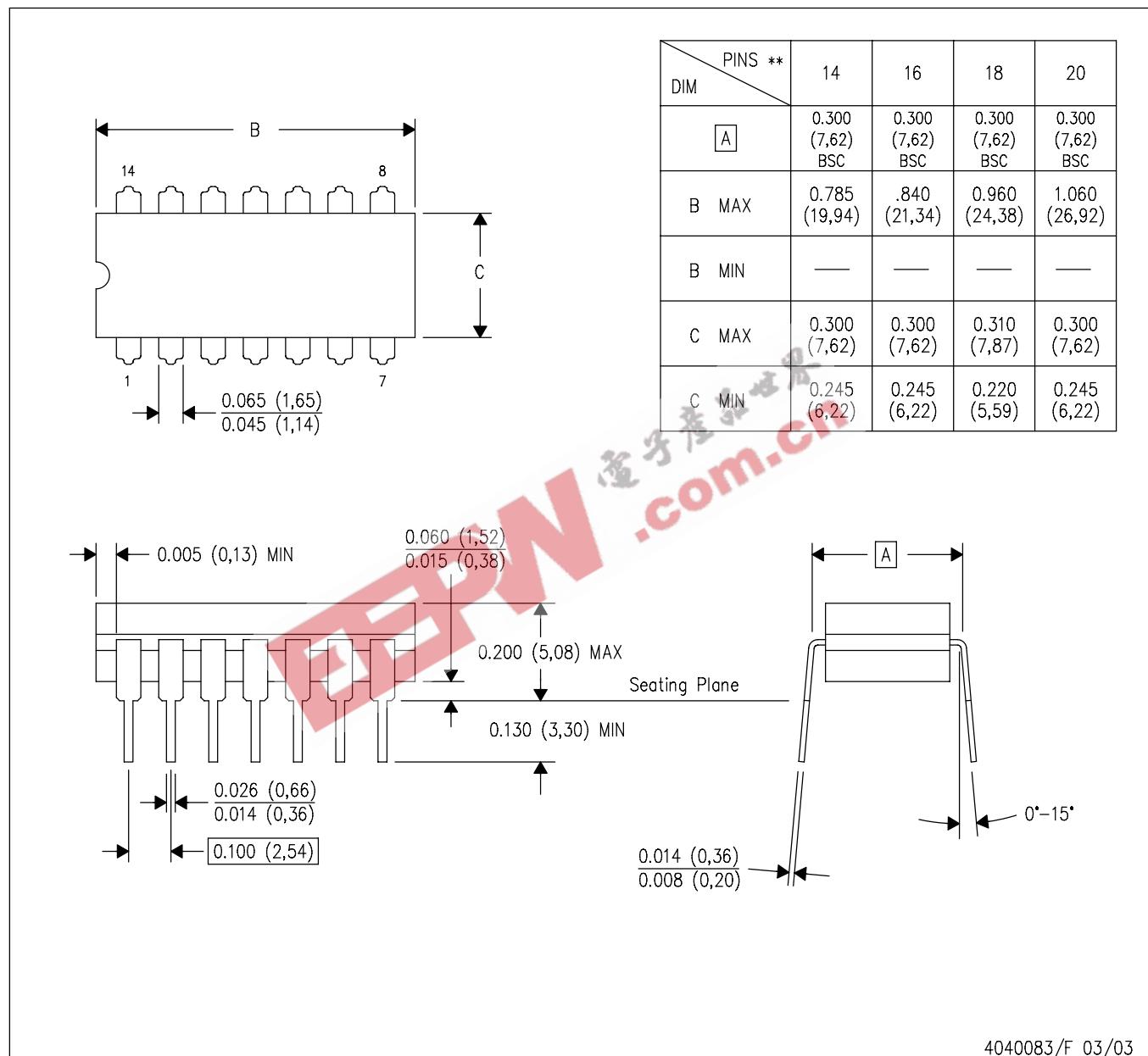
4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
    △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
    △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)
Ⓒ

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
Ⓓ

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
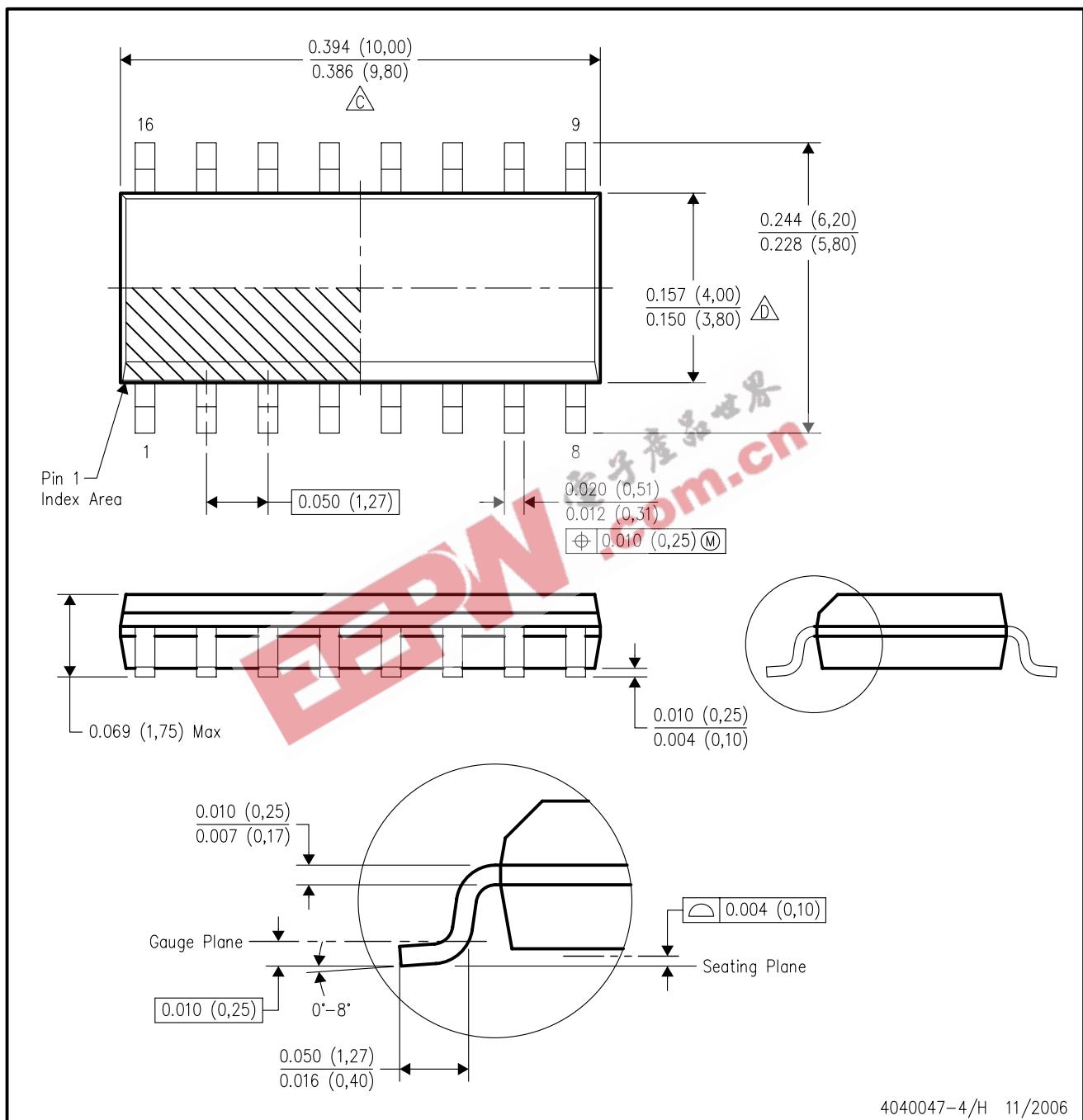
4040047−4/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed .006 (0,15) per end.
        Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
        E. Reference JEDEC MS−012 variation AC.

MECHANICAL DATA
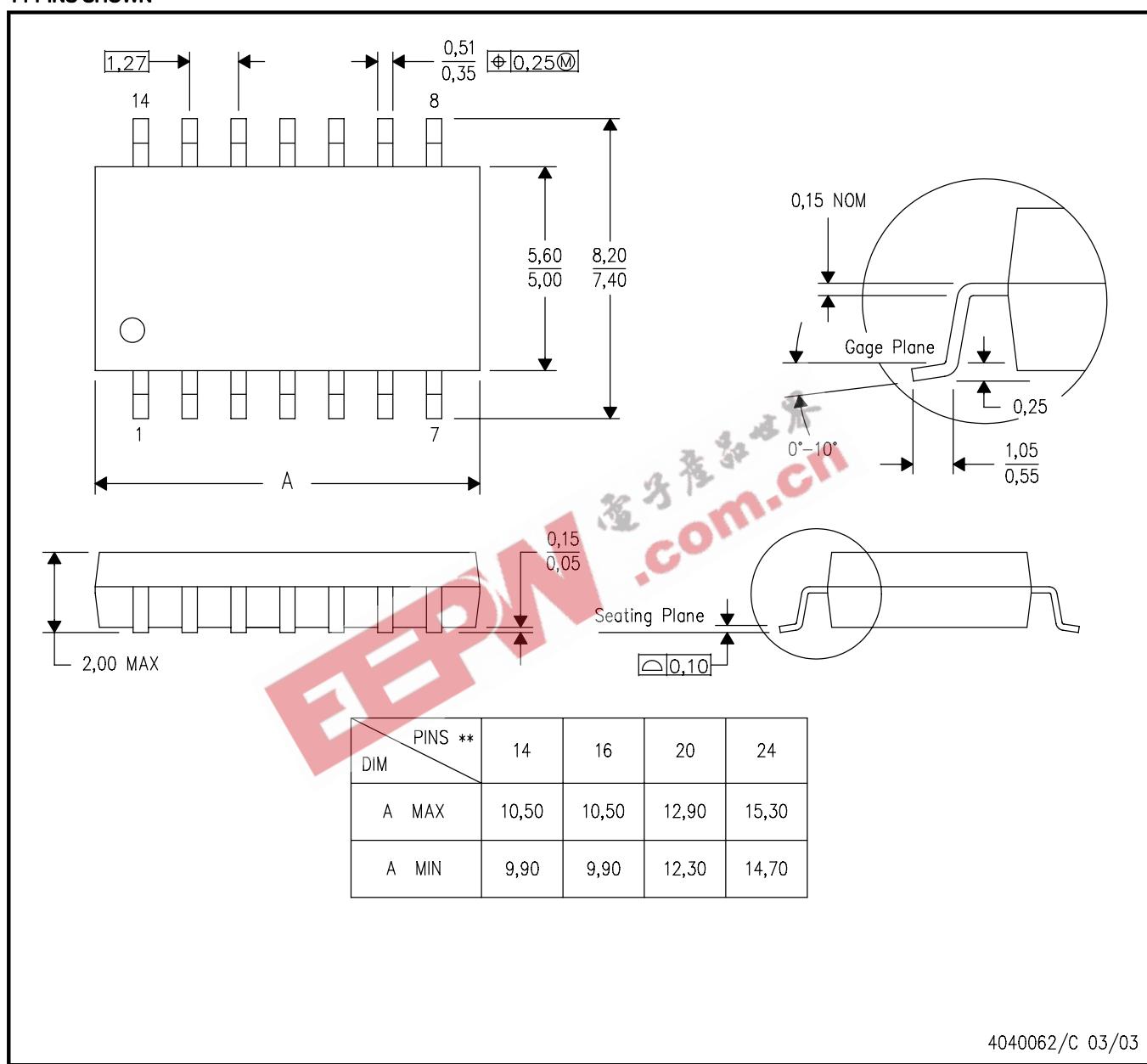
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN
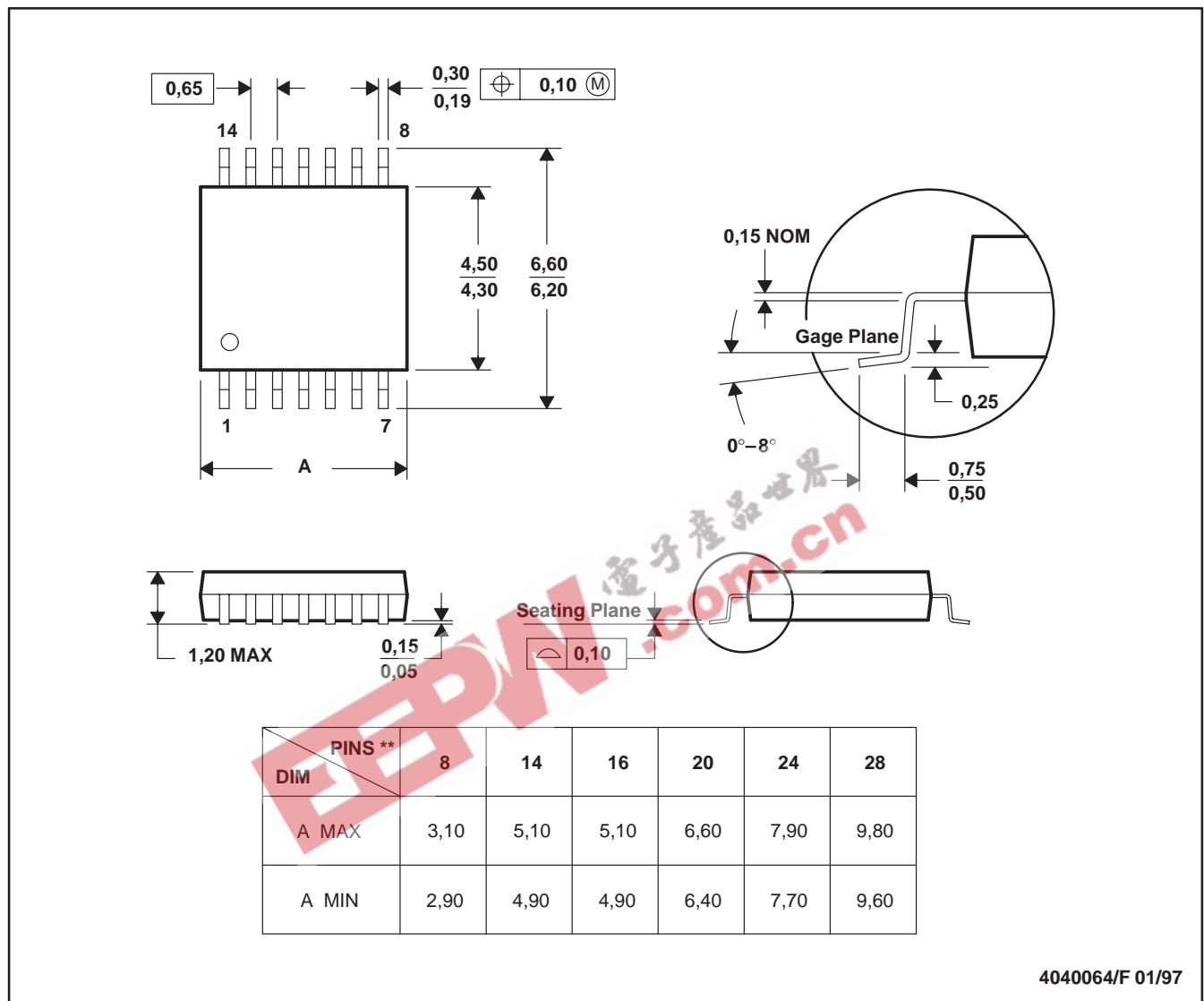
PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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