Data sheet acquired from Harris Semiconductor
SCHS272

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CD54/74FCT373, CD54/74FCT373AT, CD54/74FCT533

FCT Interface Logic
Octal Transparent Latch, Three-State

Features

- **CD54/74FCT373, CD54/74FCT373AT - Non-Inverting**
- **CD54/74FCT533 - Inverting**
- **Buffered inputs**
- **Typical Propagation Delay: 3.9ns at VCC = 5V, TA = +25°C, CL = 50pF (FCT373AT)**
- **SCR-Latchup-Resistant BiCMOS Process and Circuit Design**
- **FCTXXX Types - Speed of Bipolar FAST®/AS/S; FCTXXXAT Types - 30% Faster than FAST/AS/S with Significantly Reduced Power Consumption**
- **48mA to 32mA Output Sink Current (Commercial/ Extended Industrial)**
- **Output Voltage Swing Limited to 3.7V at VCC = 5V**
- **Controlled Output-Edge Rates**
- **Input/Output Isolation to VCC**
- **BiCMOS Technology with Low Quiescent Power**

Description

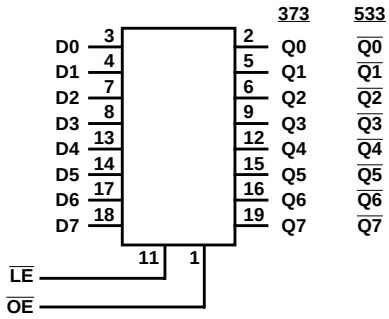
The CD54/74FCT373, 373AT, and 533 octal transparent latches use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32mA to 48mA.

The CD54/74FCT373, 373AT, and 533 outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54/74FCT373E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT373ATE	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT533E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT373M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT373ATM	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT533M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT373SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54/74FCT533SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54FCT373H	-55 to 125	
CD54FCT533H	-55 to 125	

Functional Diagram



TRUTH TABLE

$\overline{OE}$ OUTPUT ENABLE	$\overline{LE}$ LATCH ENABLE	DATA	373, 373AT OUTPUT	533 OUTPUT
L	H	H	H	L
L	H	L	L	H
L	L	l	L	H
L	L	h	H	L
H	X	X	Z	Z

H = HIGH voltage level.
L = LOW voltage level.
X = Irrelevant.
Z = HIGH Impedance.
l = LOW voltage level one setup time prior to the high-to-low latch enable transition.
h = HIGH voltage level one setup time prior to the high-to-low latch enable transition.

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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2230.2**

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