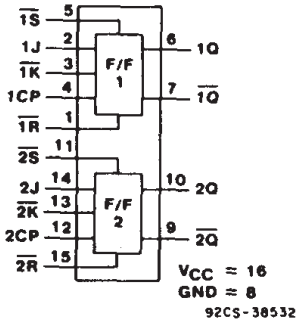
CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS282



CD54/74AC/ACT109 FUNCTIONAL DIAGRAM

Dual "J-K" Flip-Flop with Set and Reset

CD54/74AC/ACT109 - Positive-Edge-Triggered (J, $\overline{K}$)
CD54/74AC/ACT112 - Negative-Edge-Triggered (J, K)

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 4.8 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC109 and CD54/74AC112 and the CD54/74ACT109 and CD54/74ACT112 dual "J-K" flip-flops with set and reset use the RCA ADVANCED CMOS technology. These flip-flops have independent J, K (or $\overline{K}$), $\overline{Set}$, $\overline{Reset}$, and Clock inputs and Q and $\overline{Q}$ outputs. The CD54/74AC/ACT112 changes state on the negative-going transition of the clock pulse. The CD54/74AC/ACT109 changes state on the positive-going transition of the clock. Set and Reset are accomplished asynchronously by low-level inputs.

The CD74AC/ACT109 and CD74AC/ACT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT109 and CD54AC/ACT112, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

CD54/74AC/ACT109 TRUTH TABLE

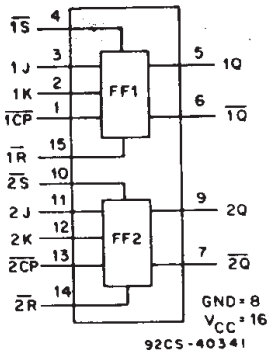
INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	NO CHANGE	
H	H	↓	H	H	H	L
H	H	L	X	X	NO CHANGE	

*Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously.

This data sheet is applicable to the CD54/74AC109, CD54AC112, CD45ACT109, and CD54ACT112. See SCHS233 for information on the CD74AC112, CD74ACT109, and CD74ACT112.

File Number **1967**

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112



CD54/74AC/ACT112 FUNCTIONAL DIAGRAM

CD54/74AC/ACT112 TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	NO CHANGE	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	NO CHANGE	

*Output states unpredictable if $\overline{S}$ and $\overline{R}$ go High simultaneously after both being Low at the same time.
H = High steady state
L = Low steady state
X = Irrelevant

↓ = High-to-Low transition

↑ = Low-to-High transition

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage V_{IL}			1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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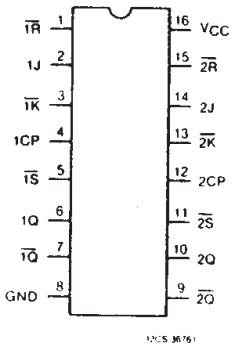
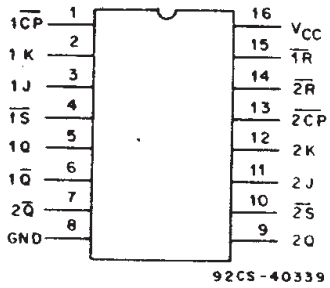
TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT109



CD54/74AC/ACT112

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.10	—	0.10	—	0.10	V
		24	4.5	—	0.36	—	0.44	—	0.50	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	109	112
J, CP, $\overline{CP}$	1	1
K	—	0.53
$\overline{K}$	0.53	—
$\overline{S}$, $\overline{R}$	0.58	0.58

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum CP, ($\overline{CP}$) Frequency							
109	f_{max}	1.5	9	—	8	—	MHz
		3.3*	81	—	71	—	
		5†	114	—	100	—	
112	f_{max}	1.5	9	—	8	—	MHz
		3.3	81	—	71	—	
		5	114	—	100	—	
CP, ($\overline{CP}$) Pulse Width	t_w	1.5	55	—	63	—	ns
		3.3	6	—	7	—	
		5	4.4	—	5	—	
$\overline{R}$, $\overline{S}$ Pulse Width	t_w	1.5	49	—	56	—	ns
		3.3	5.5	—	6.3	—	
		5	3.9	—	4.5	—	
Setup Time							
J, $\overline{K}$ to CP	t_{su}	1.5	61	—	69	—	ns
109		3.3	6.8	—	7.7	—	
		5	4.8	—	5.5	—	
J, K to $\overline{CP}$	t_{su}	1.5	44	—	50	—	ns
112		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
Hold Time							
J, $\overline{K}$ to CP	t_H	1.5	0	—	0	—	ns
109		3.3	0	—	0	—	
		5	0	—	0	—	
J, K to $\overline{CP}$	t_H	1.5	0	—	0	—	ns
112		3.3	0	—	0	—	
		5	0	—	0	—	
Removal Time							
$\overline{R}$, S to CP, ($\overline{CP}$)	t_{REM}	1.5	27	—	31	—	ns
		3.1	3.1	—	3.5	—	
		5	2.2	—	2.5	—	

*3.3 V: min. is @ 3 V
†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
CP, ($\overline{CP}$) to Q, $\overline{Q}$	t_{PLH}	1.5	—	117	—	129	ns
	t_{PHL}	3.3*	3.7	13.1	3.6	14.4	
		5†	2.7	9.4	2.6	10.3	
$\overline{S}$, R to Q, $\overline{Q}$	t_{PLH}	1.5	—	139	—	153	ns
	t_{PHL}	3.3	4.4	15.5	4.3	17.1	
		5	3.2	11.1	3.1	12.2	
Power Dissipation Capacitance	C_{PD}§	—	56 Typ.		56 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

† 5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum CP, ($\overline{CP}$) Frequency 109	f_{max}	5*	114	—	100	—	MHz
112			114	—	100	—	
CP, ($\overline{CP}$) Pulse Width	t_W	5	4.4	—	5	—	ns
R, $\overline{S}$ Pulse Width	t_W	5	4.8	—	5.5	—	ns
Setup Time J, $\overline{K}$ to CP (109)	t_{SU}	5	4.8	—	5.5	—	ns
J, K to $\overline{CP}$ (112)			3.5	—	4	—	
Hold Time J, $\overline{K}$ to CP (109)	t_H	5	0	—	0	—	ns
J, K to $\overline{CP}$ (112)			1	—	1	—	
Removal Time $\overline{R}$, $\overline{S}$ to CP, ($\overline{CP}$)	t_{REM}	5	2.2	—	2.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

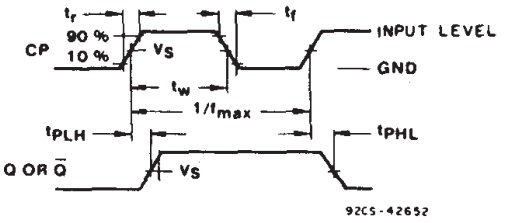
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays CP, ($\overline{CP}$) to Q, $\overline{Q}$	t_{PLH} t_{PHL}	5*	2.7	9.4	2.6	10.3	ns
$\overline{S}$, $\overline{R}$, to Q, $\overline{Q}$	t_{PLH} t_{PHL}	5	3.2	11.1	3.1	12.2	ns
Power Dissipation Capacitance	C_{PD}§	—	56 Typ.		56 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

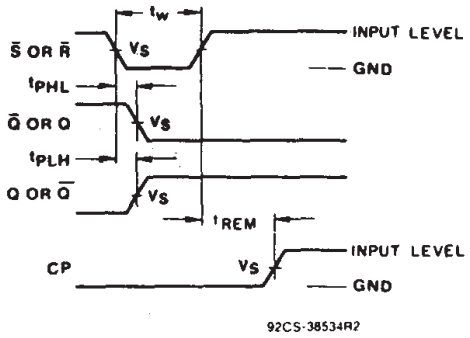
§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

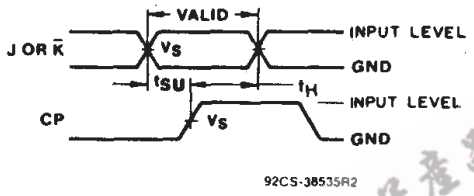
CD54/74AC/ACT109 Waveforms



Clock to output delays and clock pulse width.

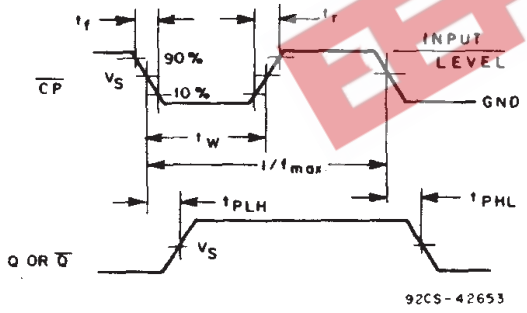


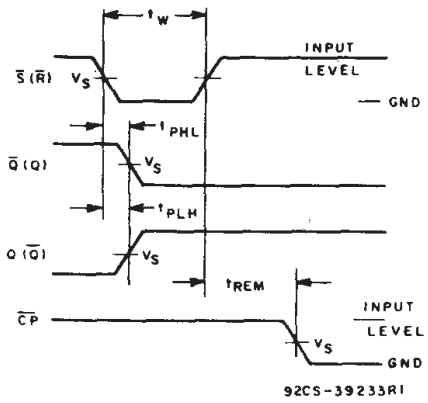
$\overline{Reset}$ or $\overline{Set}$ prerequisite and propagation delays.

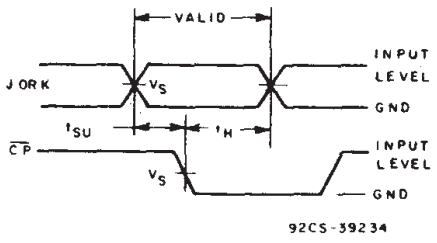


Data setup and hold times.

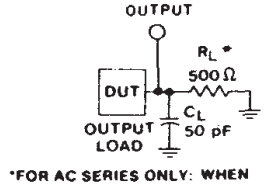
CD54/74/AC/ACT112 Waveforms







Propagation delay times, and setup and hold times.



Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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