FAIRCHILD SEMICONDUCTOR™

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# CD4013BC
# Dual D-Type Flip-Flop

## General Description

The CD4013B dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

## Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 $V_{DD}$ (typ.)
- Low power TTL: fan out of 2 driving 74L
  compatibility: or 1 driving 74LS

## Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

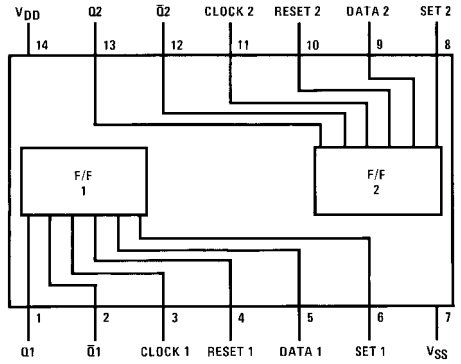
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| CD4013BCM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow |
| CD4013BCSJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| CD4013BCN | N14A | 14-Lead Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram

**Pin Assignments for DIP, SOIC and SOP**




**Top View**

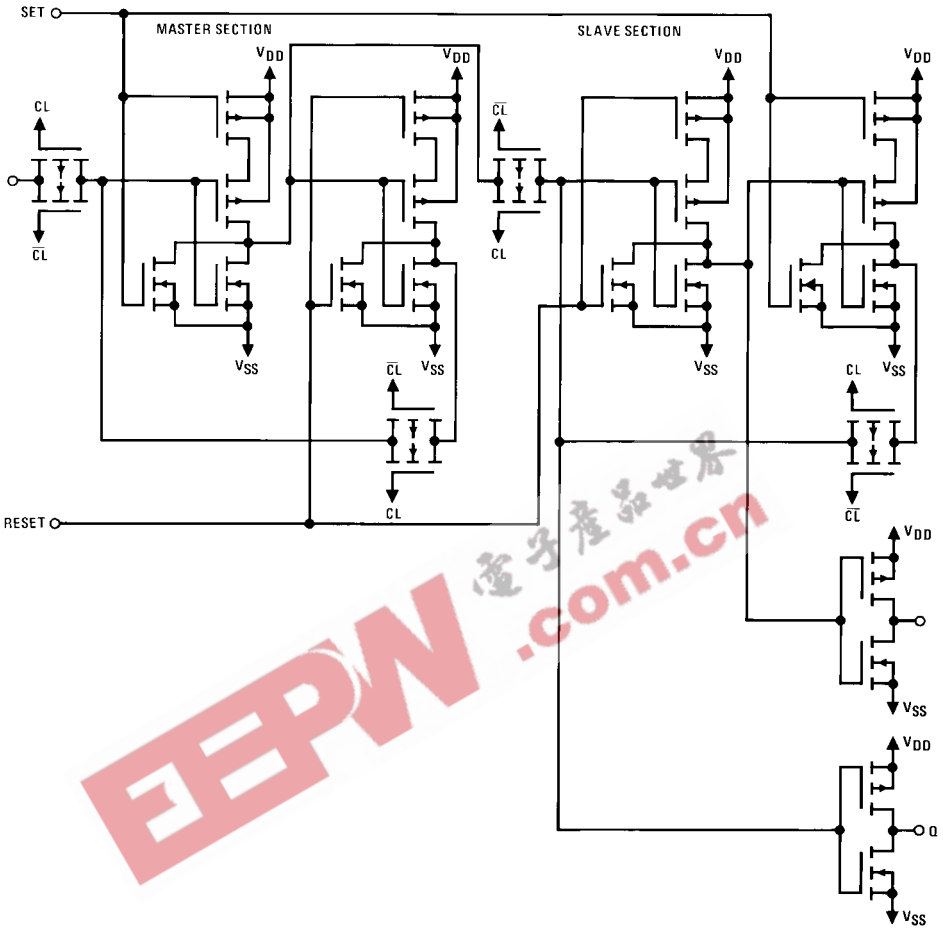
## Truth Table

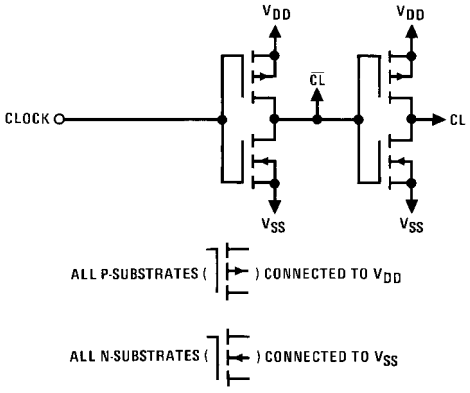
| CL (Note 1) | D | R | S | Q | $\overline{Q}$ |
|---|---|---|---|---|---|
| ↗ | 0 | 0 | 0 | 0 | 1 |
| ↗ | 1 | 0 | 0 | 1 | 0 |
| ↘ | x | 0 | 0 | Q | $\overline{Q}$ |
| x | x | 1 | 0 | 0 | 1 |
| x | x | 0 | 1 | 1 | 0 |
| x | x | 1 | 1 | 1 | 1 |

No Change
x = Don't Care Case
**Note 1:** Level Change

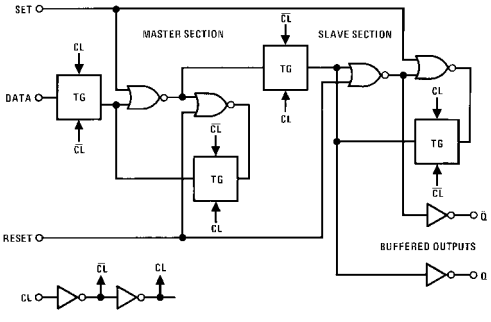
 

## Schematic Diagrams




## Logic Diagram



## Absolute Maximum Ratings (Note 2)

(Note 3)

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | −0.5 $V_{DC}$ to +18 $V_{DC}$ |
| Input Voltage ($V_{IN}$) | −0.5 $V_{DC}$ to $V_{DD}$ +0.5 $V_{DC}$ |
| Storage Temperature Range ($T_S$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |

## Recommended Operating Conditions (Note 3)

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | +3 $V_{DC}$ to +15 $V_{DC}$ |
| Input Voltage ($V_{IN}$) | 0 $V_{DC}$ to $V_{DD}$ $V_{DC}$ |
| Operating Temperature Range ($T_A$) | −40°C to +85°C |

**Note 2:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 3:** $V_{SS}$ = 0V unless otherwise specified.

## DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | −40°C | | +25°C | | | +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device | $V_{DD}$ = 5V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 4.0 | | | 4.0 | | 30 | µA |
| | Current | $V_{DD}$ = 10V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 8.0 | | | 8.0 | | 60 | µA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 16.0 | | | 16.0 | | 120 | µA |
| $V_{OL}$ | LOW Level | $\|I_O\|$ < 1.0 µA | | | | | | | | |
| | Output Voltage | $V_{DD}$ = 5V | | 0.05 | | | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 10V | | 0.05 | | | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 15V | | 0.05 | | | 0.05 | | 0.05 | V |
| $V_{OH}$ | HIGH Level | $\|I_O\|$ < 1.0 µA | | | | | | | | |
| | Output Voltage | $V_{DD}$ = 5V | 4.95 | | 4.95 | | | 4.95 | | V |
| | | $V_{DD}$ = 10V | 9.95 | | 9.95 | | | 9.95 | | V |
| | | $V_{DD}$ = 15V | 14.95 | | 14.95 | | | 14.95 | | V |
| $V_{IL}$ | LOW Level | $\|I_O\|$ < 1.0 µA | | | | | | | | |
| | Input Voltage | $V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V | | 1.5 | | | 1.5 | | 1.5 | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1.0V or 9.0V | | 3.0 | | | 3.0 | | 3.0 | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V | | 4.0 | | | 4.0 | | 4.0 | V |
| $V_{IH}$ | HIGH Level | $\|I_O\|$ < 1.0 µA | | | | | | | | |
| | Input Voltage | $V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V | 3.5 | | 3.5 | | | 3.5 | | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1.0V or 9.0V | 7.0 | | 7.0 | | | 7.0 | | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V | 11.0 | | 11.0 | | | 11.0 | | V |
| $I_{OL}$ | LOW Level Output | $V_{DD}$ = 5V, $V_O$ = 0.4V | 0.52 | | 0.44 | 0.88 | | 0.36 | | mA |
| | Current (Note 4) | $V_{DD}$ = 10V, $V_O$ = 0.5V | 1.3 | | 1.1 | 2.25 | | 0.9 | | mA |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 3.6 | | 3.0 | 8.8 | | 2.4 | | mA |
| $I_{OH}$ | HIGH Level Output | $V_{DD}$ = 5V, $V_O$ = 4.6V | −0.52 | | −0.44 | −0.88 | | −0.36 | | mA |
| | Current (Note 4) | $V_{DD}$ = 10V, $V_O$ = 9.5V | −1.3 | | −1.1 | −2.25 | | −0.9 | | mA |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | −3.6 | | −3.0 | −8.8 | | −2.4 | | mA |
| $I_{IN}$ | Input Current | $V_{DD}$ = 15V, $V_{IN}$ = 0V | | −0.3 | | $-10^{-5}$ | −0.3 | | −1.0 | µA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = 15V | | 0.3 | | $10^{-5}$ | 0.3 | | 1.0 | µA |

**Note 4:** $I_{OH}$ and $I_{OL}$ are measured one output at a time.

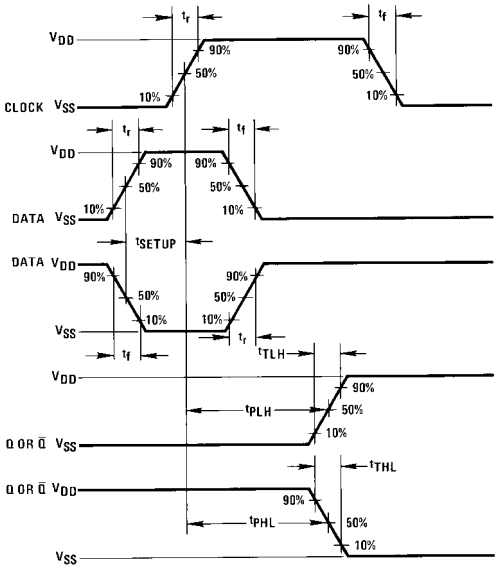
## AC Electrical Characteristics (Note 5)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, unless otherwise noted

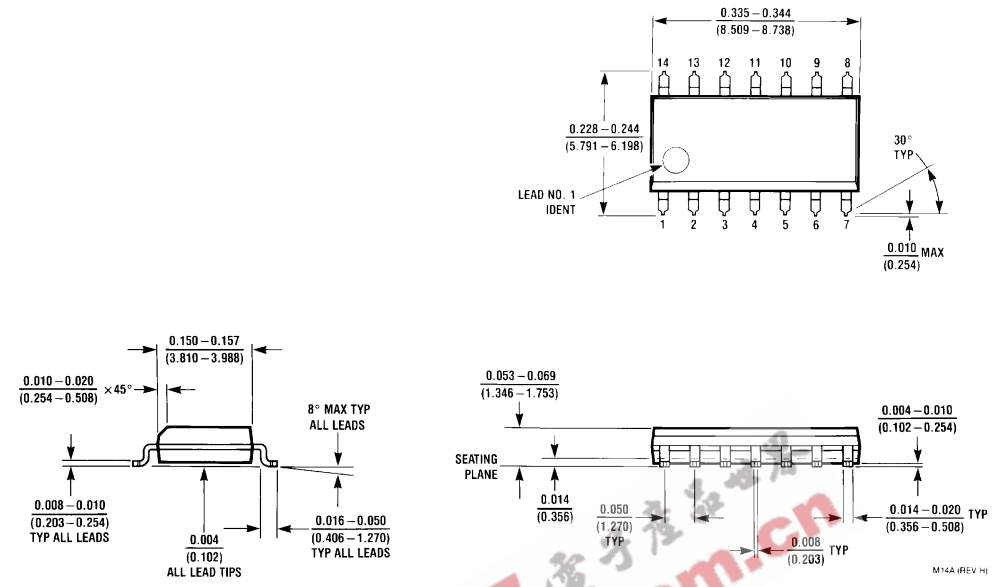
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CLOCK OPERATION** | | | | | | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time | $V_{DD}$ = 5V | | 200 | 350 | ns |
| | | $V_{DD}$ = 10V | | 80 | 160 | ns |
| | | $V_{DD}$ = 15V | | 65 | 120 | ns |
| $t_{THL}$, $t_{TLH}$ | Transition Time | $V_{DD}$ = 5V | | 100 | 200 | ns |
| | | $V_{DD}$ = 10V | | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | | 40 | 80 | ns |
| $t_{WL}$, $t_{WH}$ | Minimum Clock | $V_{DD}$ = 5V | | 100 | 200 | ns |
| | Pulse Width | $V_{DD}$ = 10V | | 40 | 80 | ns |
| | | $V_{DD}$ = 15V | | 32 | 65 | ns |
| $t_{RCL}$, $t_{FCL}$ | Maximum Clock Rise and | $V_{DD}$ = 5V | | | 15 | µs |
| | Fall Time | $V_{DD}$ = 10V | | | 10 | µs |
| | | $V_{DD}$ = 15V | | | 5 | µs |
| $t_{SU}$ | Minimum Set-Up Time | $V_{DD}$ = 5V | | 20 | 40 | ns |
| | | $V_{DD}$ = 10V | | 15 | 30 | ns |
| | | $V_{DD}$ = 15V | | 12 | 25 | ns |
| $f_{CL}$ | Maximum Clock | $V_{DD}$ = 5V | 2.5 | 5 | | MHz |
| | Frequency | $V_{DD}$ = 10V | 6.2 | 12.5 | | MHz |
| | | $V_{DD}$ = 15V | 7.6 | 15.5 | | MHz |
| **SET AND RESET OPERATION** | | | | | | |
| $t_{PHL(R)}$, | Propagation Delay Time | $V_{DD}$ = 5V | | 150 | 300 | ns |
| $t_{PLH(S)}$ | | $V_{DD}$ = 10V | | 65 | 130 | ns |
| | | $V_{DD}$ = 15V | | 45 | 90 | ns |
| $t_{WH(R)}$, | Minimum Set and | $V_{DD}$ = 5V | | 90 | 180 | ns |
| $t_{WH(S)}$ | Reset Pulse Width | $V_{DD}$ = 10V | | 40 | 80 | ns |
| | | $V_{DD}$ = 15V | | 25 | 50 | ns |
| $C_{IN}$ | Average Input Capacitance | Any Input | | 5 | 7.5 | pF |

**Note 5:** AC Parameters are guaranteed by DC correlated testing.

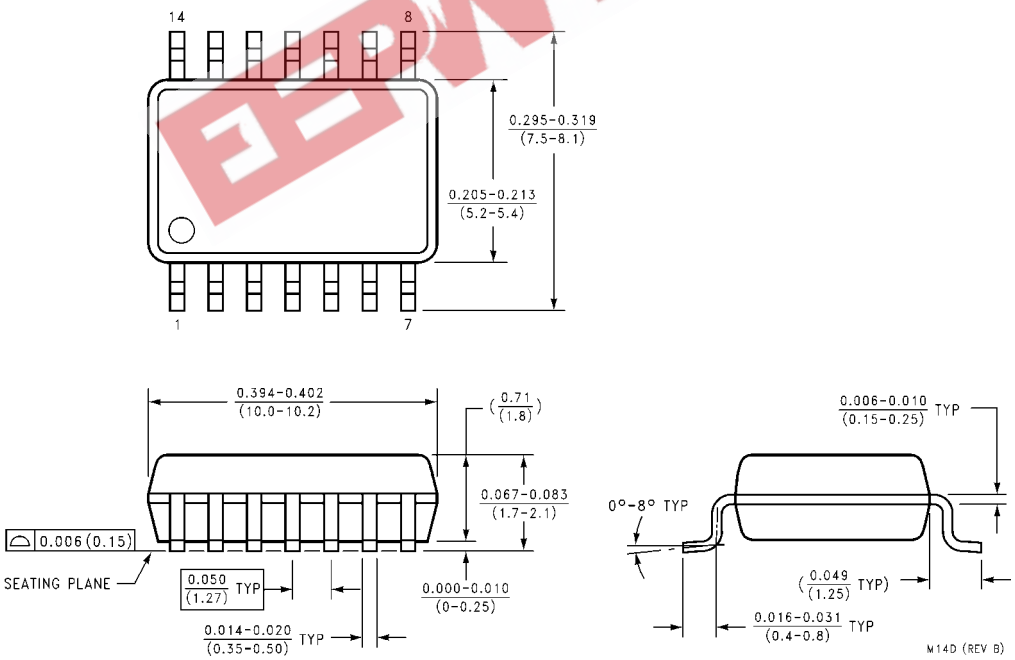
## Switching Time Waveforms



## Physical Dimensions inches (millimeters) unless otherwise noted

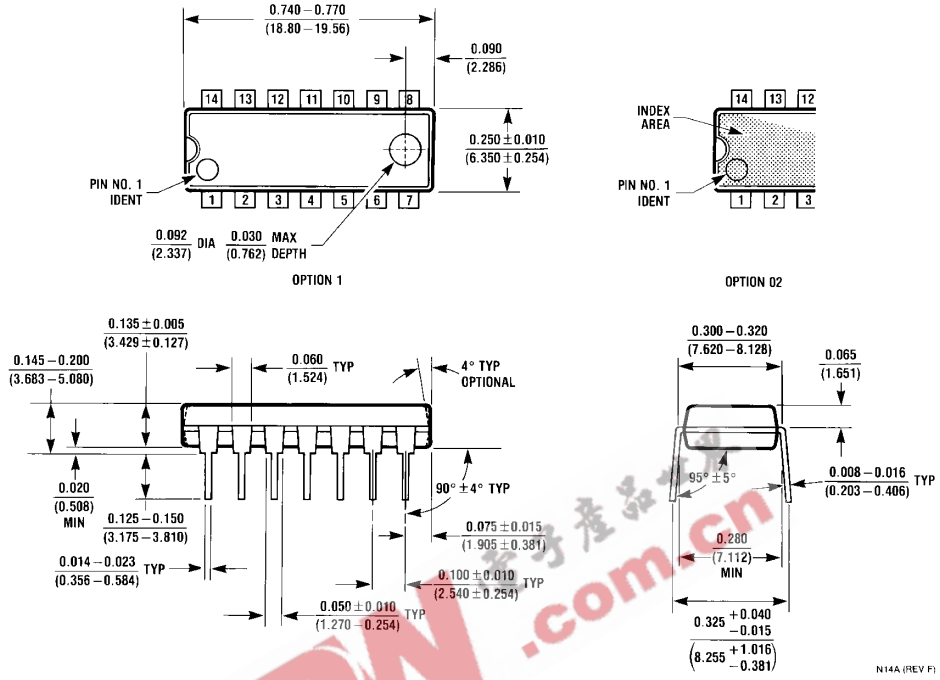



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow**
**Package Number M14A**




**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N14A**



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