

# CD40192B, CD40193B Types

## CMOS Presetable Up/Down Counters (Dual Clock With Reset)

High-Voltage Types (20-Volt Rating)  
CD40192 – BCD Type  
CD40193 – Binary Type

■ CD40192B Presetable BCD Up/Down Counter and the CD40193B Presetable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a PRESET ENABLE control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as CARRY and BORROW outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET ENABLE control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The CARRY and BORROW signals are high when the counter is counting up or down. The CARRY signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The BORROW signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the BORROW and CARRY outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

The CD40192B and CD40193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

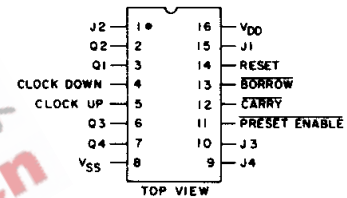
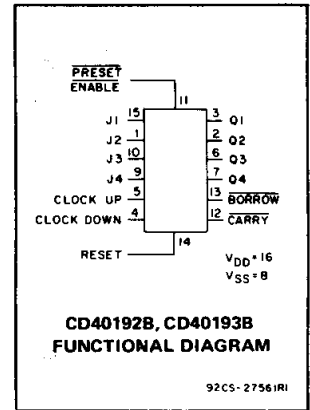
### Features:

- Individual clock lines for counting up or counting down
- Synchronous high-speed carry and borrow propagation delays for cascading
- Asynchronous reset and preset capability
- Medium-speed operation— $f_{CL} = 8 \text{ MHz (typ.) @ } 10 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package temperature range;  $100 \text{ nA}$  at 18 V and  $25^\circ\text{C}$
- Noise margin over full package temperature range:  
1 V at  $V_{DD} = 5 \text{ V}$     2 V at  $V_{DD} = 10 \text{ V}$   
2.5 V at  $V_{DD} = 15 \text{ V}$

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Up/down difference counting
- Multistage ripple counting
- Synchronous frequency dividers
- A/D and D/A conversion
- Programmable binary or BCD counting



CD40192B, CD40193B  
TERMINAL ASSIGNMENT

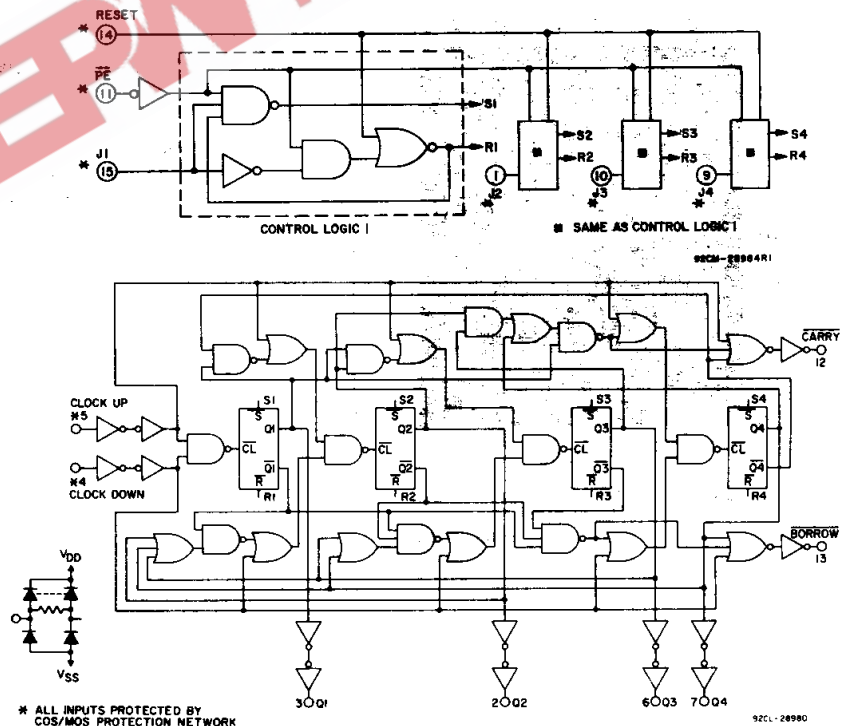


Fig. 1 – CD40192B logic diagram (BCD).

# CD40192B, CD40193B Types

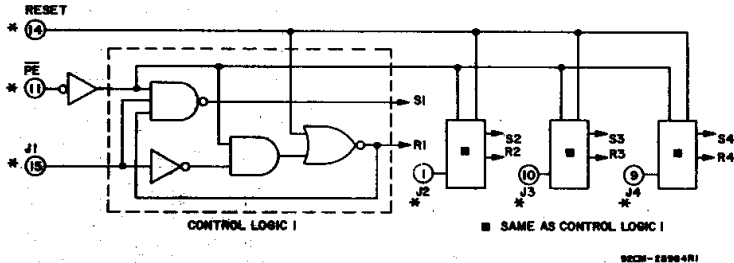


Fig. 2 - CD40193B logic diagram (binary).

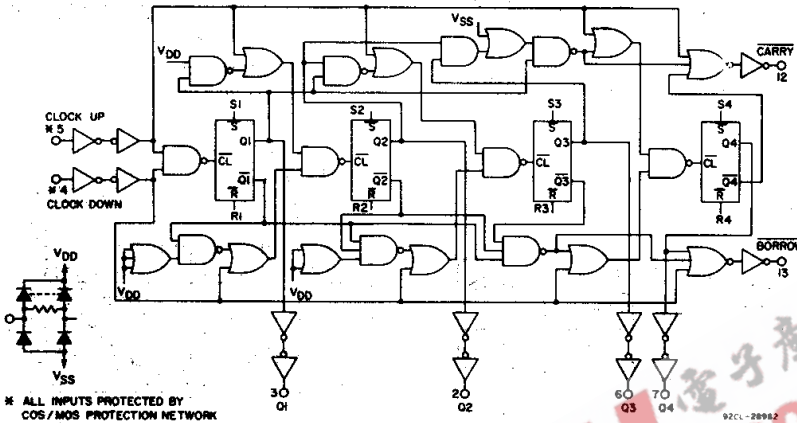


Fig. 4 - Internal logic of Flip-flop.

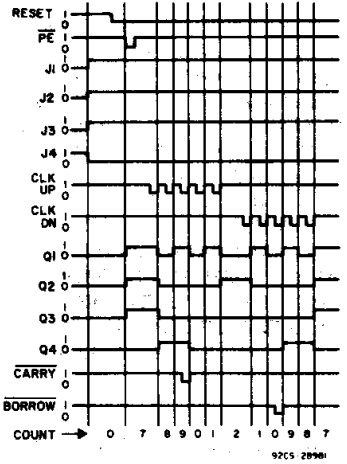
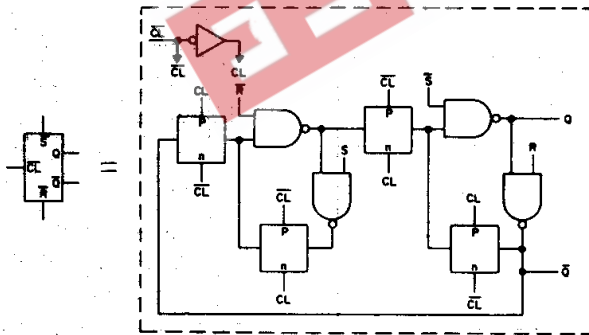


Fig. 3 - CD40192B timing diagram.

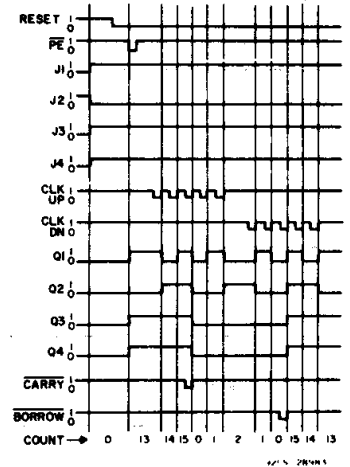


Fig. 5 - CD40193B timing diagram.

Fig. 6 - Typical output low (sink) current characteristics.

### TRUTH TABLE

| CLOCK UP | CLOCK DOWN | PRESET ENABLE | RESET | ACTION     |
|----------|------------|---------------|-------|------------|
|          | 1          | 1             | 0     | COUNT UP   |
|          | 1          | 1             | 0     | NO COUNT   |
| 1        |            | 1             | 0     | COUNT DOWN |
| 1        |            | 1             | 0     | NO COUNT   |
| X        | X          | 0             | 0     | PRESET     |
| X        | X          | X             | 1     | RESET      |

1 = HIGH LEVEL

0 = LOW LEVEL

X = DON'T CARE

## CD40192B, CD40193B Types

### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |  |
|---|--|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )<br>Voltages referenced to $V_{SS}$ Terminal)  | -0.5V to +20V  |
| INPUT VOLTAGE RANGE, ALL INPUTS   | -0.5V to $V_{DD} + 0.5V$   |
| DC INPUT CURRENT, ANY ONE INPUT   | $\pm 10\text{mA}$  |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):  |  |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$                               | 500mW  |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$                              | Derate Linearity at $12\text{mW}/^\circ\text{C}$ to $200\text{mW}$ |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR  |  |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$               | 100mW  |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )   | $-55^\circ\text{C}$ to $+125^\circ\text{C}$                        |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )   | $-65^\circ\text{C}$ to $+150^\circ\text{C}$                        |
| LEAD TEMPERATURE (DURING SOLDERING):  |  |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max | $+265^\circ\text{C}$   |

### RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$ (unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC  | $V_{DD}$<br>(V) | LIMITS |      | UNITS         |
|---|-----------------|--------|------|---------------|
|   |                 | Min.   | Max. |               |
| Supply Voltage Range (For $T_A = \text{Full Temp. Range}$ ) | -               | 3      | 18   | V             |
| Removal Time:<br>RESET or $\overline{PE}$                   | 5               | 80     | -    | ns            |
|   | 10              | 40     | -    |               |
|   | 15              | 30     | -    |               |
| Pulse Width:<br>RESET                                       | 5               | 480    | -    | ns            |
|   | 10              | 300    | -    |               |
|   | 15              | 260    | -    |               |
| $\overline{PE}$   | 5               | 240    | -    | ns            |
|   | 10              | 170    | -    |               |
|   | 15              | 140    | -    |               |
| CLOCK   | 5               | 180    | -    | ns            |
|   | 10              | 90     | -    |               |
|   | 15              | 60     | -    |               |
| Clock Input Frequency                                       | 5               | -      | 2    | MHz           |
|   | 10              | DC     | 4    |               |
|   | 15              | -      | 5.5  |               |
| Clock Rise & Fall Time                                      | 5               | -      | 15   | $\mu\text{s}$ |
|   | 10              | -      | 15   |               |
|   | 15              | -      | 5    |               |

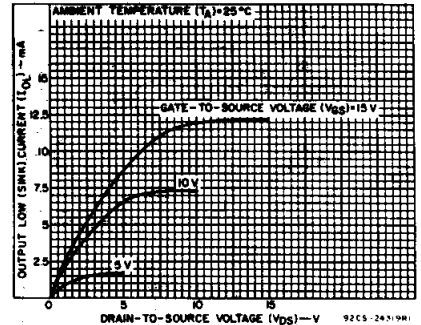


Fig. 7 — Minimum output low (sink) current characteristics.

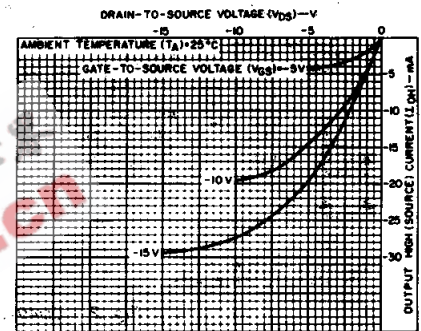


Fig. 8 — Typical output high (source) current characteristics.

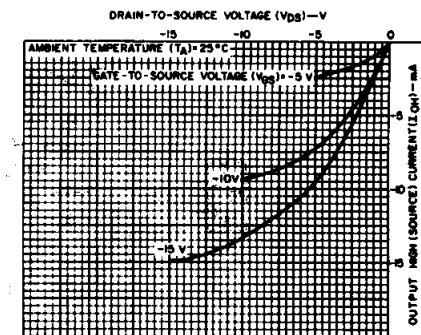


Fig. 9 — Minimum output high (source) current characteristics.

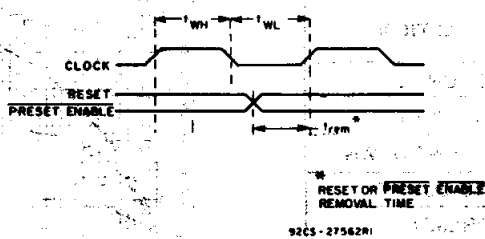


Fig. 10 — Timing diagram defining  $t_{ren}$

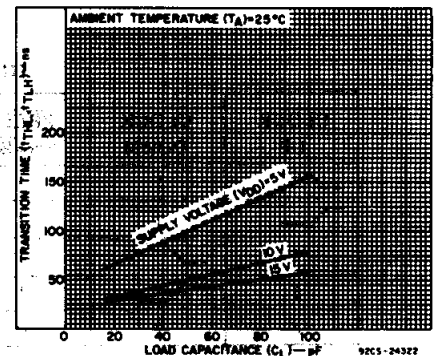


Fig. 11 — Typical transition time as a function of load capacitance.

## CD40192B, CD40193B Types

### STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                     | CONDITIONS         |                     |                     | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|  | V <sub>O</sub> (V) | V <sub>IN</sub> (V) | V <sub>DD</sub> (V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|  |                    |                     |                     |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent Device Current, I <sub>DD</sub> Max.     | -                  | 0,5                 | 5                   | 5                                     | 5     | 150   | 150   | -     | 0,04              | 5    | μA    |
|  | -                  | 0,10                | 10                  | 10                                    | 10    | 300   | 300   | -     | 0,04              | 10   |       |
|  | -                  | 0,15                | 15                  | 20                                    | 20    | 600   | 600   | -     | 0,04              | 20   |       |
|  | -                  | 0,20                | 20                  | 100                                   | 100   | 3000  | 3000  | -     | 0,08              | 100  |       |
| Output Low (Sink) Current I <sub>OL</sub> Min.     | 0,4                | 0,5                 | 5                   | 0,64                                  | 0,61  | 0,42  | 0,36  | 0,51  | 1                 | -    | mA    |
|  | 0,5                | 0,10                | 10                  | 1,6                                   | 1,5   | 1,1   | 0,9   | 1,3   | 2,6               | -    |       |
|  | 1,5                | 0,15                | 15                  | 4,2                                   | 4     | 2,8   | 2,4   | 3,4   | 6,8               | -    |       |
| Output High (Source) Current, I <sub>OH</sub> Min. | 4,6                | 0,5                 | 5                   | -0,64                                 | -0,61 | -0,42 | -0,36 | -0,51 | -1                | -    | mA    |
|  | 2,5                | 0,5                 | 5                   | -2                                    | -1,8  | -1,3  | -1,15 | -1,6  | -3,2              | -    |       |
|  | 9,5                | 0,10                | 10                  | -1,6                                  | -1,5  | -1,1  | -0,9  | -1,3  | -2,6              | -    |       |
|  | 13,5               | 0,15                | 15                  | -4,2                                  | -4    | -2,8  | -2,4  | -3,4  | -6,8              | -    |       |
| Output Voltage: Low-Level, V <sub>OL</sub> Max.    | -                  | 0,5                 | 5                   | 0,05                                  |       |       |       | -     | 0                 | 0,05 | V     |
|  | -                  | 0,10                | 10                  | 0,05                                  |       |       |       | -     | 0                 | 0,05 |       |
|  | -                  | 0,15                | 15                  | 0,05                                  |       |       |       | -     | 0                 | 0,05 |       |
| Output Voltage: High-Level, V <sub>OH</sub> Min.   | -                  | 0,5                 | 5                   | 4,95                                  |       |       |       | 4,95  | 5                 | -    | V     |
|  | -                  | 0,10                | 10                  | 9,95                                  |       |       |       | 9,95  | 10                | -    |       |
|  | -                  | 0,15                | 15                  | 14,95                                 |       |       |       | 14,95 | 15                | -    |       |
| Input Low Voltage, V <sub>IL</sub> Max.            | 0,5, 4,5           | -                   | 5                   | 1,5                                   |       |       |       | -     | -                 | 1,5  | V     |
|  | 1,9                | -                   | 10                  | 3                                     |       |       |       | -     | -                 | 3    |       |
|  | 1,5, 13,5          | -                   | 15                  | 4                                     |       |       |       | -     | -                 | 4    |       |
| Input High Voltage, V <sub>IH</sub> Min.           | 0,5, 4,5           | -                   | 5                   | 3,5                                   |       |       |       | 3,5   | -                 | -    | V     |
|  | 1,9                | -                   | 10                  | 7                                     |       |       |       | 7     | -                 | -    |       |
|  | 1,5, 13,5          | -                   | 15                  | 11                                    |       |       |       | 11    | -                 | -    |       |
| Input Current I <sub>IN</sub> Max.                 | -                  | 0,18                | 18                  | ±0,1                                  | ±0,1  | ±1    | ±1    | -     | ±10 <sup>-5</sup> | ±0,1 | μA    |

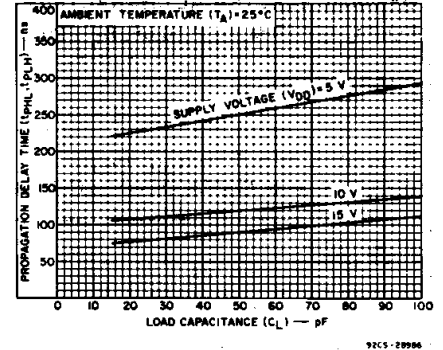


Fig. 12 - Typical propagation delay time as a function of load capacitance.

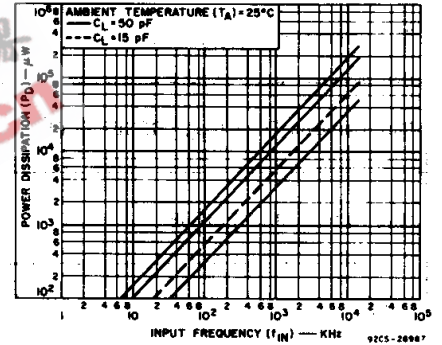
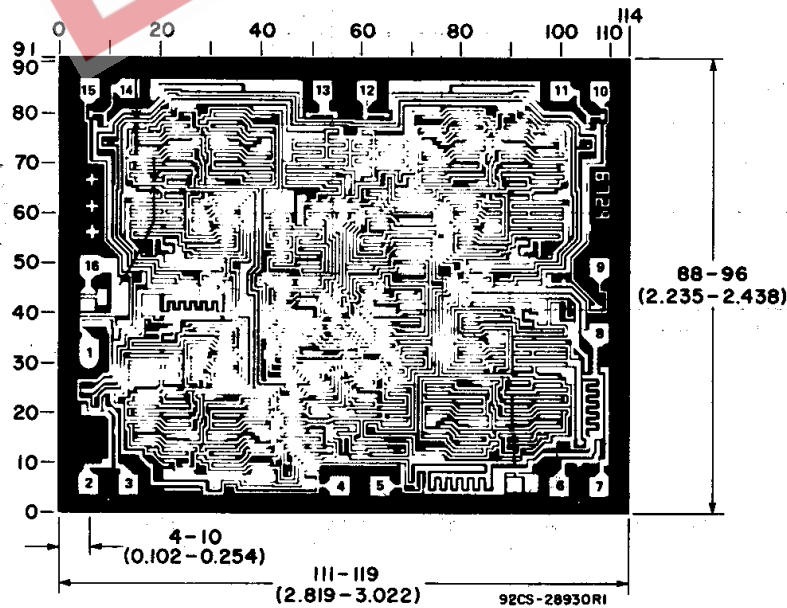


Fig. 13 - Dynamic power dissipation.



Dimensions and pad layout for the CD40192BH (dimensions and pad layout for the CD40193BH are identical).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).

COMMERCIAL CMOS HIGH VOLTAGE ICs

## CD40192B, CD40193B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$

Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

| CHARACTERISTIC   | $V_{DD}$<br>(V) | LIMITS |      |      | UNITS         |
|--|-----------------|--------|------|------|---------------|
|  |                 | Min.   | Typ. | Max. |               |
| Propagation Delay Time $t_{pHL}, t_{pLH}$ :<br>CLOCK UP or CLOCK DOWN to Q, RESET to Q                         | 5               | —      | 250  | 500  | ns            |
|  | 10              | —      | 120  | 240  |               |
|  | 15              | —      | 90   | 180  |               |
| $\overline{\text{PE}}$ to Q  | 5               | —      | 200  | 400  | ns            |
|  | 10              | —      | 100  | 200  |               |
|  | 15              | —      | 70   | 140  |               |
| CLOCK UP to $\overline{\text{CARRY}}$ , CLOCK DOWN to $\overline{\text{BORROW}}$                               | 5               | —      | 160  | 320  | ns            |
|  | 10              | —      | 80   | 160  |               |
|  | 15              | —      | 60   | 120  |               |
| $\overline{\text{RESET}}$ or $\overline{\text{PE}}$ to $\overline{\text{BORROW}}$ or $\overline{\text{CARRY}}$ | 5               | —      | 300  | 600  | ns            |
|  | 10              | —      | 150  | 300  |               |
|  | 15              | —      | 110  | 220  |               |
| Transition Time, $t_{THL}, t_{TLH}$  | 5               | —      | 100  | 200  | ns            |
|  | 10              | —      | 50   | 100  |               |
|  | 15              | —      | 40   | 80   |               |
| Min. Removal Time, $t_{rem}$ * RESET or $\overline{\text{PE}}$   | 5               | —      | 40   | 80   | ns            |
|  | 10              | —      | 20   | 40   |               |
|  | 15              | —      | 15   | 30   |               |
| Min. Pulse Width, $t_w$ RESET  | 5               | —      | 240  | 480  | ns            |
|  | 10              | —      | 150  | 300  |               |
|  | 15              | —      | 130  | 260  |               |
| $\overline{\text{PE}}$   | 5               | —      | 120  | 240  | ns            |
|  | 10              | —      | 85   | 170  |               |
|  | 15              | —      | 70   | 140  |               |
| CLOCK  | 5               | —      | 90   | 180  | ns            |
|  | 10              | —      | 45   | 90   |               |
|  | 15              | —      | 30   | 60   |               |
| Max. Clock Input Frequency, $f_{CL}$   | 5               | 2      | 4    | —    | MHz           |
|  | 10              | 4      | 8    | —    |               |
|  | 15              | 5.5    | 11   | —    |               |
| Clock Rise & Fall Time, $t_r, t_f$   | 5               | —      | —    | 15   | $\mu\text{s}$ |
|  | 10              | —      | —    | 15   |               |
|  | 15              | —      | —    | 5    |               |
| Input Capacitance, $C_{IN}$ :<br>RESET   | —               | —      | 10   | 15   | pF            |
|  | —               | —      | 5    | 7.5  |               |
| All Other Inputs   | —               | —      | 5    | 7.5  | pF            |

\* The time required for RESET or PRESET ENABLE control to be removed before clocking (see timing diagram, Fig. 10).

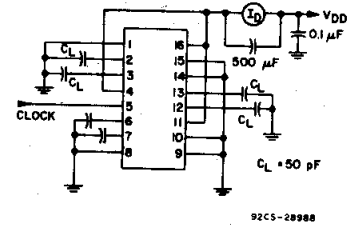


Fig. 14 — Dynamic power dissipation test circuit.

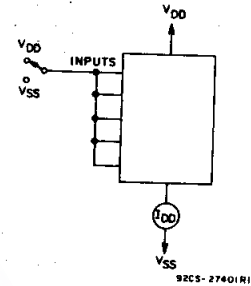


Fig. 15 — Quiescent device current test circuit.

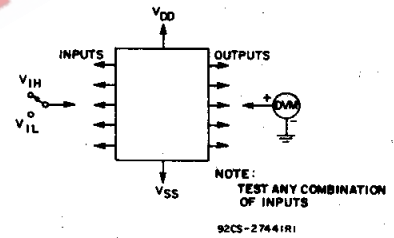


Fig. 16 — Input voltage test circuit.

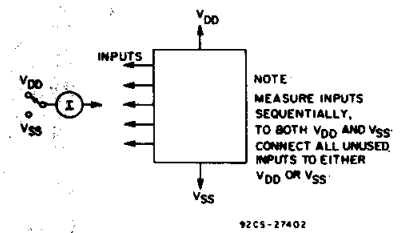


Fig. 17 — Input current test circuit.

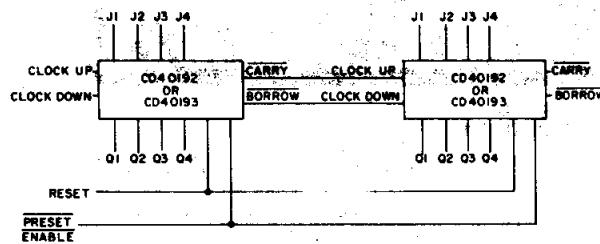


Fig. 18 — Cascaded counter packages.

PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup>               |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| CD40192BE        | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC                             |
| CD40192BF        | ACTIVE                | CDIP         | J               | 16   | 1           | None                    | Call TI          | Level-NC-NC-NC                             |
| CD40192BF3A      | ACTIVE                | CDIP         | J               | 16   | 1           | None                    | Call TI          | Level-NC-NC-NC                             |
| CD40192BNSR      | ACTIVE                | SO           | NS              | 16   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| CD40192BPW       | ACTIVE                | TSSOP        | PW              | 16   | 90          | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM                         |
| CD40192BPWR      | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM                         |
| CD40193BE        | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC                             |
| CD40193BF3A      | ACTIVE                | CDIP         | J               | 16   | 1           | None                    | Call TI          | Level-NC-NC-NC                             |
| CD40193BNSR      | ACTIVE                | SO           | NS              | 16   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| CD40193BPW       | ACTIVE                | TSSOP        | PW              | 16   | 90          | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM                         |
| CD40193BPWR      | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM                         |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

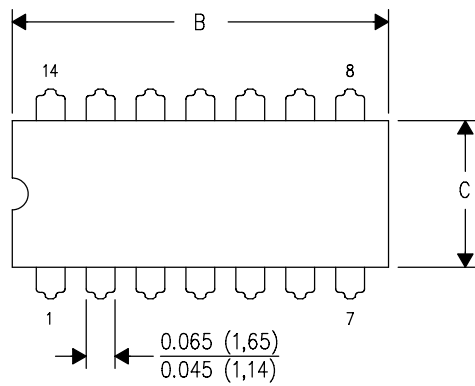
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

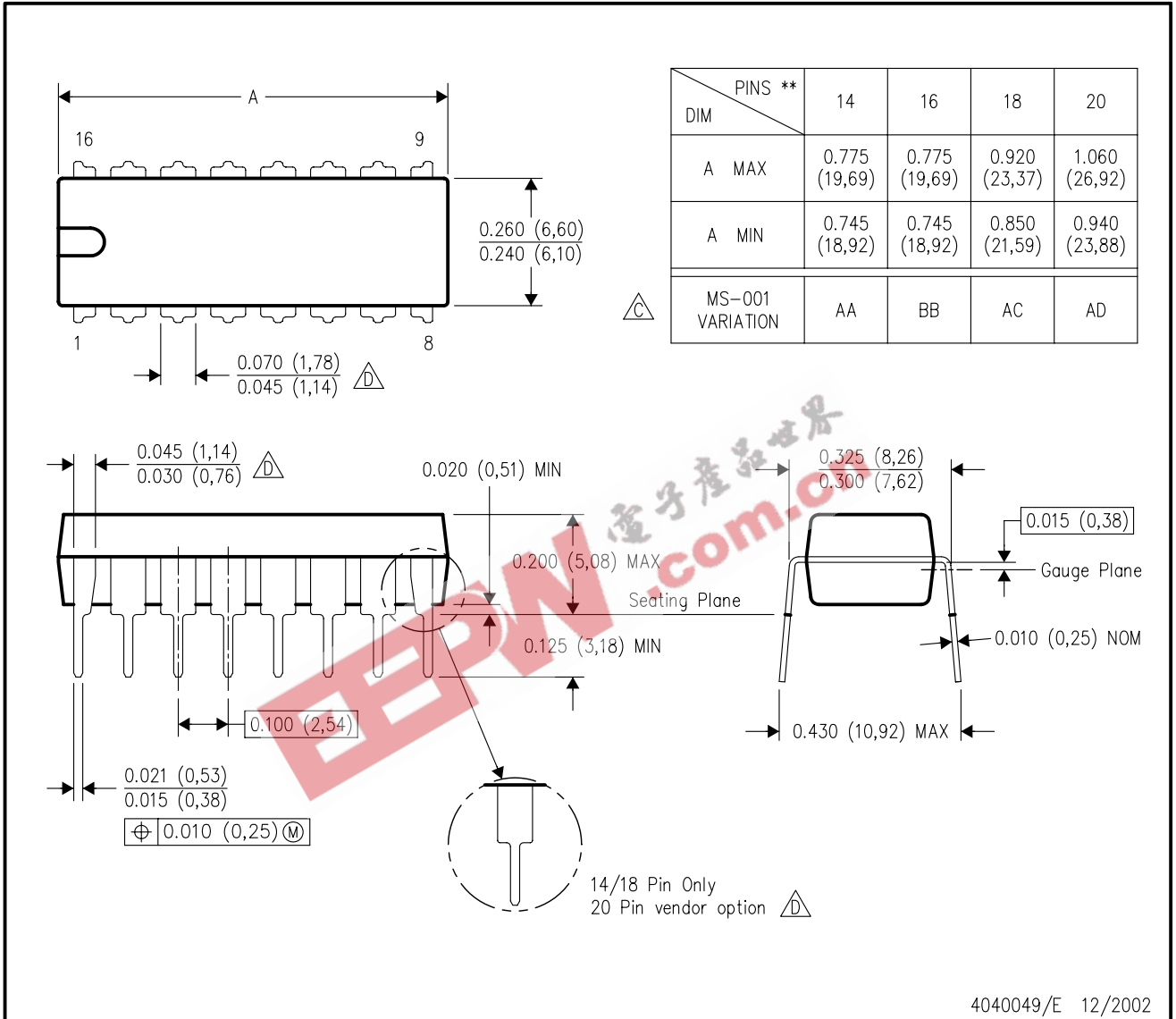
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

- △ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 △ The 20 pin end lead shoulder width is a vendor option, either half or full width.

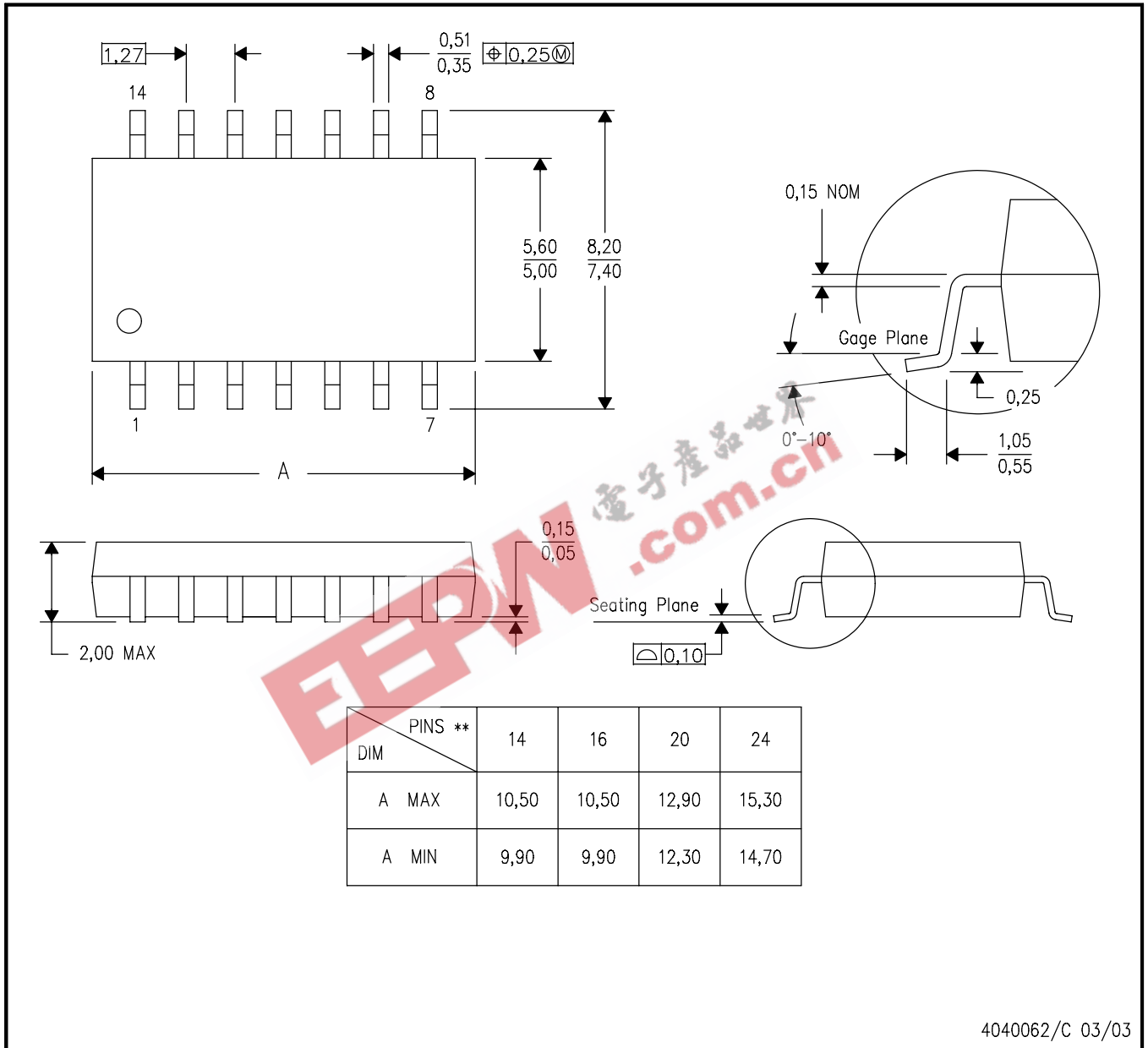


## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-153

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