



Data sheet acquired from Harris Semiconductor
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CD54/74FCT240, CD54/74FCT240AT, CD54/74FCT241, CD54/74FCT244, CD54/74FCT244AT

FCT Interface Logic Octal Buffers/Line Drivers, Three-State

Features

- CD54/74FCT240, CD54/74FCT240AT - Inverting
- CD54/74FCT241, CD54/74FCT244, CD54/74FCT244AT - Non-Inverting
- Buffered Inputs
- Typical Propagation Delay:
4.1ns at VCC = 5V, TA = 25°C (FCT240AT, FCT244AT)
- SCR-Latchup-Resistant BiCMOS Process and Circuit Design
- FCTXXX Types - Speed of Bipolar FAST®/AS/S;
FCTXXXAT Types - 30% Faster Than FAST/AS/S with
Significantly Reduced Power Consumption
- 48mA to 64mA Output Sink Current (Commercial/Extended Industrial)
- Output Voltage Swing Limited to 3.7V at VCC = 5V
- Controlled Output-Edge Rates
- Input/Output Isolation to VCC
- BiCMOS Technology with Low Quiescent Power

Ordering Information

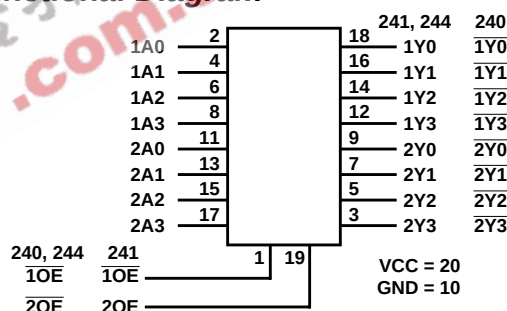
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54/74FCT240E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT240ATE	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT241E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT244E	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT244ATE	-55 to 125, 0 to 70	20 Ld PDIP
CD54/74FCT240M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT240ATM	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT241M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT244M	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT244ATM	-55 to 125, 0 to 70	20 Ld SOIC
CD54/74FCT240SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54/74FCT241SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54/74FCT244SM	-55 to 125, 0 to 70	20 Ld SSOP
CD54FCT240H	-55 to 125	
CD54FCT241H	-55 to 125	
CD54FCT244H	-55 to 125	

Description

The CD54/74FCT240, 240AT, 241, 244 and 244AT three-state octal buffers/line drivers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48mA to 64mA.

The CD54/74FCT240, 240AT, 244 and 244AT have active-LOW output enables ($\overline{1OE}$, $\overline{2OE}$). The CD54/74FCT241 and CD54/74FCT241AT have one active-LOW ($\overline{1OE}$) and one active-HIGH (2OE) output enable.

Functional Diagram



CD54/74FCT240, CD54/74FCT240AT TRUTH TABLE

INPUT	INPUT	OUTPUT
$\overline{1OE}, \overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

CD54/74FCT244, CD54/74FCT244AT TRUTH TABLE

INPUT	INPUT	OUTPUT
$\overline{1OE}, \overline{2OE}$	A	Y
L	L	H
L	H	L
H	X	Z

CD54/74FCT241 TRUTH TABLE

INPUT	OUTPUT	INPUT	OUTPUT
$\overline{1OE}$	1A	2OE	2A
L	L	L	X
L	H	H	L
H	X	H	H

NOTE: H = High Voltage Level, L = LOW Voltage Level
X = Immaterial, Z = HIGH Impedance

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CD54/74FCT540, CD54/74FCT540AT, CD54/74FCT241, CD54/74FCT244, CD54/74FCT244AT

Switching Specifications FCT Series $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L - See Figure 2

PARAMETER		SYMBOL	V _{CC} (V)	+25° C	0°C to +70°C		-55°C to +125°C		+25° C	0°C to +70°C		-55°C to +125°C		UNITS
				TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays														
Data to Outputs	FCT240/AT	t _{PLH} , t _{PHL}	5†	5	1.5	8	1.5	9	4.4	1.5	5.6	1.5	6.7	ns
	FCT241	t _{PLH} , t _{PHL}	5	4	1.5	6.5	1.5	7	-	-	-	-	-	ns
	FCT244/AT	t _{PLH} , t _{PHL}	5	4.5	1.5	6.5	1.5	7	3.8	1.5	5.3	1.5	6.2	μs
Output Enable Times	FCT240/AT	t _{PZL} , t _{PZH}	5	7	1.5	10	1.5	10.5	4.7	1.5	6.2	1.5	7.7	μs
	FCT241	t _{PZL} , t _{PZH}	5	5.5	1.5	8	1.5	8.5	-	-	-	-	-	ns
	FCT244/AT	t _{PZL} , t _{PZH}	5	6	1.5	8	1.5	8.5	4.8	1.5	6.5	1.5	7.8	ns
Output Disable Times	FCT240/AT	t _{PLZ} , t _{PHZ}	5	6	1.5	9.5	1.5	10	4	1.5	5.6	1.5	6.5	μs
	FCT241	t _{PLZ} , t _{PHZ}	5	4.5	1.5	7	1.5	7.5	-	-	-	-	-	ns
	FCT244/AT	t _{PLZ} , t _{PHZ}	5	5	1.5	7	1.5	7.5	4.5	1.5	5.8	1.5	6.8	μs
Power Dissipation Capacitance	FCT240/AT	C _{PD} §	-	38 Typical					38 Typical					pF
	FCT241	C _{PD} §	-	33 Typical					-					pF
	FCT244/AT	C _{PD} §	-	35 Typical					35 Typical					pF
Min. (Valley) V _{OHV} During Switch- ing of Other Outputs (Output Under Test Not Switching)		V _{OHV} See Figure 1	5	0.5 Typical at +25°C										V
Max. (Peak) V _{OLP} During Switch- ing of Other Outputs (Output Under Test Not Switching)		V _{OLP} See Figure 1	5	1 Typical at +25°C										V
Input Capacitance		C _I	-	-	-	10	-	10	-	-	10	-	10	pF
3-State Output Capacitance		C _O	-	-	-	15	-	15	-	-	15	-	15	pF

† 5V: min. is at 5.5V, max. is at 4.5V.

5V: min. is at 5.25V for 0°C to +70°C, max. is at 4.75V for 0°C to +70°C, typ. is at 5V

§ C_{PD} , measured per function, is used to determine the dynamic power consumption. P_D (per package) = $V_{CC} I_{CC} + \sum (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} \Delta I_{CC} D)$ where:

V_{CC} = supply voltage

ΔI_{CC} = flow through current x unit load

C_L = output load capacitance

D = duty cycle of input high

f_o = output frequency

f_i = input frequency

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