

CD40192BMS CD40193BMS

CMOS Presettable Up/Down Counters (Dual Clock With Reset)

December 1992

Features

- CD40192BMS - BCD Type
- CD40193BMS - Binary Type
- High Voltage Type (20V Rating)
- Individual Clock Lines for Counting Up or Counting Down
- Synchronous High-Speed Carry and Borrow Propagation Delays for Cascading
- Asynchronous Reset and Preset Capability
- Medium Speed Operation
 - fCL = 8MHz (typ.) at 10V
- 5V, 10V and 15V Parametric Ratings
- Standardize Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Up/Down Difference Counting
- Multistage Ripple Counting
- Synchronous Frequency Dividers
- A/D and D/A Conversion
- Programmable Binary or BCD Counting

Description

CD40192BMS Presettable BCD Up/Down Counter and the CD40193BMS Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET}} \overline{\text{ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET}} \overline{\text{ENABLE}}$ control is low.

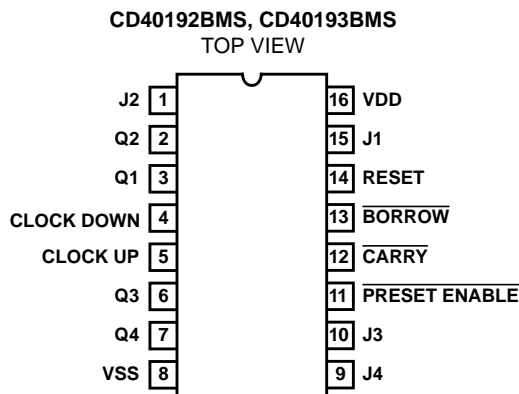
The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

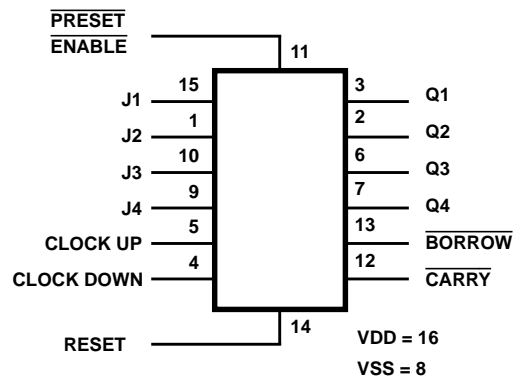
The CD40192BMS and CD40193BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H4W,	†H4X
Frit Seal DIP	H1F	
Ceramic Flatpack	*H6P,	†H6W
* CD40192B Only	†CD40193B Only	

Pinout



Functional Diagram



Specifications CD40192BMS, CD40193BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input ±10mA
 Operating Temperature Range -55°C to +125°C
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to +150°C
 Lead Temperature (During Soldering) +265°C
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at +125°C
 For $T_A = -55^\circ\text{C}$ to +100°C (Package Type D, F, K) 500mW
 For $T_A = +100^\circ\text{C}$ to +125°C (Package Type D, F, K) Derate
 Linearity at 12mW/°C to 200mW
 Device Dissipation per Output Transistor 100mW
 For $T_A =$ Full Package Temperature Range (All Package Types)
 Junction Temperature +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
 2. Go/No Go test with limits applied to inputs.

Specifications CD40192BMS, CD40193BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock Up or Clock Down to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Reset to Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay PE to Q	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Clock Up to Carry, Clock Down to Borrow	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	320	ns
			10, 11	+125°C, -55°C	-	432	ns
Propagation Delay PE to Borrow or Carry	TPHL5 TPLH5	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Reset to Borrow or Carry	TPHL6 TPLH6	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA

Specifications CD40192BMS, CD40193BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock Up or Down to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Reset to Q	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay PE to Q	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Propagation Delay Clock Up to Carry, Clock Down to Borrow	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay PE to Borrow or Carry	TPHL5 TPLH5	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Propagation Delay Reset to Borrow or Carry	TPHL6 TPLH6	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Transition Time	TTHL1 TTLH1	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	15	μs
		VDD = 10V	1, 2, 3, 4	+25°C	-	15	μs
		VDD = 15V	1, 2, 3, 4	+25°C	-	5	μs
Minimum Removal Time Reset or PE	TREM	VDD = 5V	1, 2, 3, 5	+25°C	-	80	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	40	ns
		VDD = 15V	1, 2, 3, 5	+25°C	-	30	ns
Minimum Pulse Width Reset	TW	VDD = 5V	1, 2, 3	+25°C	-	480	ns
		VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	260	ns
Minimum Pulse Width PE	TW	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns

Specifications CD40192BMS, CD40193BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Reset	1, 2	+25°C	-	15	pF
Input Capacitance	CIN	All Other Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.
5. The time required for RESET or PRESET ENABLE control to be removed before clocking. See timing diagram defining TREM.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND VDD = 3V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

Specifications CD40192BMS, CD40193BMS

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± 0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD40192BMS, CD40193BMS						
Static Burn-In 1 (Note 1)	2, 3, 6, 7, 12, 13	1, 4, 5, 8 - 11, 14, 15	16			
Static Burn-In 2 (Note 1)	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16			
Dynamic Burn-In (Note 1)	-	8, 14	1, 5, 9 - 11, 15, 16	2, 3, 6, 7, 12, 13	4	-
Irradiation (Note 2)	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16			

NOTES:

- Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$, $VDD = 18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, $VDD = 10V \pm 0.5V$

CD40192BMS, CD40193BMS

Logic Diagrams

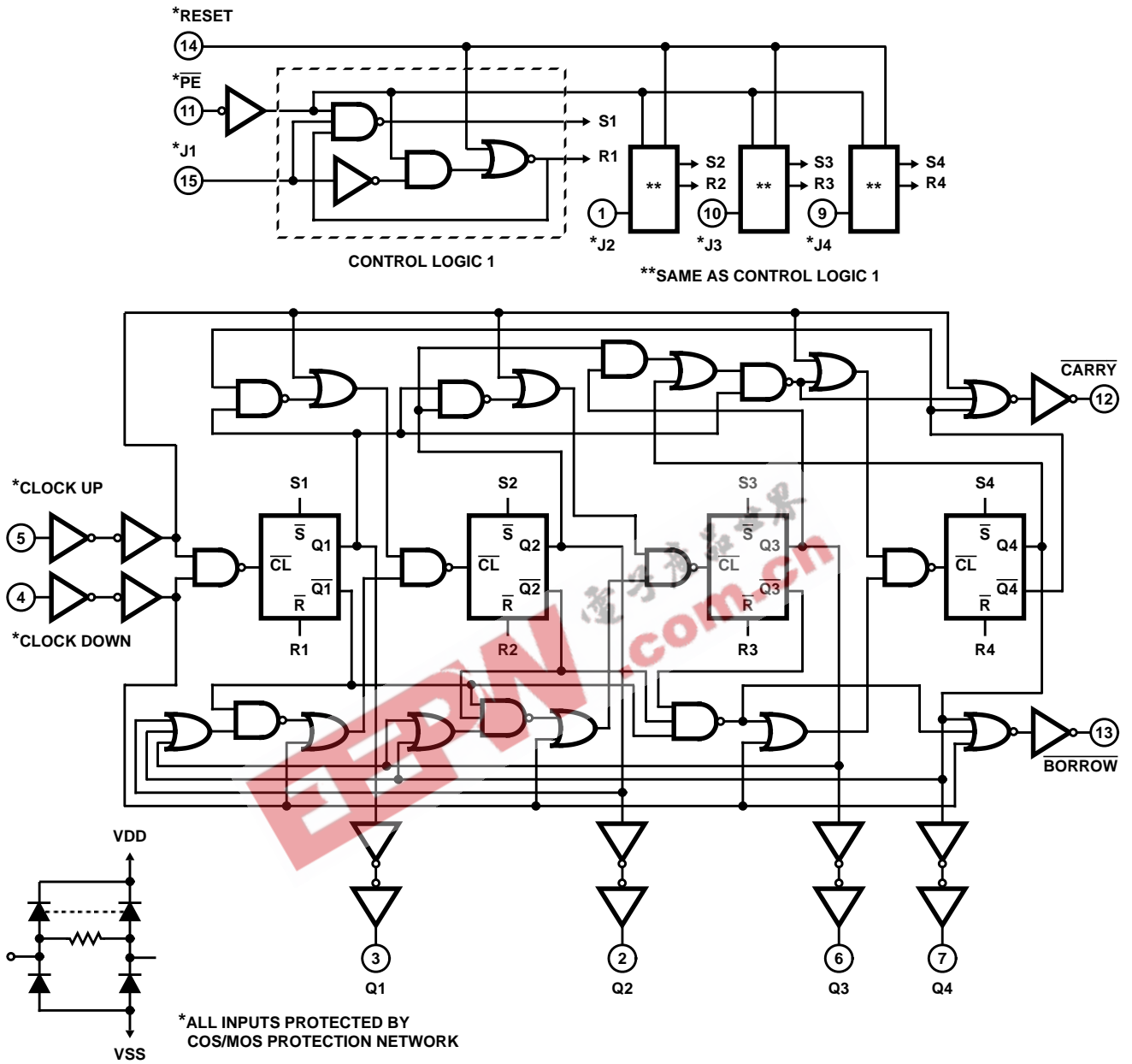


FIGURE 1. CD40192BMS LOGIC DIAGRAM (BCD)

CD40192BMS, CD40193BMS

Logic Diagrams (Continued)

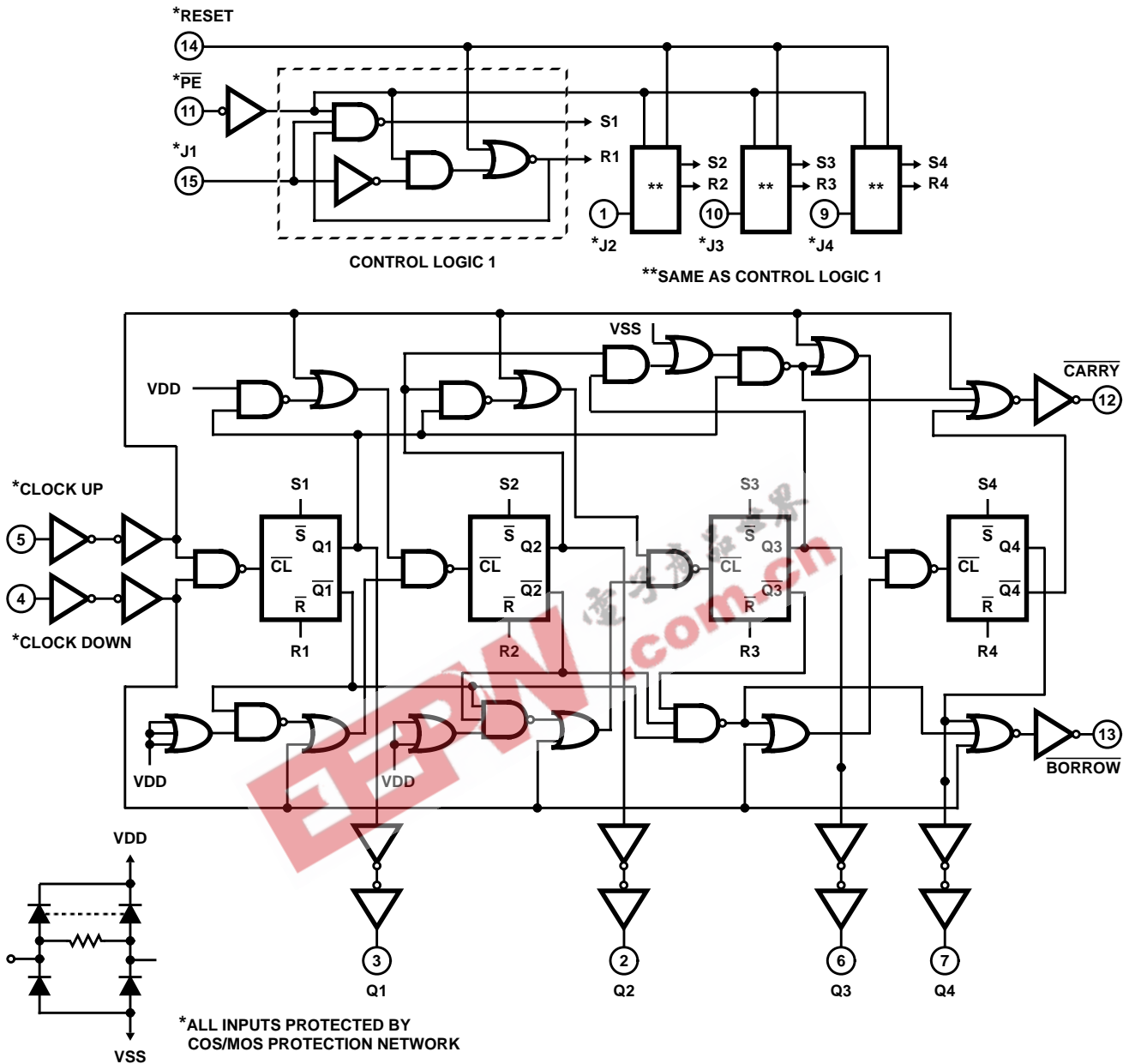


FIGURE 2. CD40193BMS LOGIC DIAGRAM (BINARY)

CD40192BMS, CD40193BMS

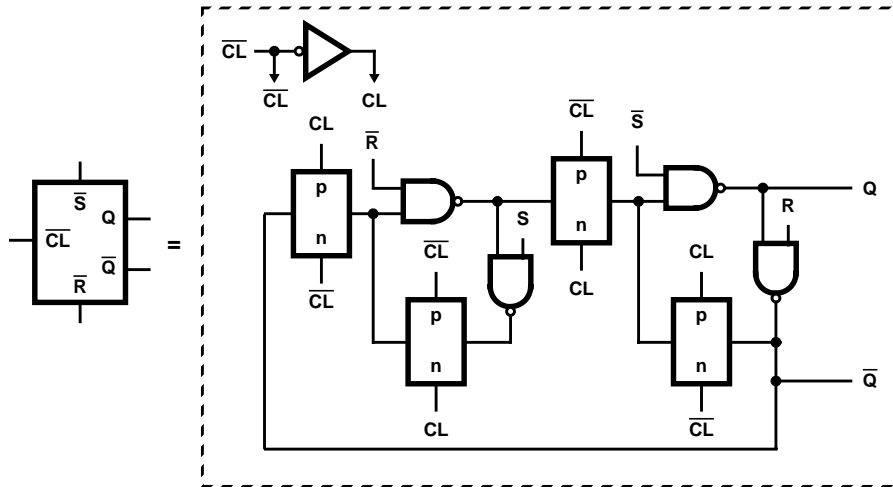


FIGURE 3. INTERNAL LOGIC OF FLIP-FLOP

TRUTH TABLE

CLOCK UP	CLOCK DOWN	PRESET ENABLE	RESET	ACTION
	1	1	0	Count Up
	1	1	0	No Count
1		1	0	Count Down
1		1	0	No Count
X	X	0	0	Preset
X	X	X	1	Reset

1 = High Level

0 = Low Level

X = Don't Care

Typical Performance Characteristics

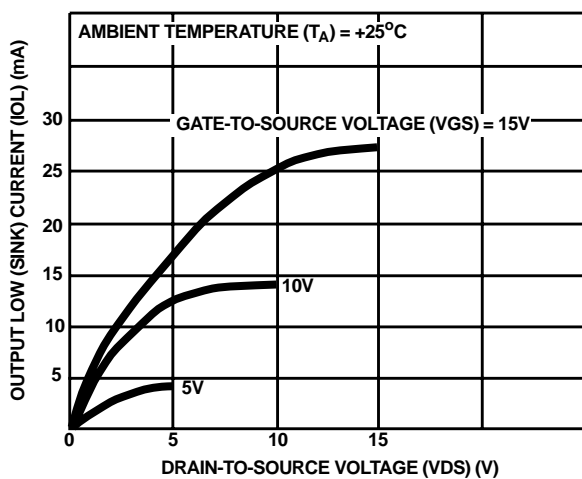


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

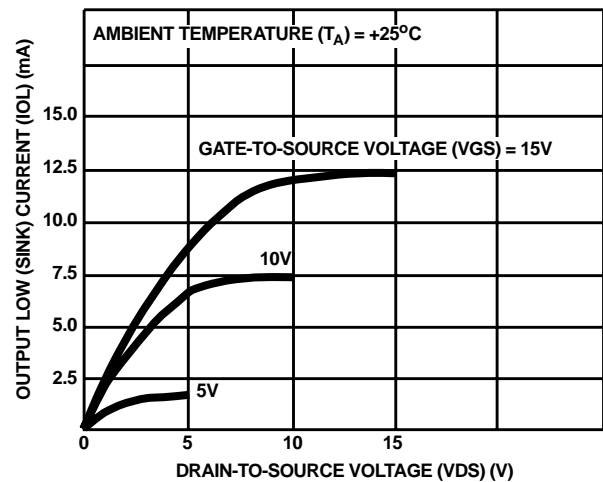


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

CD40192BMS, CD40193BMS

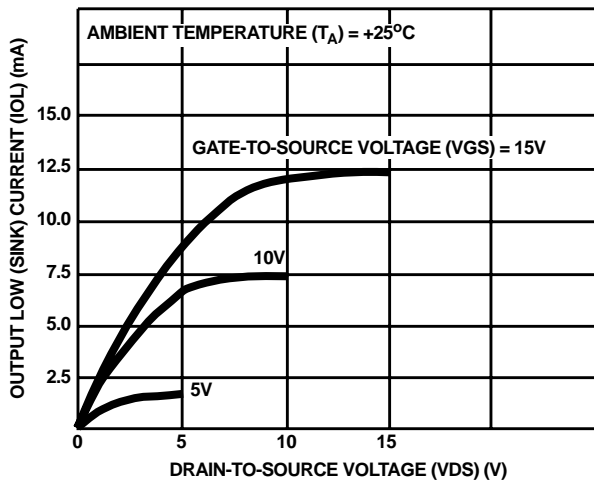


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

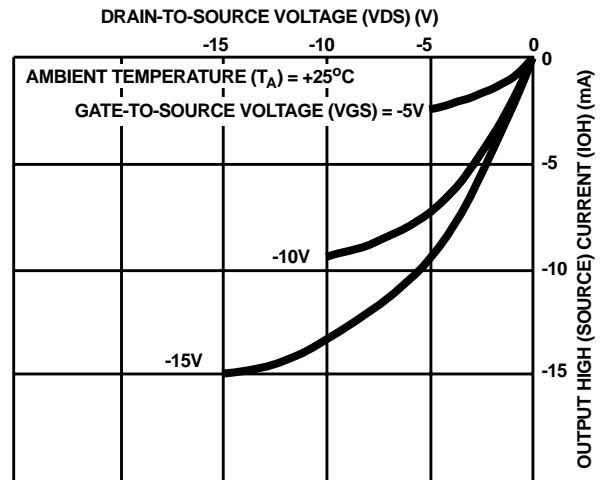


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

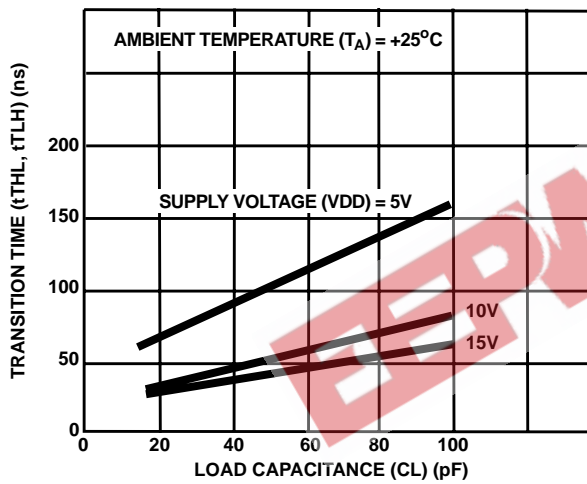


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

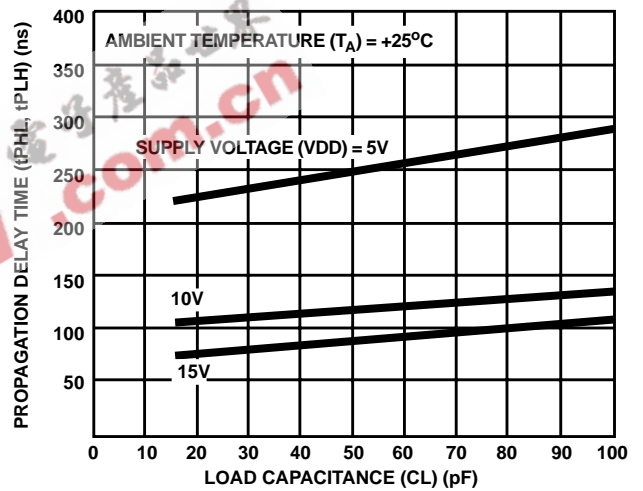


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

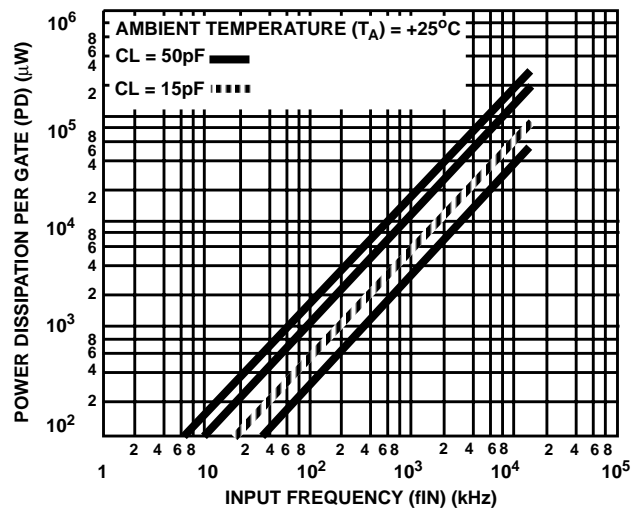


FIGURE 10. DYNAMIC POWER DISSIPATION

CD40192BMS, CD40193BMS

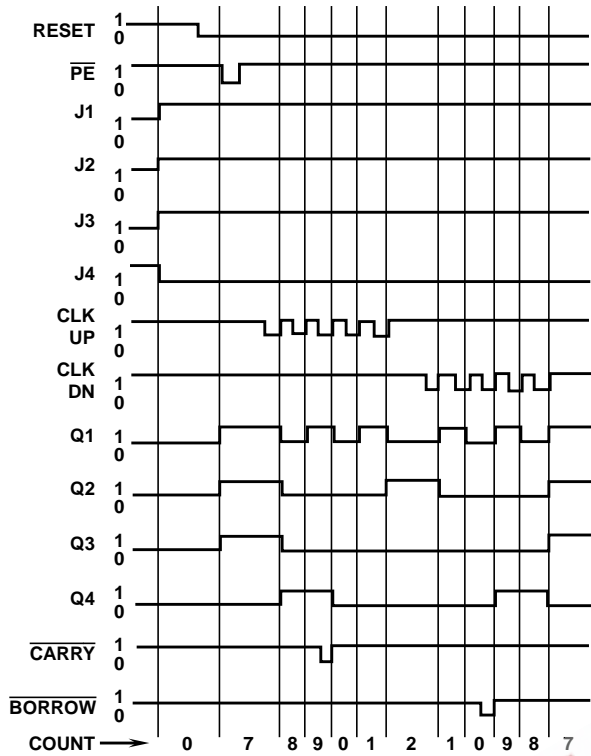


FIGURE 11. CD40192BMS TIMING DIAGRAM

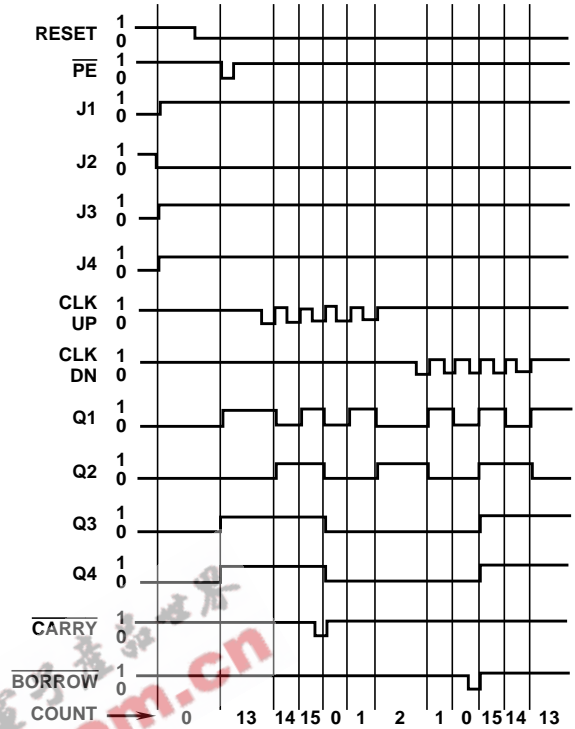
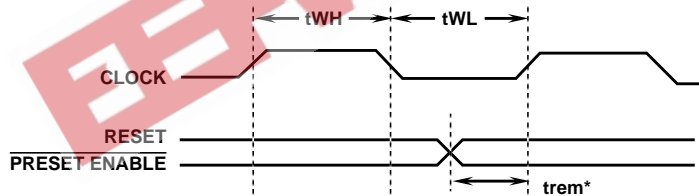


FIGURE 12. CD40193BMS TIMING DIAGRAM



*RESET OR PRESET ENABLE
REMOVAL TIME

FIGURE 13. TIMING DIAGRAM DEFINING t_{rem}

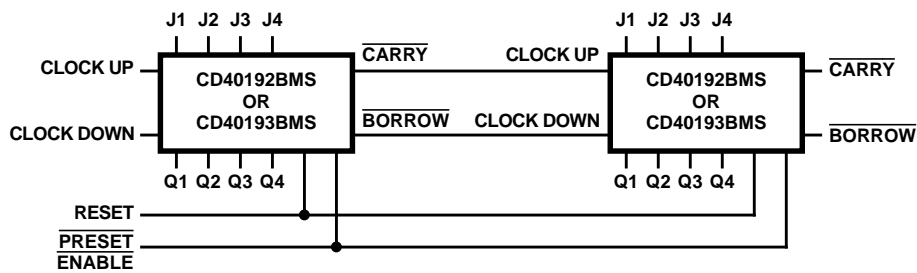
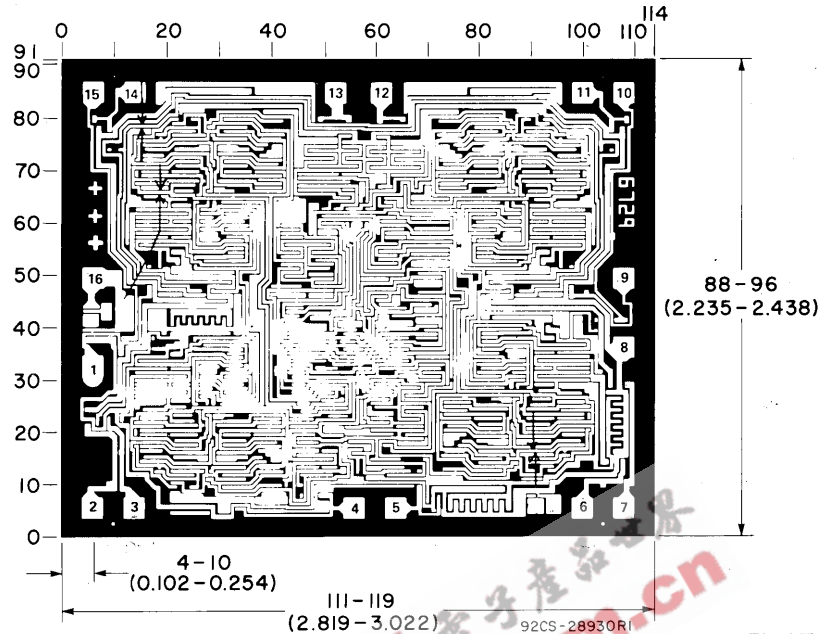


FIGURE 14. CASCADED COUNTER PACKAGES

CD40192BMS, CD40193BMS

Chip Dimensions and Pad Layout



Dimensions and pad layout for the CD40192BMSH
(dimensions and pad layout for the CD40193BMSH
are identical).

Dimensions in parentheses are in millimeters
and are derived from the basic inch dimensions
as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.
PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

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