HARRIS SEMICONDUCTOR

CD54AC112/3A
CD54ACT112/3A

June 1997

COMPLETE DATA SHEET COMING SOON!

Dual “J-K” Flip-Flop with Set and Reset

Description

The CD54AC112/3A and CD54ACT112/3A are dual “J-K” flip-flops with set and reset that utilize the Harris Advanced CMOS Logic technology. These flip-flops have independent J, K, $\overline{Set}$, $\overline{Reset}$ and Clock inputs and Q and $\overline{Q}$ outputs. The CD54AC112/3A and CD54ACT112/3A changes state on the negative-going transition of the clock. $\overline{Set}$ and $\overline{Reset}$ are accomplished asynchronously by low-level inputs.

The CD54AC112/3A and CD54ACT112/3A are supplied in 16 lead dual-in-line ceramic packages (F suffix).

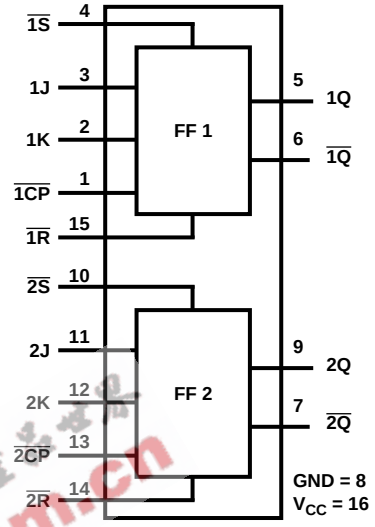
ACT INPUT LOAD TABLE

INPUT	UNIT LOAD (NOTE 1)
J, CP, $\overline{CP}$	1
K	0.53
$\overline{S}$, $\overline{R}$	0.58

NOTE:

1. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA Max at +25°C.

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to +6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±50mA
DC Output Source or Sink Current, Per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±50mA
DC V_{CC} or GND Current, I_{CC} or I_{GND}
For Up to 4 Outputs Per Device, Add ±25mA For Each Additional Output . . . . . ±100mA

Power Dissipation Per Package, P_D
T_A = -55°C to +100°C (Package F) 500mW
T_A = +100°C to +125°C (Package F) . . . . . Derate Linearly at 8mW/°C to 300mW
Operating Temperature Range, T_A
Package Type F . . . . . -55°C to +125°C
Storage Temperature, T_{STG} . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
From Case For 10s Max . . . . . +265°C
Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)
With Solder Contacting Lead Tips Only. . . . . +300°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply Voltage Range, V_{CC}
Unless Otherwise Specified, All Voltages Referenced to GND
T_A = Full Package Temperature Range
CD54AC Types . . . . . 1.5V to 5.5V
CD54ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}

Operating Temperature, T_A . . . . . -55°C to +125°C
Input Rise and Fall Slew Rate, dt/dv
at 1.5V to 3V (AC Types) . . . . . 0ns/V to 50ns/V
at 3.6V to 5.5V (AC Types) . . . . . 0ns/V to 20ns/V
at 4.5V to 5.5V (AC Types) . . . . . 0ns/V to 10ns/V

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