

# Off-Line Current Mode PWM Control Circuit with Undervoltage Lockout

## Description

The CS284XA, CS384XA provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS384XA family incorporates a new precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty-cycle clamp eliminates the need for an external oscillator when a 50% duty-cycle is used. Duty-cycles greater than 50% are also possible. On board logic ensures that  $V_{REF}$  is stabilized before

the output stage is enabled. Ion implant resistors provide tighter control of undervoltage lockout.

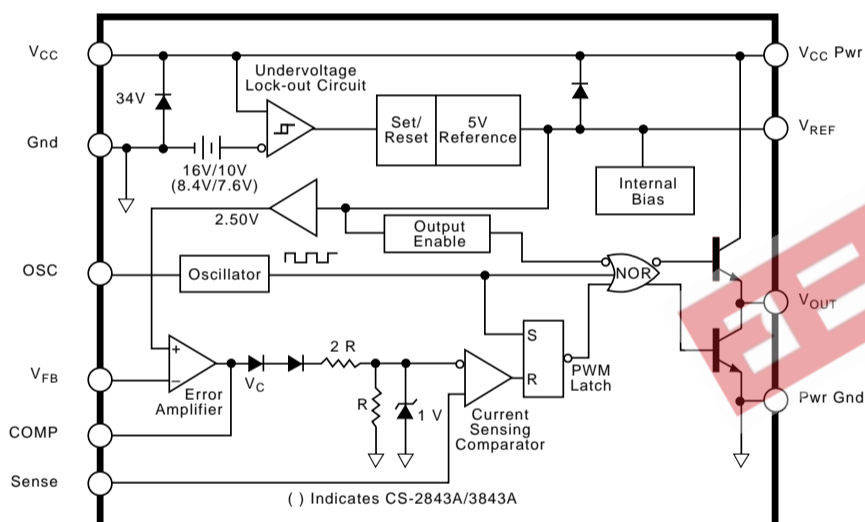
Other features include low start-up current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as the gate of power MOSFET. The output is LOW in the off state, consistent with N-channel devices.

The CS384XA series of current-mode control ICs are available in 8 and 14 lead packages for surface mount (SO) applications as well as 8 lead PDIP packages.

## Absolute Maximum Ratings

Supply Voltage ( $I_{CC} < 30mA$ ).....	Self Limiting
Supply Voltage (Low Impedance Source) .....	30V
Output Current.....	$\pm 1A$
Output Energy (Capacitive Load) .....	5 $\mu J$
Analog Inputs ( $V_{FB}$ , Sense).....	-0.3V to 5.5V
Error Amp Output Sink Current .....	10mA
Lead Temperature Soldering	
Wave Solder (through hole styles only) .....	10 sec. max, 260°C peak
Reflow (SMD styles only) .....	60 sec. max above 183°C, 230°C peak

## Block Diagram

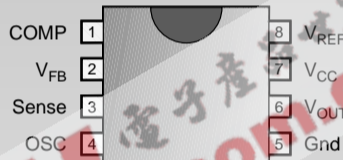


## Features

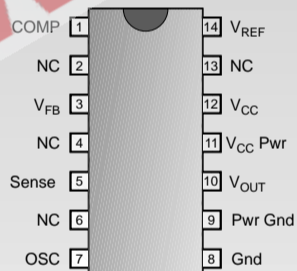
- Optimized for Off-line Control
- Internally Trimmed Temperature Compensated Oscillator
- Maximum Duty-cycle Clamp
- $V_{REF}$  stabilized before Output Stage is Enabled
- Low Start-up Current
- Pulse-by-pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1% Trimmed Bandgap Reference
- High Current Totem Pole Output

## Package Options

### 8 Lead PDIP & SO Narrow



### 14 Lead SO Narrow



Electrical Characteristics:  $-25^{\circ} \leq T_A \leq 85^{\circ} \text{C}$  for CS2842A/2843A,  $0^{\circ} \leq T_A \leq 70^{\circ} \text{C}$  for CS3842A/3843A.  $V_{CC} = 15\text{V}$  (Note 1);  $R_T = 680\Omega$ ,  $C_T = .022\mu\text{F}$  for triangular mode,  $R_T = 10\text{k}\Omega$ ,  $C_T = 3.3\text{nF}$  for sawtooth mode (see Figure 3), unless otherwise stated.

PARAMETER	TEST CONDITIONS	CS2842A/CS2843A			CS3842A/CS3843A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Output Voltage	$T_J = 25^{\circ}\text{C}$ , $I_{OUT} = 1\text{mA}$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25\text{V}$		6	20		6	20	mV
Load Regulation	$1 \leq I_{OUT} \leq 20\text{mA}$		6	25		6	25	mV
Temperature Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/ $^{\circ}\text{C}$
Total Output Variation	Line, Load, Temp. (Note 2)	4.90		5.10	4.82		5.18	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$ , $T_J = 25^{\circ}\text{C}$ (Note 2)		50			50		$\mu\text{V}$
Long Term Stability	$T_A = 125^{\circ}\text{C}$ , 1kHrs. (Note 2)		5	25		5	25	mV
Output Short Circuit	$T_A = 25^{\circ}\text{C}$	-30	-100	-180	-30	-100	-180	mA
<b>Oscillator Section</b>								
Initial Accuracy	Sawtooth Mode (see Fig. 3), $T_J = 25^{\circ}\text{C}$	47	52	57	47	52	57	kHz
	Triangular Mode (see Fig. 3), $T_J = 25^{\circ}\text{C}$	47	52	57	44	52	60	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{V}$		0.2	1.0		0.2	1.0	%
Temp. Stability	Sawtooth Mode $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
	Triangular Mode $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		8			8		%
Amplitude	OSC peak to peak		1.7			1.7		V
Discharge Current	$T_J = 25^{\circ}\text{C}$	7.5	8.3	9.3	7.5	8.3	9.3	mA
	$T_{MIN} \leq T_A \leq T_{MAX}$	7.2		9.5	7.2		9.5	mA
<b>Error Amp Section</b>								
Input Voltage	$V_{COMP} = 2.5\text{V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current	$V_{FB} = 0$		-0.3	-1.0		-0.3	-2.0	$\mu\text{A}$
$A_{VOL}$	$2 \leq V_{OUT} \leq 4\text{V}$	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1.0		0.7	1.0		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		60	70		dB
Output Sink Current	$V_{FB} = 2.7\text{V}$ , $V_{COMP} = 1.1\text{V}$	2	6		2	6		mA
Output Source Current	$V_{FB} = 2.3\text{V}$ , $V_{COMP} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		mA
$V_{OUT}$ High	$V_{FB} = 2.3\text{V}$ , $R_L = 15\text{k}\Omega$ to ground	5	6		5	6		V
$V_{OUT}$ Low	$V_{FB} = 2.7\text{V}$ , $R_L = 15\text{k}\Omega$ to $V_{REF}$		0.7	1.1		0.7	1.1	V
<b>Current Sense Section</b>								
Gain	(Notes 3 & 4)	2.85	3.00	3.15	2.85	3.00	3.15	V/V
Maximum Input Signal	$V_{COMP} = 5\text{V}$ (Note 3)	0.9	1.0	1.1	0.9	1.0	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 3)		70			70		dB
Input Bias Current	$V_{sense} = 0$		-2	-10		-2	-10	$\mu\text{A}$
Delay to Output	$T_J = 25^{\circ}\text{C}$ (Note 2)		150	300		150	300	ns
<b>Output Section</b>								
Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 200\text{mA}$		1.5	2.2		1.5	2.2	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13.0	13.5		13.0	13.5		V
	$I_{SOURCE} = 200\text{mA}$	12.0	13.5		12.0	13.5		V

Electrical Characteristics: continued

CS2842A/3843A SERIES

PARAMETER	TEST CONDITIONS	CS2842A/CS2843A			CS3842A/CS3843A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>■ Output Section: continued</b>								
Rise Time	T <sub>J</sub> = 25°C, C <sub>L</sub> = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T <sub>J</sub> = 25°C, C <sub>L</sub> = 1nF (Note 2)		50	150		50	150	ns
Output Leakage	UVLO Active, V <sub>OUT</sub> = 0		-0.01	-10.00		-0.01	-10.00	μA

■ Total Standby Current

Start-Up Current			0.5	1.0		0.5	1.0	mA
Operating Supply Current	V <sub>FB</sub> = V <sub>Sense</sub> = 0V, R <sub>T</sub> = 10kΩ, C <sub>T</sub> = 3.3nF	11	17		11	17		mA
V <sub>CC</sub> Zener Voltage	I <sub>CC</sub> = 25mA		34			34		V

PARAMETER	TEST CONDITIONS	CS2842A			CS3842A			CS2843A/CS3843A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>■ Under-Voltage Lockout Section</b>											
Start Threshold		15	16	17	14.5	16.0	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	9	10	11	8.5	10.0	11.5	7.0	7.6	8.2	V

- Notes: 1. Adjust V<sub>CC</sub> above the start threshold before setting at 15V. 2. These parameters, although guaranteed, are not 100% tested in production. 3. Parameter measured at trip point of latch with V<sub>FB</sub>=0. 4. Gain defined as:

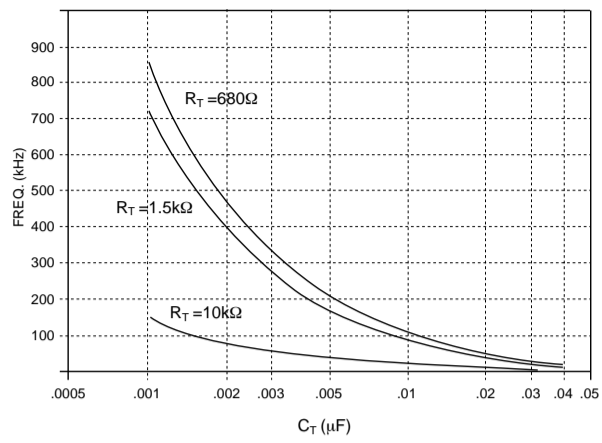
$$A = \frac{\Delta V_{COMP}}{\Delta V_{Sense}} ; 0 \leq V_{Sense} \leq 0.8V.$$

Package Pin Description

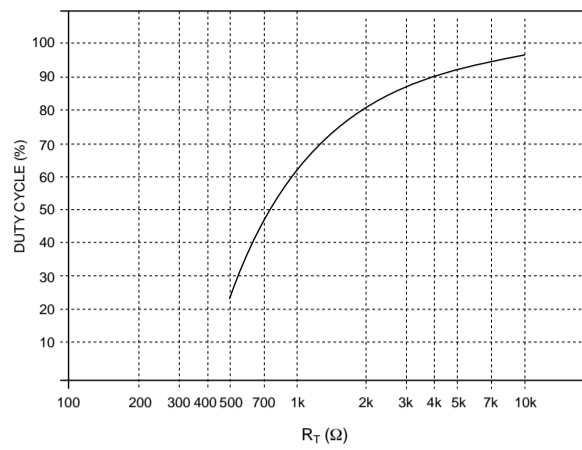
PACKAGE PIN #		PIN SYMBOL	FUNCTION
8L PDIP/SO	14L SO Narrow		
1	1	COMP	Error amp output, used to compensate error amplifier
2	3	V <sub>FB</sub>	Error amp inverting input
3	5	Sense	Noninverting input to Current Sense Comparator
4	7	OSC	Oscillator timing network with Capacitor to Ground, resistor to V <sub>REF</sub>
5	8	Gnd	Ground
	9	Pwr Gnd	Output driver Ground
6	10	V <sub>OUT</sub>	Output drive pin
	11	V <sub>CCPWR</sub>	Output driver positive supply
7	12	V <sub>CC</sub>	Positive power supply
8	14	V <sub>REF</sub>	Output of 5V internal reference
	2,4,6,13	NC	No Connection

Typical Performance Characteristics

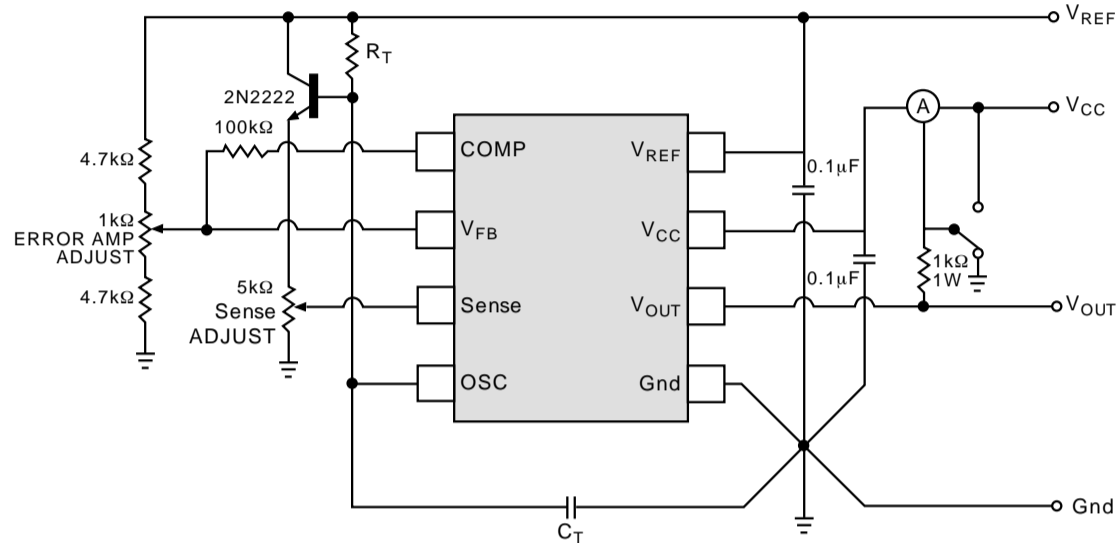
Oscillator Frequency vs  $C_T$



Oscillator Duty Cycle vs  $R_T$



Test Circuit



Circuit Description

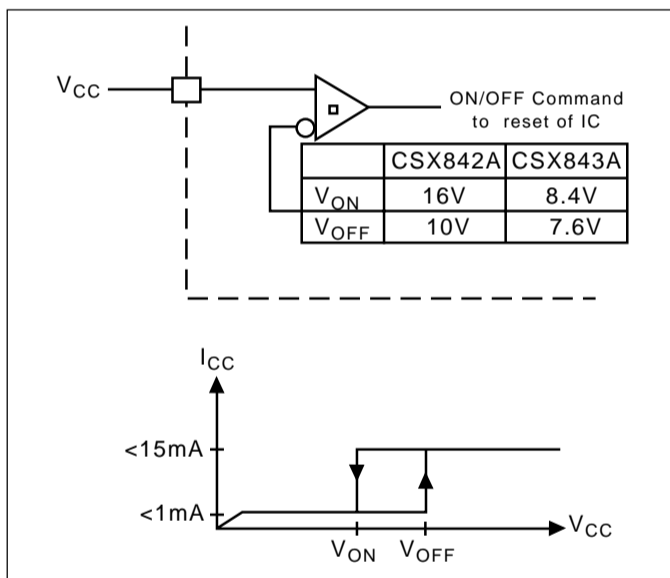


Figure 1: Typical Undervoltage Characteristics

Undervoltage Lockout

During Undervoltage Lockout (Figure 1), the output driver is biased to a high impedance state. The output should be shunted to ground with a resistor to prevent output leakage current from activating the power switch.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 2). An increase in  $V_{CC}$  causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent trans-

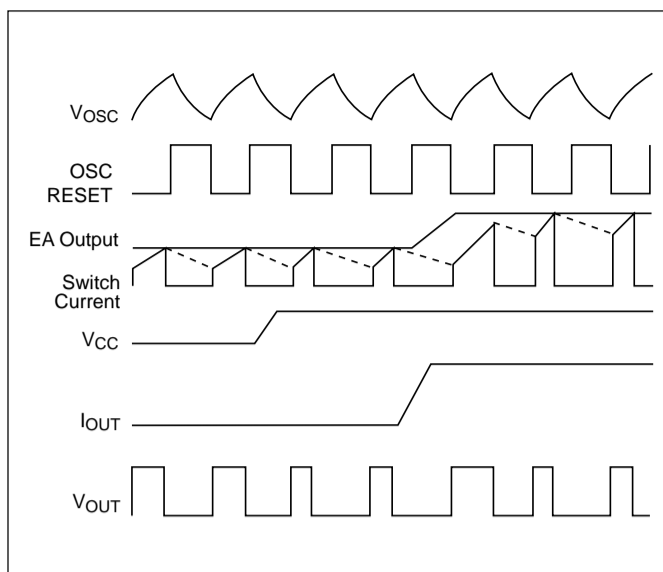


Figure 2: Timing Diagram for key CS2841B parameters

former saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of oscillator components.

### Setting the Oscillator

Oscillator timing capacitor,  $C_T$ , is charged by  $V_{REF}$  through  $R_T$  and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the Low state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the formula:

$$t_c = R_T C_T \ln \left( \frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}} \right)$$

$$t_d = R_T C_T \ln \left( \frac{V_{REF} - I_d R_T - V_{lower}}{V_{REF} - I_d R_T - V_{upper}} \right)$$

Substituting in typical values for the parameters in the above formulas:

$$V_{REF} = 5.0V, V_{upper} = 2.7V, V_{lower} = 1.0V, I_d = 8.3mA$$

$$t_c \approx 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln \left( \frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T} \right)$$

The frequency and maximum duty cycle can be determined using the Typical Performance Characteristic graphs.

### Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Gnd pin in a single point ground.

The transistor and 5k $\Omega$  potentiometer, shown in the test circuit, are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

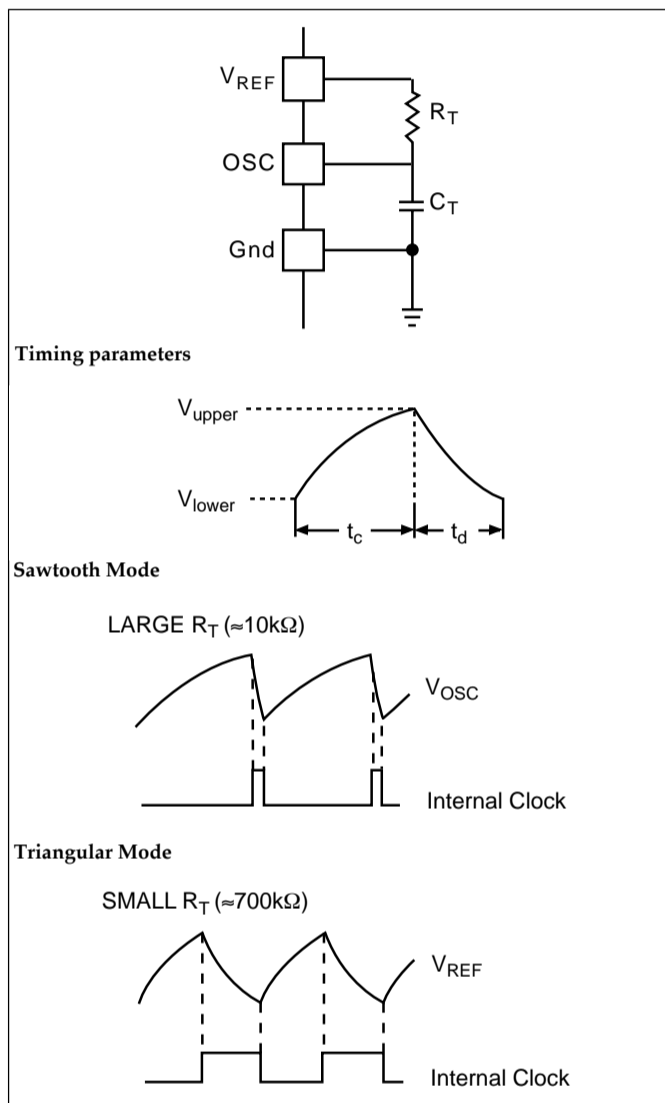


Figure 3: Oscillator Timing Network and parameters

## Package Specification

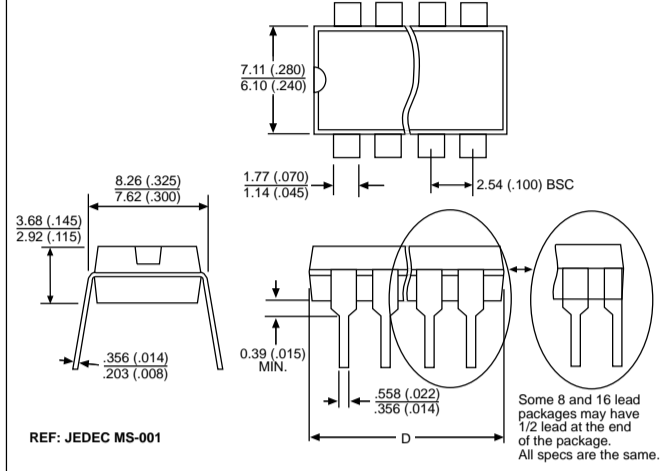
## PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead PDIP	10.16	9.02	.400	.355
8 Lead SO Narrow	5.00	4.80	.197	.189
14 Lead SO Narrow	8.75	8.55	.344	.337

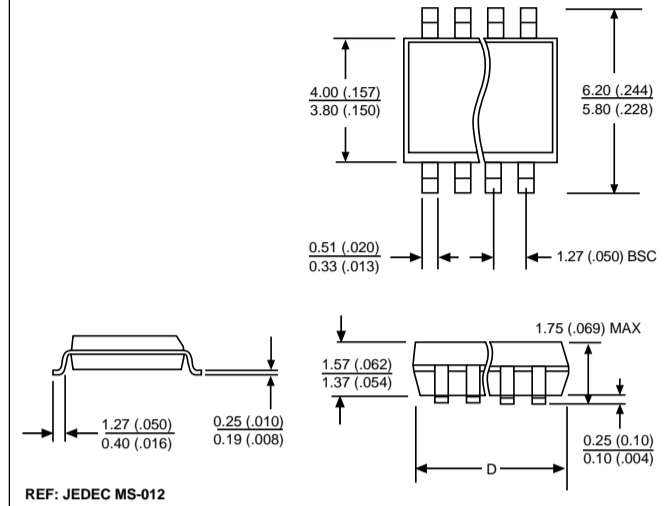
## PACKAGE THERMAL DATA

Thermal Data		8 L PDIP	8 L SO Narrow	14 L SO Narrow	
$R_{\theta JC}$	typ	52	45	30	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	typ	100	165	125	$^{\circ}\text{C}/\text{W}$

## Plastic DIP (N); 300 mil wide



## Surface Mount Narrow Body (D); 150 mil wide



## Ordering Information

Part Number	0°C to 70°C	-25°C to 85°C	Description
CS2842ALN8		•	8L PDIP
CS2843ALN8		•	8L PDIP
CS3842AGN8	•		8L PDIP
CS3842AGD8	•		8L SO Narrow
CS3842AGDR8	•		8L SO Narrow (tape & reel)
CS3842AGD14	•		14L SO Narrow
CS3842AGDR14	•		14L SO Narrow (tape & reel)
CS2843ALD14		•	14L SO Narrow
CS2843ALDR14		•	14L SO Narrow (tape & reel)
CS3843AGN8	•		8L PDIP
CS3843AGD8	•		8L SO Narrow
CS3843AGDR8	•		8L SO Narrow (tape & reel)
CS3843AGD14	•		14L SO Narrow
CS3843AGDR14	•		14L SO Narrow (tape & reel)

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