



High Speed Super Low Power SRAM

256K-Word By 8 Bit

CS18LV20483

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
1.0	Initial issue	Jan.26,2005	

ECPW 电子产品世界
.com.cn



High Speed Super Low Power SRAM

256K-Word By 8 Bit

CS18LV20483

■ GENERAL DESCRIPTION

The CS18LV20483 is a high performance, high speed, and super low power CMOS Static Random Access Memory organized as 262,144 words by 8 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.50uA and maximum access time of 55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable inputs (/CE1,CE2) and active LOW output enable (/OE) and three-state output drivers.

The CS18LV20483 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV20483 is available in JEDEC standard 32-pin sTSSOP (8x13.4 mm), TSOP (8x20mm), TSOP (II) (400mil) and SOP (450 mil) packages.

■ FEATURES

- Low operation voltage : 2.7 ~ 3.6V
Ultra low power consumption : 2mA@1MHz (Max.) operating current
0.50 uA (Typ.) CMOS standby current
- High speed access time : 55/70ns (Max.) at Vcc = 3.0V.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE and /OE options.

■ Product Family

Product Family	Operating Temp	Vcc. Range	Speed (ns)	Standby (Typ.)	Package Type
CS18LV20483	0~70°C	2.7~3.6	55/70	0.50 uA (Vcc = 3.0V)	32 SOP
					32 STSOP
					32 TSOP
					32 TSOP (II)
					Dice
	-40~85°C	2.7~3.6	55/70	0.8 uA (Vcc= 3.0V)	32 SOP
					32 STSOP
					32 TSOP
					32 TSOP (II)
					Dice



High Speed Super Low Power SRAM

256K-Word By 8 Bit

CS18LV20483

■ PIN DESCRIPTIONS

Name	Type	Function
A0 – A17	Input	Address inputs for selecting one of the 262,144 x 8 bit words in the RAM
/CE1, CE2	Input	/CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground
NC		No connection

■ TRUTH TABLE

MODE	/CE1	CE2	/WE	/OE	DQ0~7	Vcc Current
Standby	H	X	X	X	High Z	I _{CCSB} , I _{CCSB1}
	X	L	X	L		
Output Disabled	L	H	H	H	High Z	I _{CC}
Read	L	H	H	L	D _{OUT}	I _{CC}
Write	L	H	L	X	D _{IN}	I _{CC}



High Speed Super Low Power SRAM

256K-Word By 8 Bit

CS18LV20483

■ ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
T_{BIAS}	Temperature Under Bias	-40 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	25	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

Range	Ambient Temperature	V_{CC}
Commercial	0~70°C	2.7V ~ 3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

1. Overshoot : $V_{CC} + 2.0V$ in case of pulse width $\leq 20ns$.
2. Undershoot : $- 2.0V$ in case of pulse width $\leq 20ns$.
3. Overshoot and undershoot are sampled, not 100% tested.

■ CAPACITANCE ⁽¹⁾ ($T_A = 25^\circ C$, $f = 1.0 MHz$)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	$V_{IN}=0V$	6	pF
C_{DQ}	Input/Output Capacitance	$V_{IO}=0V$	8	pF

1. This parameter is guaranteed and not tested.



High Speed Super Low Power SRAM

256K-Word By 8 Bit

CS18LV20483

■ DC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C, Vcc = 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP ⁽¹⁾	MAX	Unit
V _{IL}	Guaranteed Input Low Voltage ⁽²⁾		-0.5		0.8	V
V _{IH}	Guaranteed Input High Voltage ⁽²⁾		2.0		V _{CC} +0.2	V
I _{IL}	Input Leakage Current	V _{CC} =MAX, V _{IN} =0 to V _{CC}	-1		1	uA
I _{OL}	Output Leakage Current	V _{CC} =MAX, /CE=V _{IN} , or /OE=V _{IN} , V _{IO} =0V to V _{CC}	-1		1	uA
V _{OL}	Output Low Voltage	V _{CC} =MAX, I _{OL} = 2mA			0.4	V
V _{OH}	Output High Voltage	V _{CC} =MIN, I _{OH} = -1mA	2.4			V
I _{CC}	Operating Power Supply Current	/CE=V _{IL} , I _{DQ} =0mA, F=F _{MAX} ⁽³⁾			25	mA
I _{CCSB}	Standby Supply - TTL	/CE=V _{IH} , I _{DQ} =0mA,			1	mA
I _{CCSB1}	Standby Current -CMOS	/CE ≥ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V		0.5	4	uA

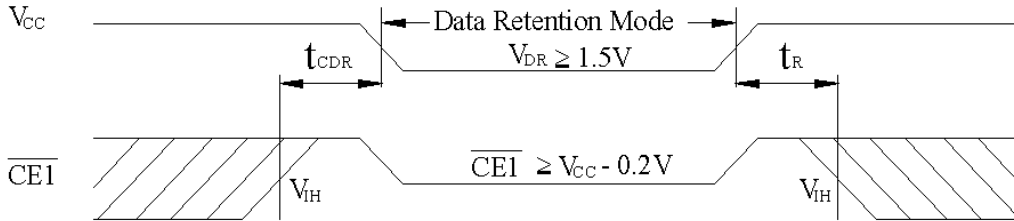
1. Typical characteristics are at TA = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Fmax = 1/t_{RC}.

■ DATA RETENTION CHARACTERISTICS (TA = 0 to + 70°C)

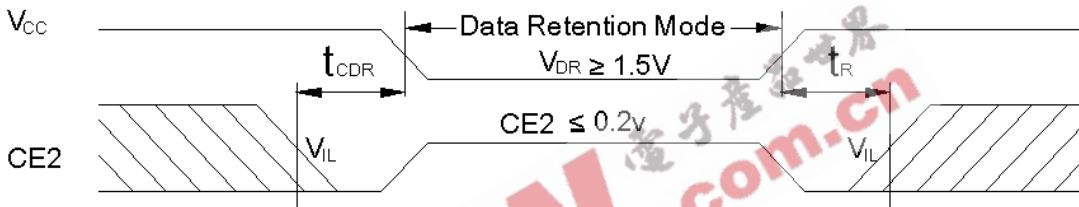
Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V _{DR}	V _{CC} for Data Retention	/CE ≥ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	1.5			V
I _{CCDR}	Data Retention Current	/CE ≥ V _{CC} -0.2V, V _{CC} =1.5V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V		0.3	2	uA
T _{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t _R	Operation Recovery Time		t _{RC} (1)			ns

1. Read Cycle Time.

■ **LOW V_{CC} DATA RETENTION WAVEFORM 1 (/CE1 Controlled)**



■ **LOW V_{CC} DATA RETENTION WAVEFORM 2 (CE2 Controlled)**



■ **AC TEST CONDITIONS**

Input Pulse Levels	V _{CC} /0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5V _{CC}
Output Load	See FIGURE 1A and 1B

■ **KEY TO SWITCHING WAVEFORMS**

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

■ AC TEST LOADS AND WAVEFORMS

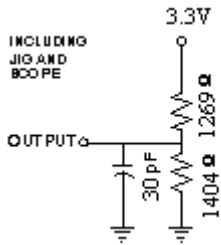


FIGURE 1A

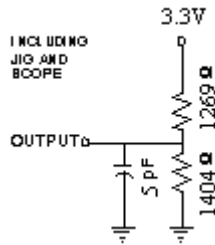
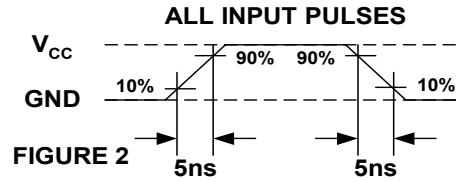


FIGURE 1B



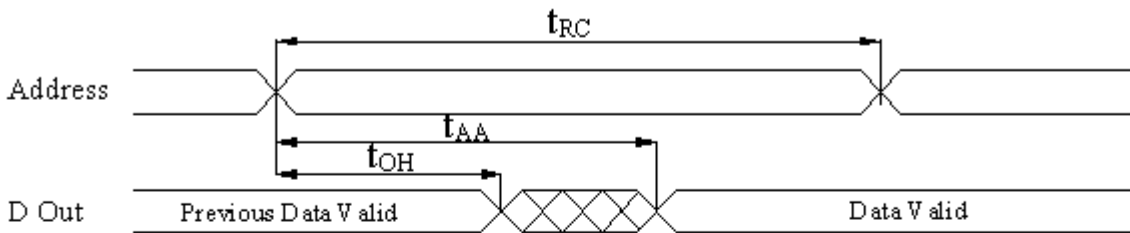
■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to +70°C, Vcc = 3.3V)

< READ CYCLE >

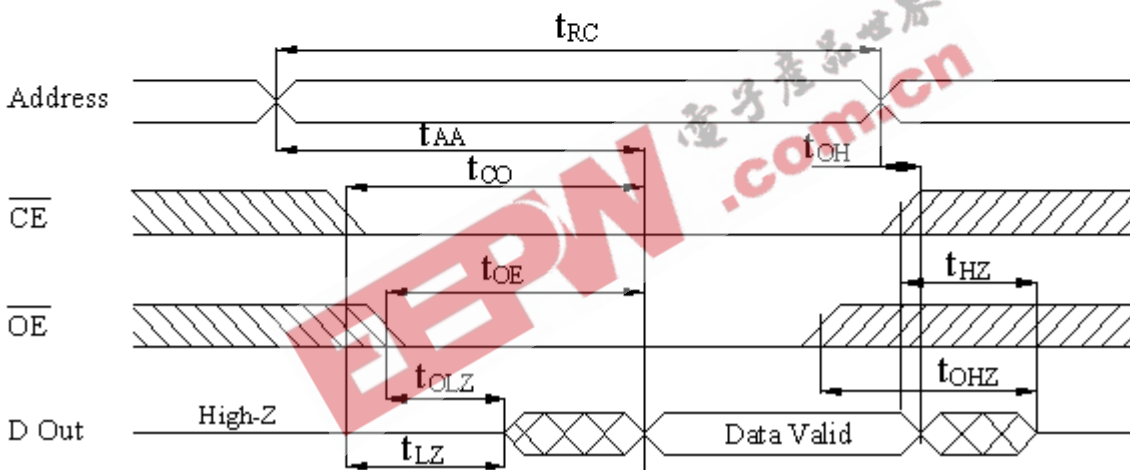
JEDEC Parameter Name	Parameter Name	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t _{AVAX}	t _{RC}	Read Cycle Time	55		70		ns
t _{AVQV}	t _{AA}	Address Access Time		55		70	ns
t _{ELQV}	t _{CO}	Chip Select Access Time		55		70	ns
t _{GLQV}	t _{OE}	Output Enable to Output Valid		25		35	ns
t _{ELQX}	t _{LZ}	Chip Select to Output Low Z	10		10		ns
t _{GLQX}	t _{OLZ}	Output Enable to Output in Low Z	5		5		ns
t _{EHQZ}	t _{CHZ}	Chip Deselect to Output in High Z	0	20	0	25	ns
t _{GHQZ}	t _{OHZ}	Output Disable to Output in High Z	0	20	0	25	ns
t _{AXOX}	t _{OH}	Out Disable to Address Change	10		10		ns

■ SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE 1.



READ CYCLE 2.



NOTES:

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.



High Speed Super Low Power SRAM

256K-Word By 8 Bit

CS18LV20483

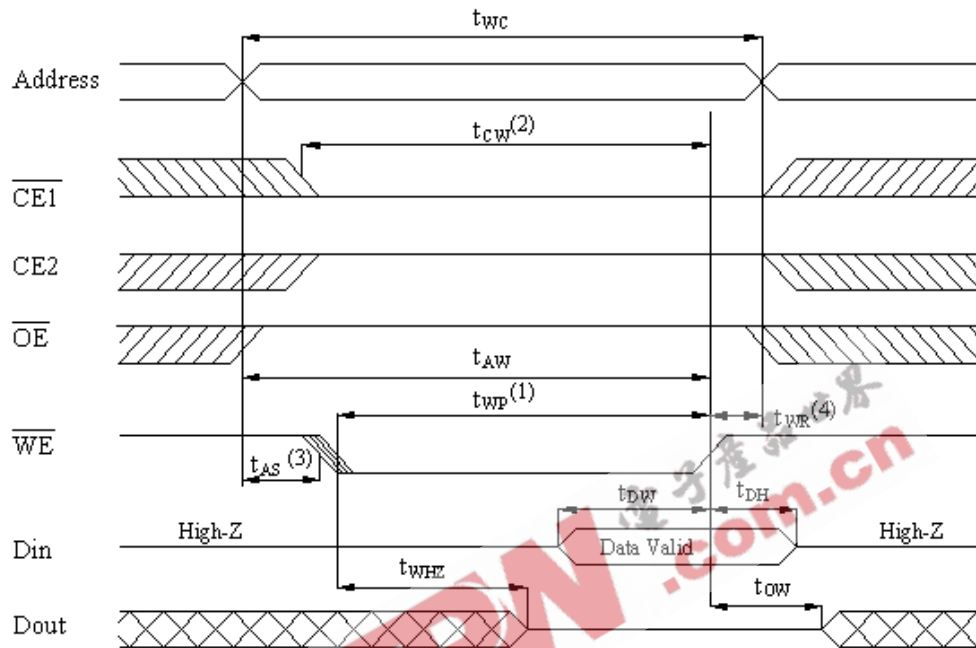
■ AC ELECTRICAL CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{V}$)

< WRITE CYCLE >

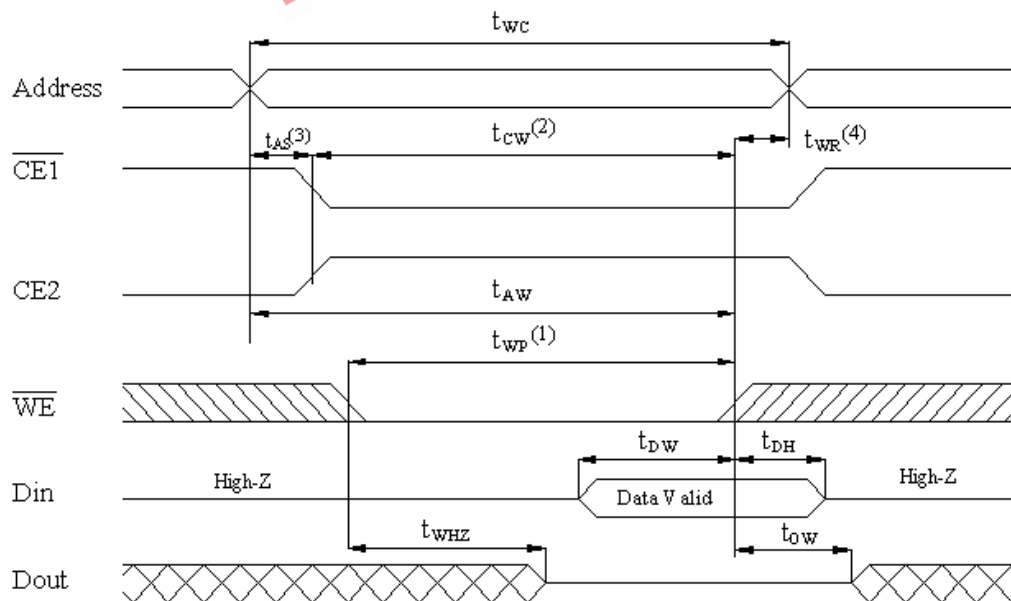
JEDEC Parameter Name	Parameter Name	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	45		60		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time	0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		20		20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25		30		ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		0		ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1. (\overline{WE} controlled)



WRITE CYCLE 2. ($\overline{CE1}$ and $\overline{CE2}$ Controlled)

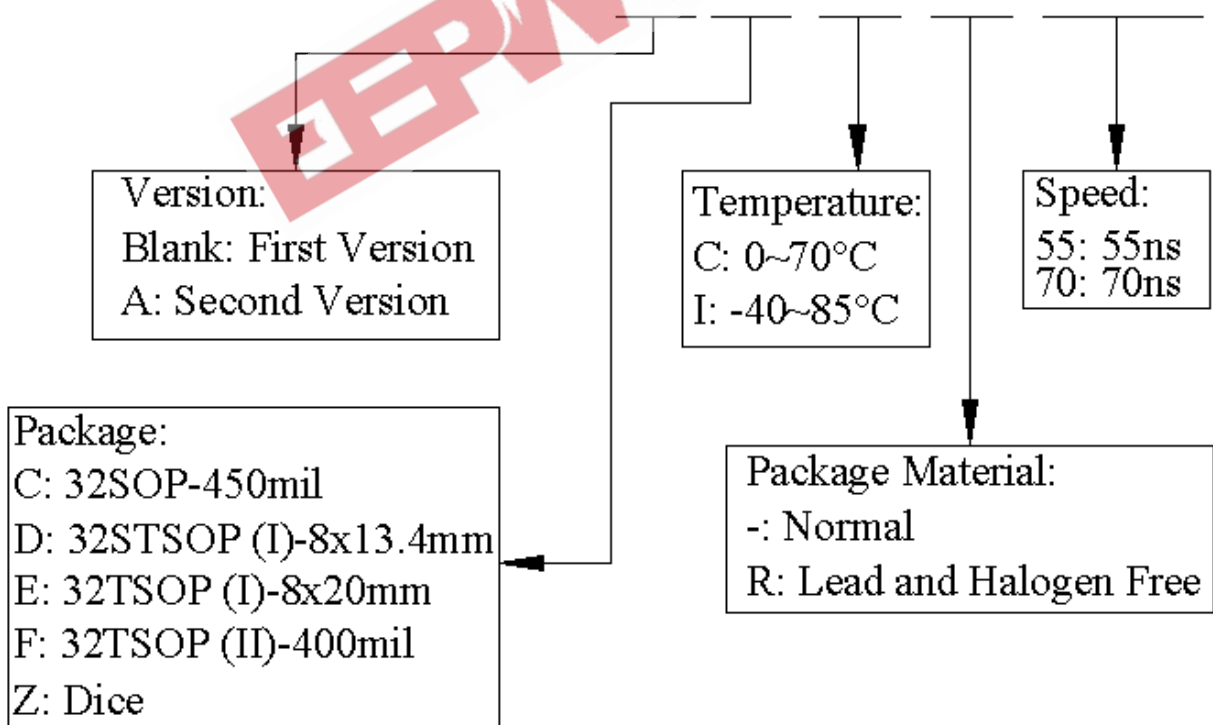


NOTES:

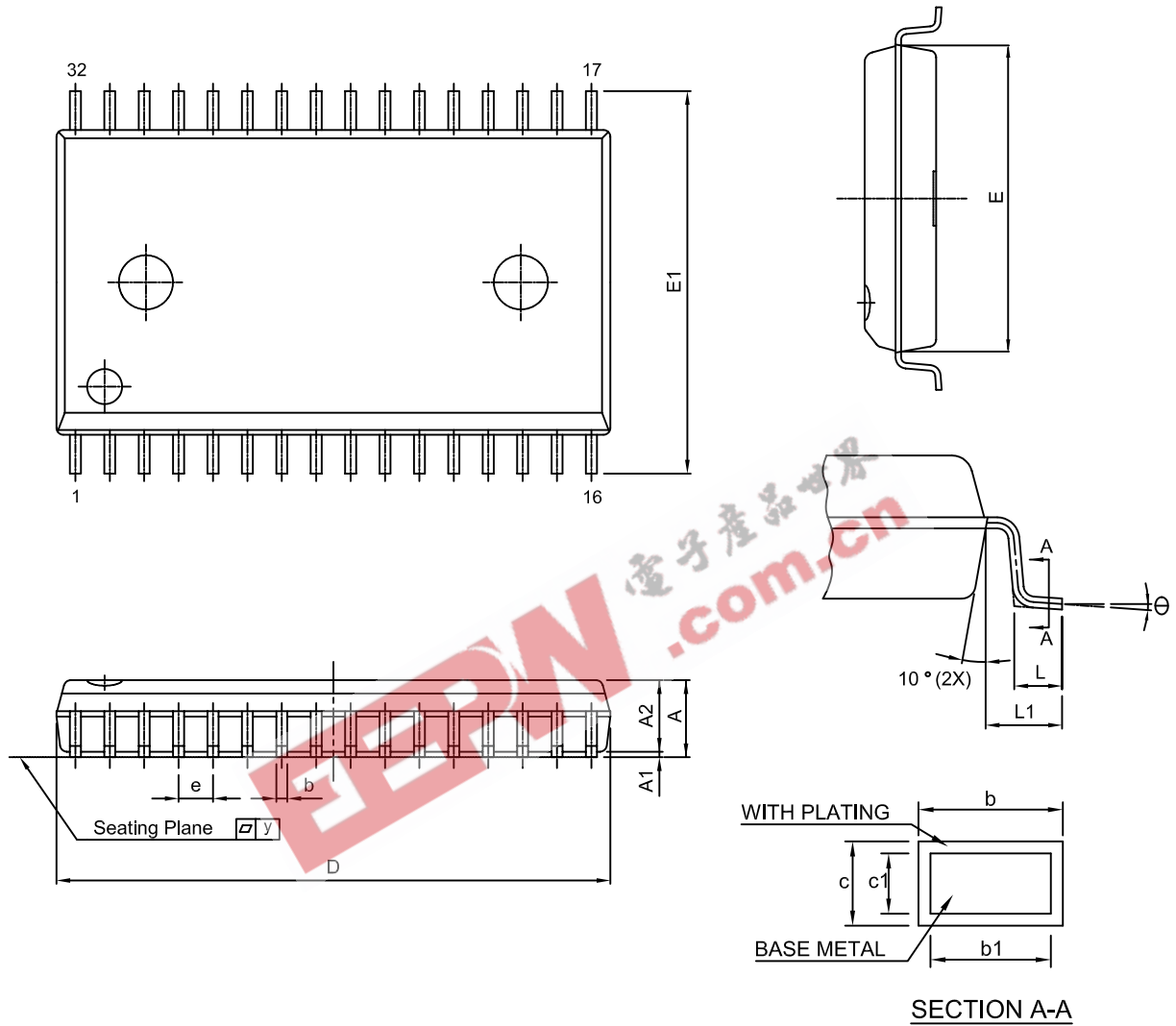
1. A write occurs during the overlap(t_{WP}) of low $/CE1$, a high $CE2$ and low $/WE$. A write begins when $/CE1$ goes low, $CE2$ going high and $/WE$ goes low. A write ends at the earliest transition when $/CE1$ goes high, $CE2$ goes high and $/WE$ goes high. The t_{WP} is measured from the beginning of the write to the end of write.
2. t_{CW} is measured from the $/CE1$ going low or $CE2$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. T_{WR} applied in case a write ends as $/CE1$ or $/WE$ going high or $CE2$ going low.

■ **ORDER INFORMATION**

CS18LV20483



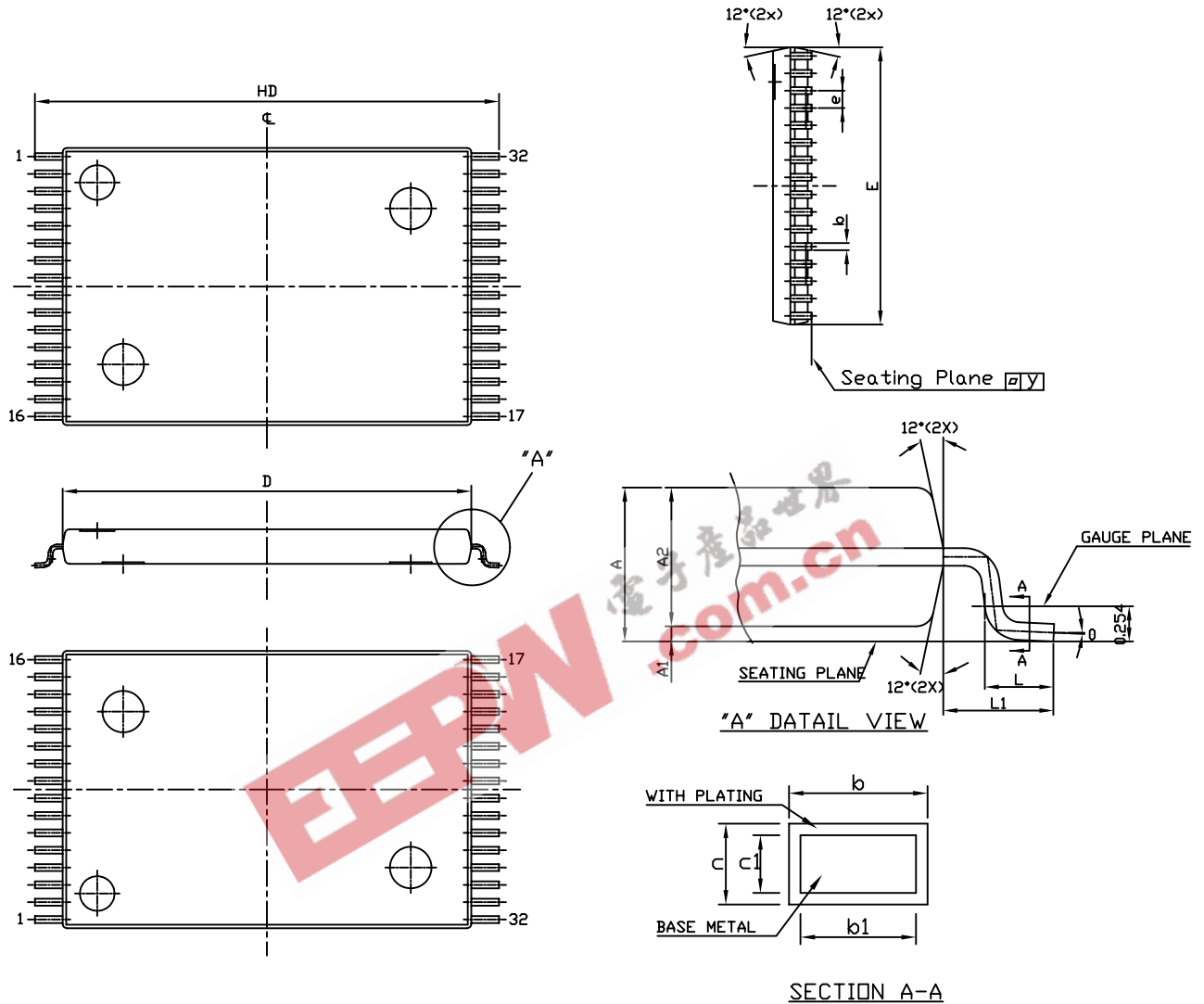
■ PACKAGE DIMENSIONS - 32L SOP 450 mil



SECTION A-A

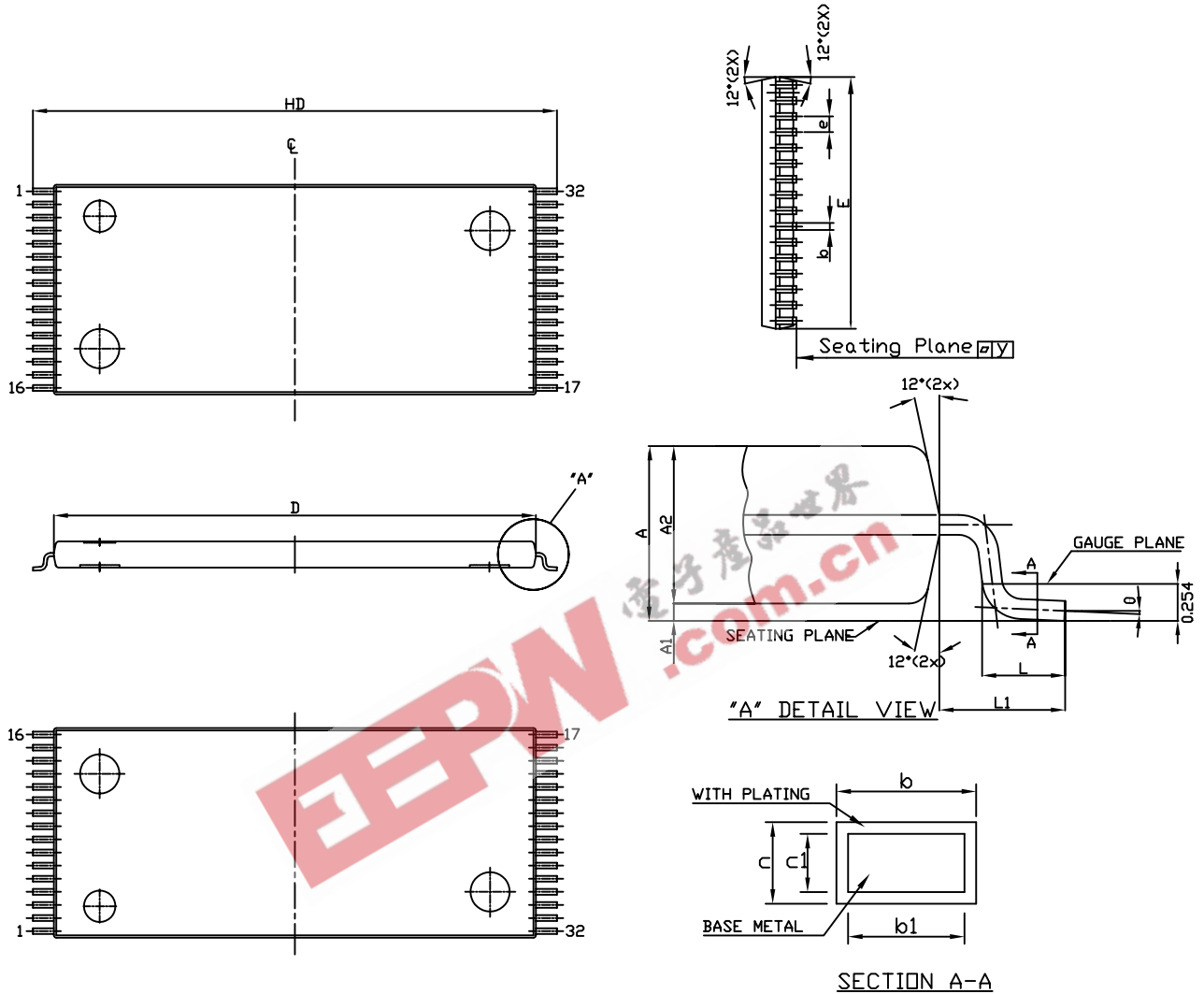
SYMBOL UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
	mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.176	13.792	1.118	0.584	1.194	—
Nom.		2.821	0.229	2.680	—	—	—	—	20.447	11.303	14.097	1.270	0.834	1.397	—	—
Max.		2.997	0.356	2.820	0.50	0.46	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.600	0.1	10°
inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	—	0°
	Nom.	0.111	0.009	0.1055	—	—	—	—	0.805	0.445	0.555	0.050	0.033	0.055	—	—
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

■ PACKAGE DIMENSIONS: 32L STSOP 1-8x13.4mm



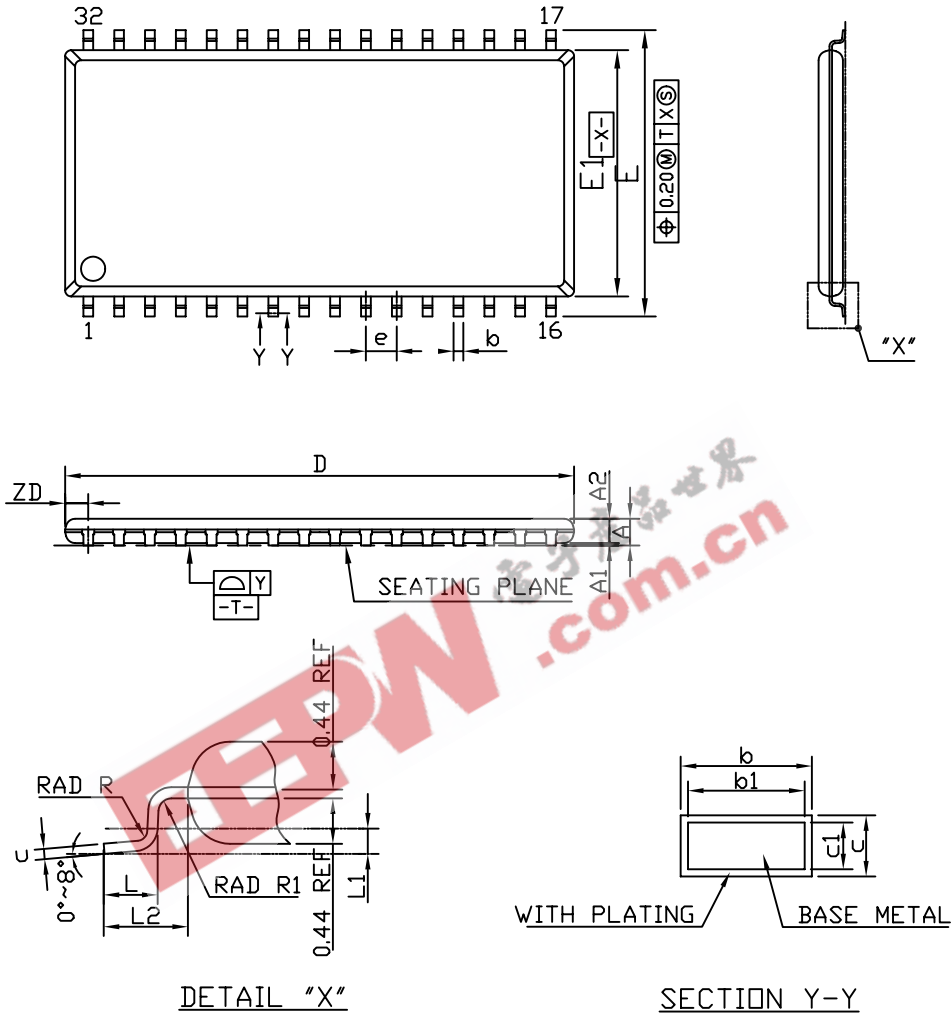
SYMBOL		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
UNIT																
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.40	13.20	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	-	-	11.80	8.00	0.50	13.40	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.60	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.016	0.520	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	-	-	0.465	0.315	0.020	0.528	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.024	0.536	0.0277	0.0355	0.004	8°

■ PACKAGE DIMENSIONS: 32L TSOP 1-8x20mm



SYMBOL		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
UNIT																
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	18.30	7.90	0.40	19.80	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	-	-	18.40	8.00	0.50	20.00	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	-	-	0.724	0.315	0.020	0.787	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004	8°

■ PACKAGE DIMENSIONS: 32L TSOP 2-400mil



SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	L2	R	R1	ZD	Y
UNIT																			
mm	Min.	-	0.05	0.95	0.30	0.30	0.12	0.10	20.82	11.56	10.03		0.40			0.12	0.12		-
	Nom.	-	0.10	1.00	-	0.40	-	0.127	20.95	11.76	10.16	1.27	0.50	0.25	0.8	-	-	0.95	-
	Max.	1.20	0.15	1.05	0.52	0.45	0.21	0.16	21.08	11.96	10.29	bsc	0.60	bsc	ref	0.25	-	ref	0.10
inch	Min.	-	0.002	0.037	0.012	0.012	0.005	0.004	0.820	0.455	0.394		0.016			0.005	0.005		-
	Nom.	-	0.004	0.039	-	0.016	-	0.005	0.825	0.463	0.400	0.050	0.020	0.010	0.031	-	-	0.037	-
	Max.	0.047	0.006	0.042	0.020	0.018	0.008	0.006	0.830	0.471	0.405	bsc	0.024	bsc	ref	0.010	-	ref	0.004