

**SONY®**

# CXA1114P/M/CXA1434P

## Audio Video Switch Compatible with I<sup>2</sup>C Bus

### Description

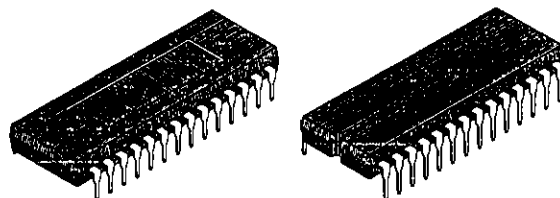
The CXA1114P and CXA1434P are bipolar ICs developed as audio video switches for the I<sup>2</sup>C bus.

### Features

- Serial control through I<sup>2</sup>C bus
- 4 channels for input and 3 channels for output
- The 3 channels for output are respectively independent and allow for input selection at will
- Video and audio switches are independently controllable
- Corresponds to mutual dubbing and simultaneous broadcasting
- Built-in amplifier with gain = 6 dB for both video and audio systems
- Wide band video amplifier (15 MHz – 3dB)
- Slave address for CXA1114 and CXA1434 differ  
CXA1114: 90H, CXA1434: 96H

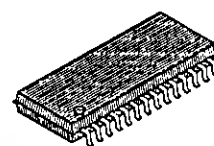
CXA1114P  
CXA1434P

28pin DIP (Plastic)



CXA1114M

28pin SOP (Plastic)



### Functions

Input channels { Video input 4 channels  
                  { Audio input, STEREO 4 channels  
Output channels { Video output 3 channels  
                  { Audio output, STEREO 3 channels

Each output features a built-in 6dB gain amplifier.

Output at the 3 channels can independently select an input at will.

### Structure

Bipolar silicon monolithic IC

### Absolute Maximum Ratings (Ta=25°C)

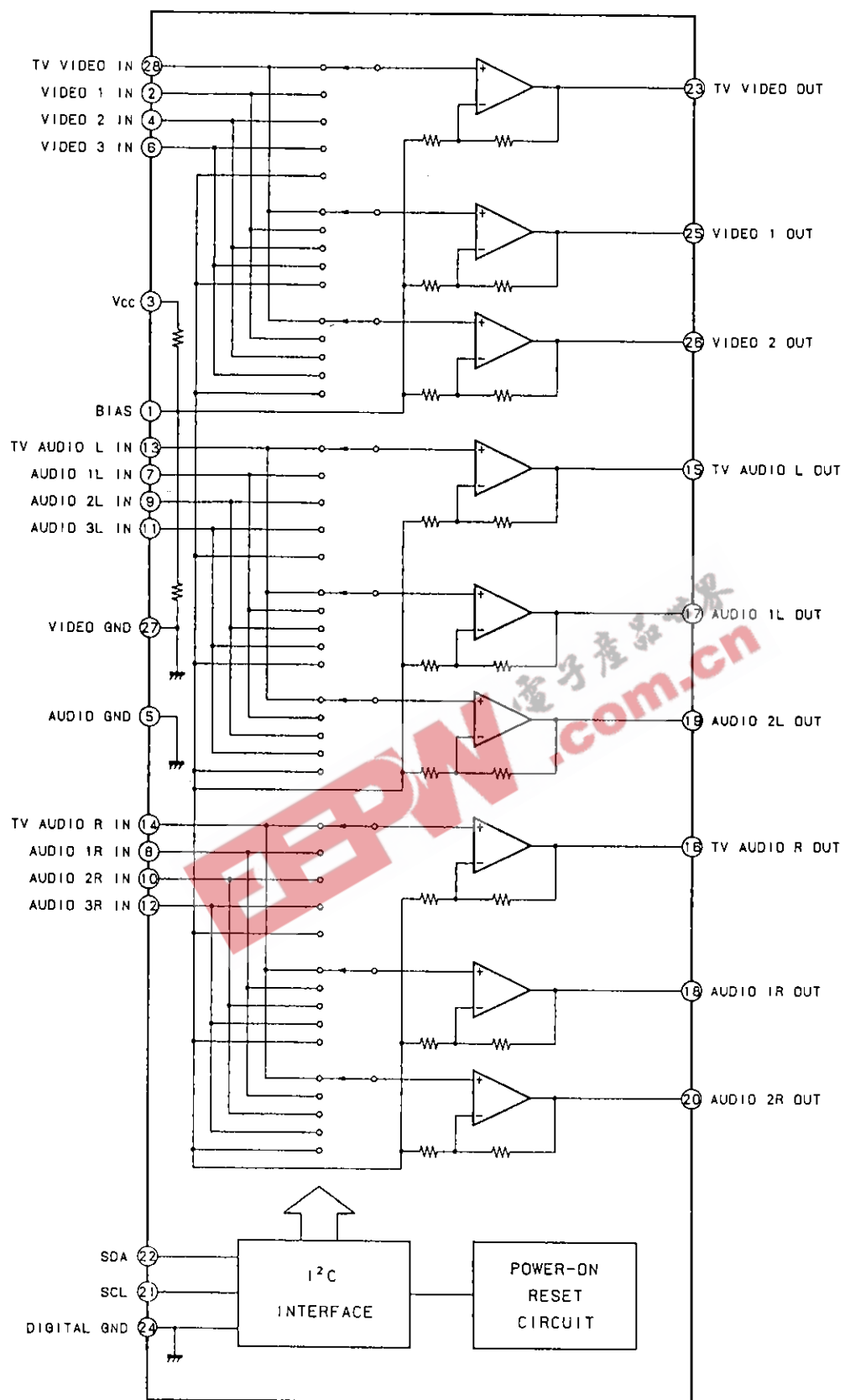
- |                               |      |             |                        |
|-------------------------------|------|-------------|------------------------|
| • Supply voltage              | Vcc  | 12          | V                      |
| • Operating temperature       | Topr | -20 to +75  | °C                     |
| • Storage temperature         | Tstg | -65 to +150 | °C                     |
| • Allowable power dissipation | Pd   | 830         | mW (CXA1114P/CXA1434P) |
|                               |      | 570         | mW (CXA1114M)          |

### Operating Supply Voltage Range

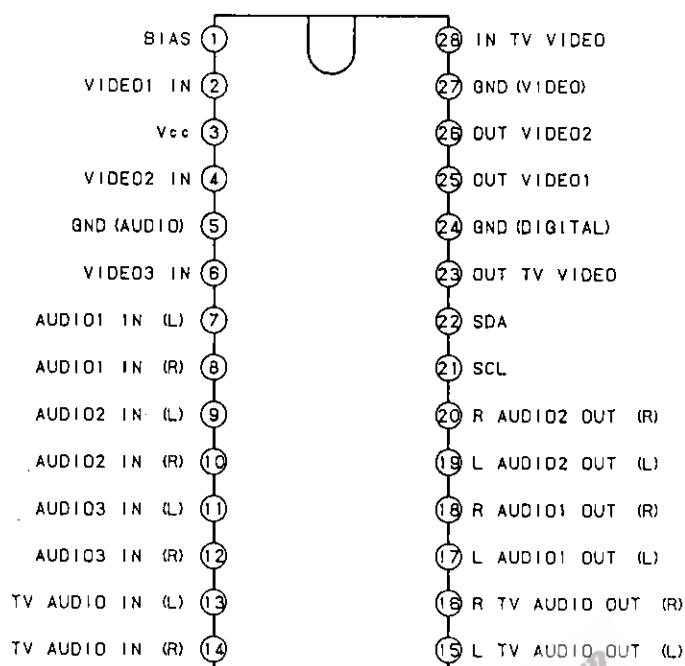
Vcc +8 to +10 V

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## Block Diagram



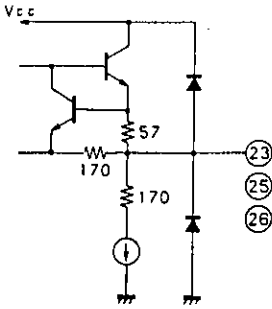
## Pin Configuration (Top View)



## Pin Description

| No.               | Symbol                                                | Voltage | Equivalent circuit | Description                                                                                                                                                                                                               |
|-------------------|-------------------------------------------------------|---------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                 | BIAS                                                  | 4.6V    |                    | Builds up $V_{cc}/2$ that becomes the internal bias reference. Supply ripple is suppressed by installing a capacitor. Cut off frequency is supplied through,<br>$f_0 = \frac{1000}{2\pi \times 11 \times C (\mu F)} [Hz]$ |
| 2<br>4<br>6<br>28 | VIDEO 1 IN<br>VIDEO 2 IN<br>VIDEO 3 IN<br>TV.VIDEO IN | 4.5V    |                    | Video 1, 2, 3, and TV video input pins                                                                                                                                                                                    |
| 3                 | $V_{cc}$                                              | 9.0V    |                    | Power supply pin                                                                                                                                                                                                          |

| No.                                       | Symbol                                                                                                                                 | Voltage | Equivalent circuit | Description                                                                                        |
|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|---------|--------------------|----------------------------------------------------------------------------------------------------|
| 5<br>24<br>27                             | GND(AUDIO)<br>GND(DIGITAL)<br>GND(VIDEO)                                                                                               |         |                    | Audio, digital and video GND pins                                                                  |
| 7<br>8<br>9<br>10<br>11<br>12<br>13<br>14 | AUDIO 1 IN(L)<br>AUDIO 1 IN(R)<br>AUDIO 2 IN(L)<br>AUDIO 2 IN(R)<br>AUDIO 3 IN(L)<br>AUDIO 3 IN(R)<br>TV AUDIO IN(L)<br>TV AUDIO IN(R) | 4.6V    |                    | Input pins for 1,2,3 audio, the TV audio and their respective L and R channels                     |
| 15<br>16<br>17<br>18<br>19<br>20          | TV AUDIO OUT(L)<br>TV AUDIO OUT(R)<br>AUDIO 1 OUT(L)<br>AUDIO 1 OUT(R)<br>AUDIO 2 OUT(L)<br>AUDIO 2 OUT(R)                             | 4.6V    |                    | Output pins for 1,2 audio, the TV audio and their respective L and R channels                      |
| 21                                        | SCL                                                                                                                                    | —       |                    | SCL (Serial Clock Line) of I <sup>2</sup> C bus standards. Threshold level is set to approx. 2.3V. |
| 22                                        | SDA                                                                                                                                    | —       |                    | SDA (Serial Data Line) of I <sup>2</sup> C bus standards. Threshold level is set to approx. 2.3V.  |

| No.            | Symbol                                     | Voltage | Equivalent circuit                                                                 | Description                                    |
|----------------|--------------------------------------------|---------|------------------------------------------------------------------------------------|------------------------------------------------|
| 23<br>25<br>26 | TV VIDEO OUT<br>VIDEO 1 OUT<br>VIDEO 2 OUT | 4.5V    |  | Output pins for TV video, video 1 and video 2. |

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## Electrical Characteristics

(Ta=25°C, Vcc=9V See Fig. 1 to 10)

| Item                | Symbol | Conditions                         | Min. | Typ. | Max. | Unit |
|---------------------|--------|------------------------------------|------|------|------|------|
| Consumption current | Icc    | Vcc=9V, No signal, No load (Fig.1) | 20   | 35   | 50   | mA   |
| BIAS                | Vcc/2  | Vcc=9V, No signal, No load         | 4.2  | 4.6  | 5.0  | V    |

## (Video system)

|                                 |       |                                                                                                                            |     |     |     |      |
|---------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| I/O pin voltage                 | Vvpin | Vcc=9V, No signal, No load                                                                                                 | 4.1 | 4.5 | 4.9 | V    |
| Frequency characteristics       | Fbwv  | With input at 0.3 Vp-p and output at 100 kHz set to 0 dB.<br>Test input frequency when output level reaches -3 dB. (Fig.2) | 10  | 15  | —   | MHz  |
| Gain                            | GVv   | f=100kHz, 0.3Vp-p input (Fig.2)                                                                                            | 5.5 | 6.0 | 6.5 | dB   |
| Input dynamic range             | Vdv   | At 100 kHz max input level when distortion < 1.0% (Fig.2)                                                                  | 2.0 | 3.0 | —   | Vp-p |
| Crosstalk between video outputs | Vctv  | f=4.43MHz, 1Vp-p input (Fig.2)                                                                                             | —   | -55 | -50 | dB   |
| Input resistance                | Rinv  | Tested at DC (Fig.5)                                                                                                       | 7   | 11  | 15  | kΩ   |
| Ripple rejection ratio          | RRv   | f=100Hz, 0.3Vp-p added to Vcc (Fig.7)                                                                                      | —   | -35 | -30 | dB   |
| Output impedance                | Ro v  | f=100kHz, 5Vp-p input (Fig.3)                                                                                              | —   | 12  | 30  | Ω    |

## (Audio system)

|                                 |       |                                                                                          |     |      |     |      |
|---------------------------------|-------|------------------------------------------------------------------------------------------|-----|------|-----|------|
| I/O pin voltage                 | Vapin | Vcc=9V, no signal, No load                                                               | 4.4 | 4.6  | 4.7 | V    |
| Frequency characteristics       | Fbwa  | With 1Vp-p input, 1kHz output as 0dB, an input frequency where -3dB is obtained. (Fig.9) | 100 | —    | —   | kHz  |
| Gain                            | Gva   | f=1kHz, 1Vp-p input (Fig.9)                                                              | 5.5 | 6.0  | 6.5 | dB   |
| Total harmonic distortion       | THD   | f=1kHz, 2.2Vp-p input (Fig.8)                                                            | —   | 0.06 | 0.2 | %    |
| Input dynamic range             | Vda   | At 1 kHz max input level when distortion < 1.0% (Fig.9)                                  | 2.8 | 3.0  | —   | Vp-p |
| Crosstalk between audio outputs | Vcta  | f=1kHz, 1Vp-p input (Fig.9)                                                              | —   | -90  | -75 | dB   |
| Input resistance                | Rina  | Tested at DC (Fig.6)                                                                     | 25  | 30   | 40  | kΩ   |
| Ripple rejection ratio          | RRa   | f=100Hz, 0.3Vp-p added to Vcc (Fig.7)                                                    | —   | -50  | -40 | dB   |
| Output impedance                | Ro a  | f=1kHz, 5Vp-p input (Fig.4)                                                              | —   | 12   | 30  | Ω    |

|                  |                  |                                                                                    |   |     |      |    |
|------------------|------------------|------------------------------------------------------------------------------------|---|-----|------|----|
| Output DC offset | V <sub>off</sub> | Offset with regards to mute in respective modes. (Fig.9)                           | — | 6.0 | 25.0 | mV |
| Residual noise   | V <sub>na</sub>  | f <sub>CL</sub> =300Hz, f <sub>CH</sub> =19kHz, 40dB amplifier connected. (Fig.10) | — | 0.8 | 5.0  | mV |

(Logic system) Fig.11

|                                              |                     |                         |     |   |     |     |
|----------------------------------------------|---------------------|-------------------------|-----|---|-----|-----|
| High level input voltage                     | V <sub>IH</sub>     |                         | 3.0 | — | 5.0 | V   |
| Low level input voltage                      | V <sub>IL</sub>     |                         | 0   | — | 1.5 | V   |
| Low level output voltage                     | V <sub>OL</sub>     | During SDA, 3mA flow in | 0   | — | 0.4 | V   |
| Clock frequency                              | f <sub>SCL</sub>    |                         | 0   | — | 100 | kHz |
| Min. waiting time for data modification      | t <sub>BUF</sub>    |                         | 4.7 | — | —   | μs  |
| Min. waiting time for start of data transfer | t <sub>HD;STA</sub> |                         | 4.0 | — | —   | μs  |
| Low level clock pulse width                  | t <sub>LOW</sub>    |                         | 4.7 | — | —   | μs  |
| High level clock pulse width                 | t <sub>HIGH</sub>   |                         | 4.0 | — | —   | μs  |
| Min. waiting time for start preparation      | t <sub>SU;STA</sub> |                         | 4.7 | — | —   | μs  |
| Min. data hold time                          | t <sub>HD;DAT</sub> |                         | 5   | — | —   | μs  |
| Min. data preparation time                   | t <sub>SU;DAT</sub> |                         | 250 | — | —   | ns  |
| Rise time                                    | t <sub>R</sub>      |                         | —   | — | 1   | μs  |
| Fall time                                    | t <sub>F</sub>      |                         | —   | — | 300 | ns  |
| Min. stop reparation time                    | t <sub>SU;STO</sub> |                         | 4.7 | — | —   | μs  |

Electrical Characteristics Test Circuit

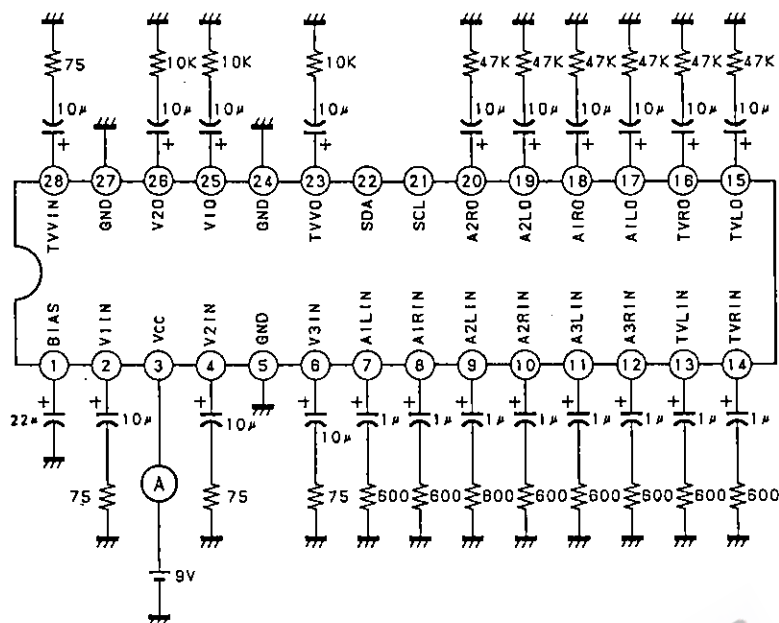


Fig. 1

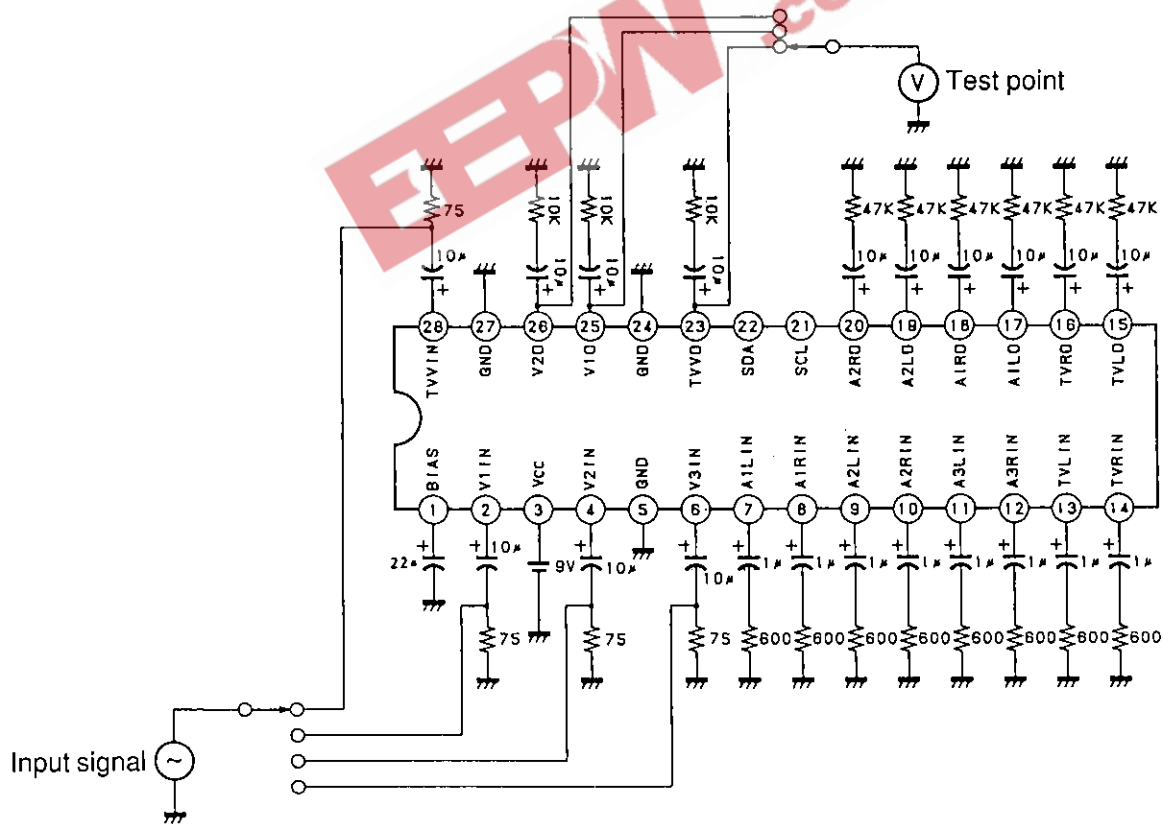


Fig. 2

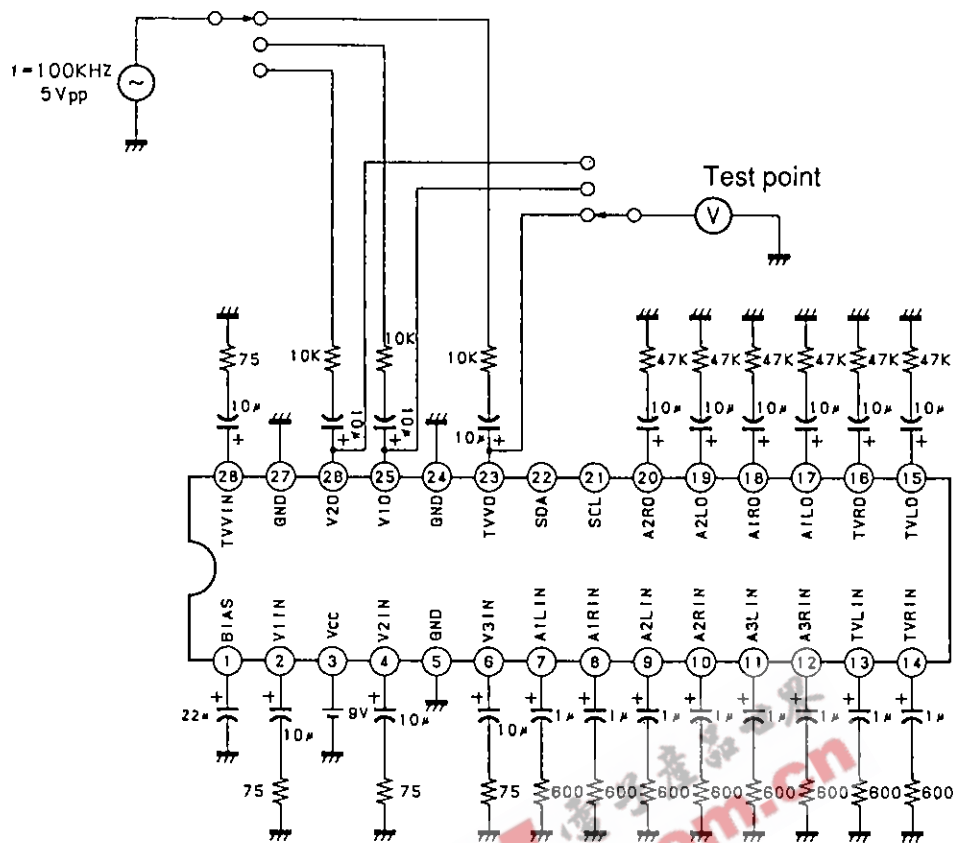


Fig. 3

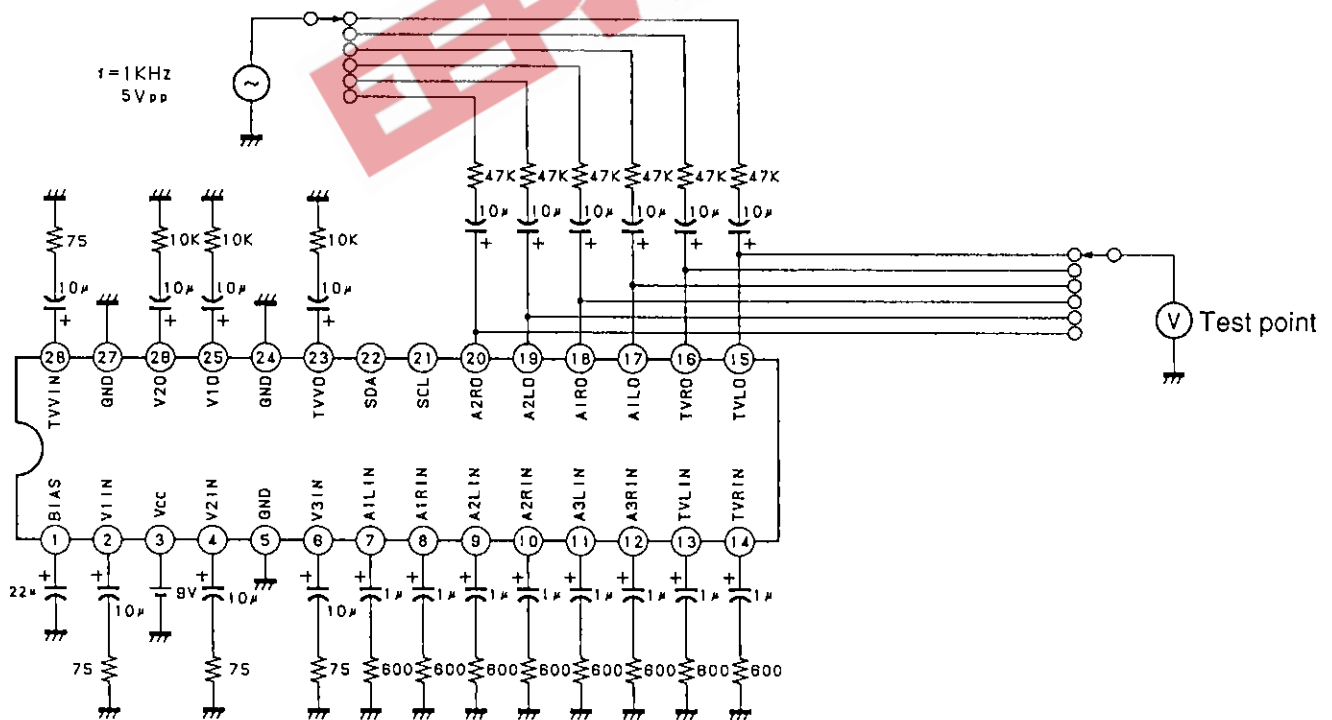


Fig. 4

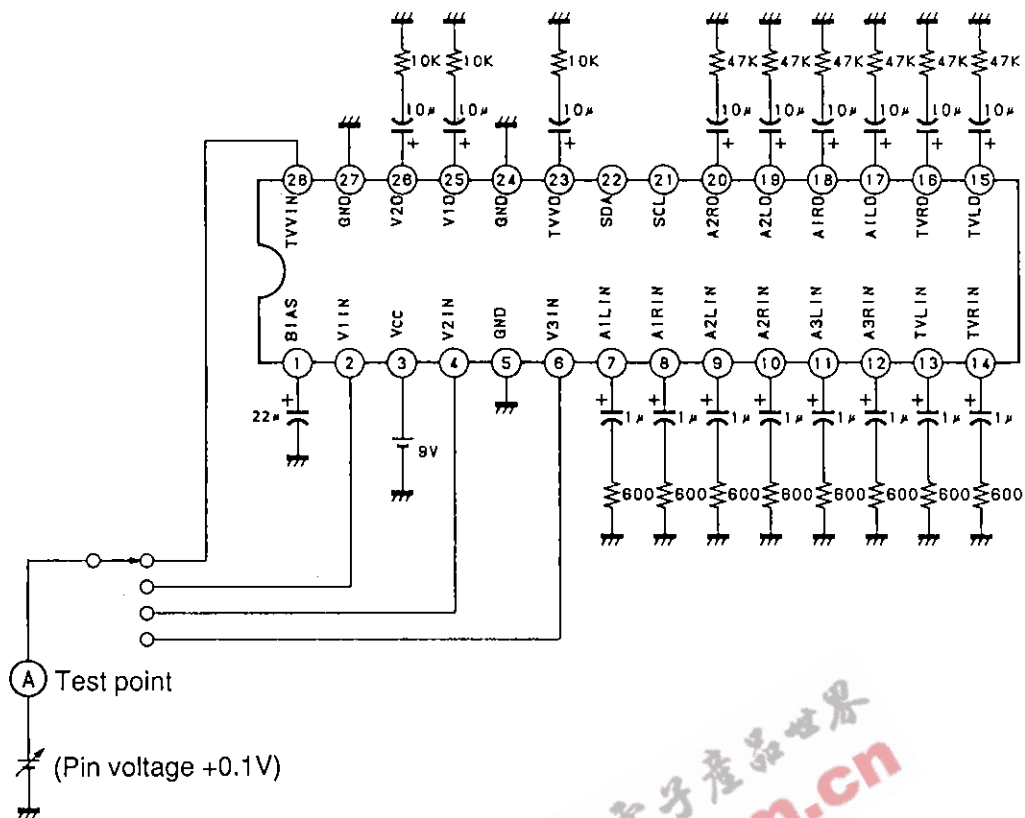


Fig. 5

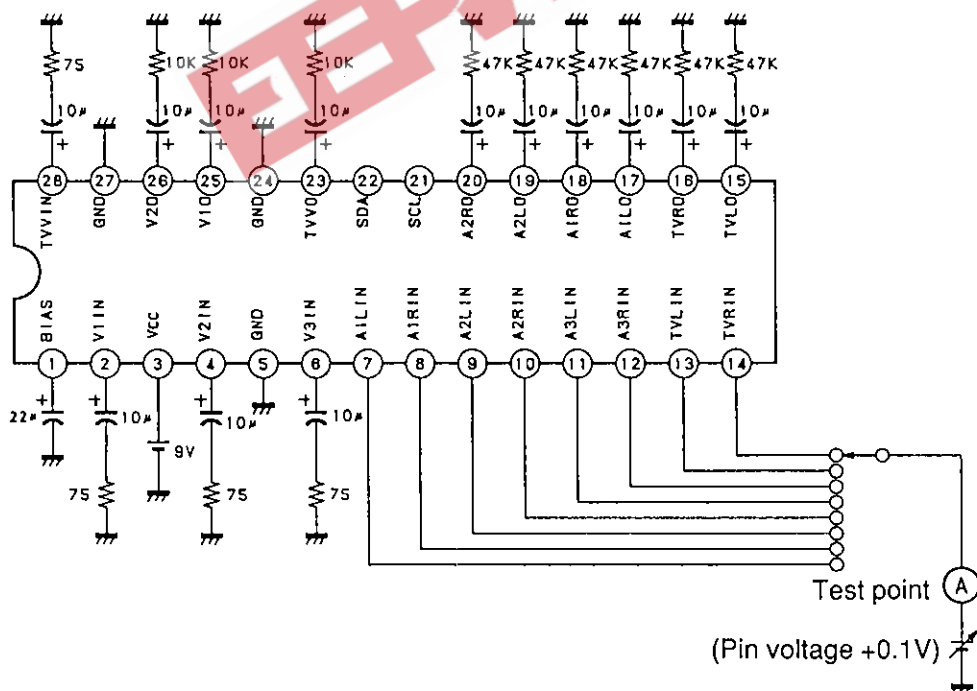


Fig. 6





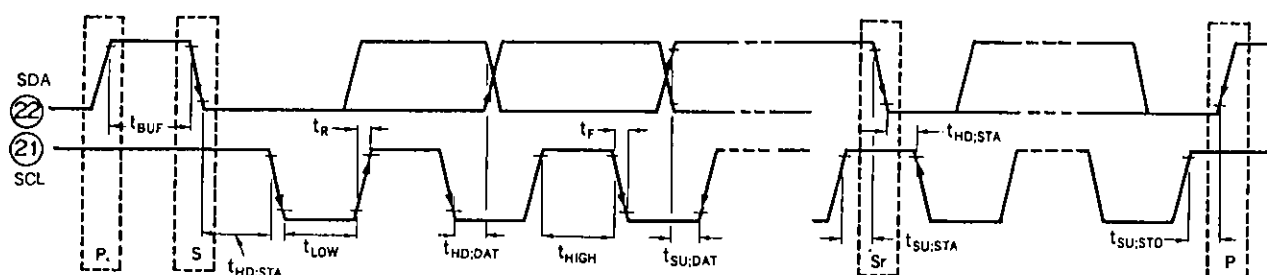
I<sup>2</sup>C BUS Control signal

Fig. 11

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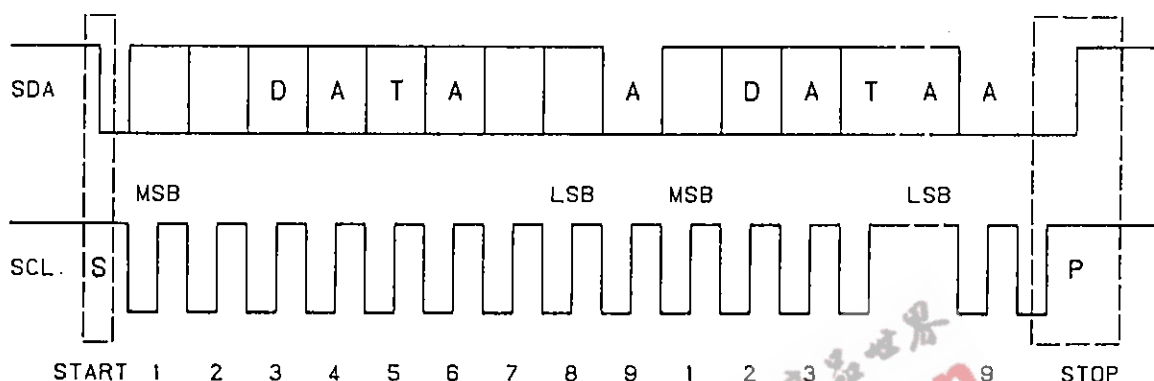
## Operation

The CXA1114 and CXA1434 are used for audio and video selection. These IC's feature 4 channels for video input, 4 for audio stereo input, 3 channels for video output and 3 for audio stereo output. Respective outputs have built-in amplifiers of approx. 6dB.

The respective audio and video outputs (L and R channels make a set) can independently select the desired input. This is executed through I<sup>2</sup>C bus.

### 1) I<sup>2</sup>C Bus

The I<sup>2</sup>C bus (Inter IC bus) is a bus system inside the equipment developed by Philips. Start, Stop, Data transfer, Sync and Collision prevention can be executed through two lines, SDA and SCL. The output of respective ICs is either an open collector or an open drain shaped into a wired OR to form the bus line. The bus signal structure is shown below.



S:Start Condition...High to Low transition of SDA when SCL is at High.

P:Stop Condition...Low to High transition of SDA when SCL is at High.

A:Acknowledge...Reply signal coming from slave.

Data is transferred by MSB first. 8 bits in one unit. After that acknowledge (A) is set on to confirm the signal from slave. Normally slave \*<sup>1</sup> ICs take in data with the rising edge of SCL while Master \*<sup>2</sup> ICs change data with the falling edge of SCL. The actual data format of CXA1114 and CXA1434 is shown below.

|   |                          |   |       |   |       |   |       |   |   |
|---|--------------------------|---|-------|---|-------|---|-------|---|---|
| S | Slave address<br>90H/96H | A | DATA0 | A | DATA1 | A | DATA2 | A | P |
|---|--------------------------|---|-------|---|-------|---|-------|---|---|

Slave address is proper to the IC and is assigned to each IC according to its functions. From the 8 bits the upper 7 bits are proper addresses while the last bit is allocated to R/W. This R/W bit turns to Read \*<sup>3</sup> at 1 and Write \*<sup>4</sup> at 0. For the CXA1114/CXA1434, 90H and 96H are assigned as slave addresses. (Write only as there is no Read mode.)

\*<sup>1</sup> Slave: ICs controlled by the Master. Normally all ICs except microcomputers are slaves.

\*<sup>2</sup> Master: Indicates ICs that control, such as microcomputers and the like.

\*<sup>3</sup> Read: Mode in which Master reads out data from Slave.

\*<sup>4</sup> Write: Mode in which data is written out from Master to Slave.

## 2) Control

The CXA1114/CXA1434 control is performed by writing 3 bytes of data into 3 control registers composed of 8 bits (actually 6 bits since 2 bits are empty) that control the output selection of 3 systems. First byte data performs the input selection of TV OUT, second byte data that of VIDEO1 OUT and third byte data that of VIDEO 2OUT, respectively. Slave address for CXA1114/CXA1434 is 90H/96H in write mode only.

|   |                          |   |       |   |       |   |       |   |   |
|---|--------------------------|---|-------|---|-------|---|-------|---|---|
| S | Slave address<br>90H/96H | A | DATA0 | A | DATA1 | A | DATA2 | A | P |
|---|--------------------------|---|-------|---|-------|---|-------|---|---|

S: Start condition

A: Acknowledge emitted by slave (CXA1114/CXA1434)

P: Stop condition

### Structure of Respective Control Registers (DATA 0 to 2)

|    |    |     |     |    |    |     |     |
|----|----|-----|-----|----|----|-----|-----|
| b7 | b6 | b5  | b4  | b3 | b2 | b1  | b0  |
| x  | VM | VS1 | VS0 | x  | AM | AS1 | AS0 |

\* b7, b3 undefined

\* At Power On all bits turn to "0".  
(Power On Reset function)

#### Video switch control

| VM | VS1 | VS0 | Output pin      |
|----|-----|-----|-----------------|
| 0  | x   | x   | Mute (blanking) |
| 1  | 0   | 0   | TV VIDEO IN     |
| 1  | 0   | 1   | VIDEO 1 IN      |
| 1  | 1   | 0   | VIDEO2 IN       |
| 1  | 1   | 1   | VIDEO3 IN       |

#### Audio switch control

| AM | AS1 | AS0 | Output pin  |
|----|-----|-----|-------------|
| 0  | x   | x   | Mute        |
| 1  | 0   | 0   | TV AUDIO IN |
| 1  | 0   | 1   | AUDIO1 IN   |
| 1  | 1   | 0   | AUDIO2 IN   |
| 1  | 1   | 1   | AUDIO3 IN   |

## 3) Control Data Example

| Input selection          |          | Video input | Audio input   |
|--------------------------|----------|-------------|---------------|
| Output pin               |          |             |               |
| TV-Video<br>TV sound     | } output | Video 1     | TV sound      |
| Video 1<br>Video 1 sound | } output | Video 2     | Video 1 sound |
| Video 2<br>Video 2 sound | } output | Video 3     | Video 2 sound |

To select the above the control codes to be used are

|                          |          |     |     |                |
|--------------------------|----------|-----|-----|----------------|
| TV-Video<br>TV sound     | } output | 101 | 100 | } control code |
| Video 1<br>Video 1 sound | } output | 110 | 101 |                |
| Video 2<br>Video 2 sound | } output | 111 | 110 |                |

For the I<sup>2</sup>C bus, after the slave address 90H/96H for CXA1114/ CXA1434, the 3 bytes data transfer is performed:  
(x bit is not defined. Either 1 or 0 will do.)

$\times 101 \times 100$        $\times 110 \times 101$        $\times 111 \times 110$   
 first byte      second byte      third byte

That is for CXA1114    90H, 54H, 65H, 76H (When x=0)  
                               90H, DC<sub>H</sub>, ED<sub>H</sub>, FE<sub>H</sub> (When x=1)  
 or for CXA1434        96H, 54H, 65H, 76H (When x=0)  
                               96H, DC<sub>H</sub>, ED<sub>H</sub>, FE<sub>H</sub> (When x=1)  
 either can be transferred.



## Notes on Operations

As these ICs utilize video, audio and digital signals, the following points should be taken into consideration.

- 1) On both video and audio systems, the wiring may cause crosstalk. An effective measure would be to separate input by using an earth line on the P.C.B.
- 2) When control is performed through I<sup>2</sup>C bus, once it is set on, as long as there is no change in the data (with Power OFF, it is called off however), the condition at which it is set, is kept on. To avoid noise caused by SCL, SDA clocks and data transfer, it is recommended to temporarily stop the master, except during input selection.
- 3) Pin 1 provides bias. By installing a capacitor here and effective suppression of power supply ripple is obtained.

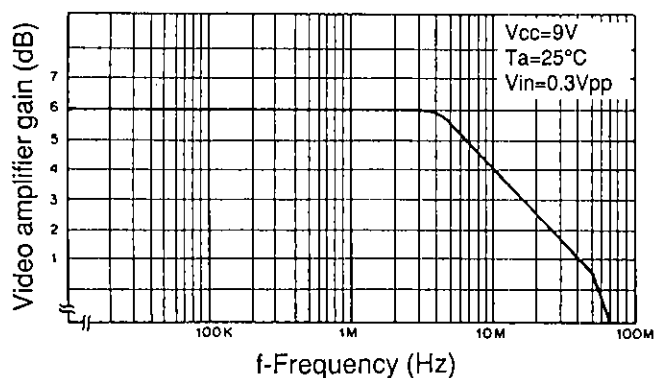
Here the cut off frequency obtained is 
$$f_0 = \frac{1000}{2\pi \times 11 \times C (\mu F)} \text{ [Hz]}$$

- 4) Keep the bypass capacitor for the power supply near Pin 3.

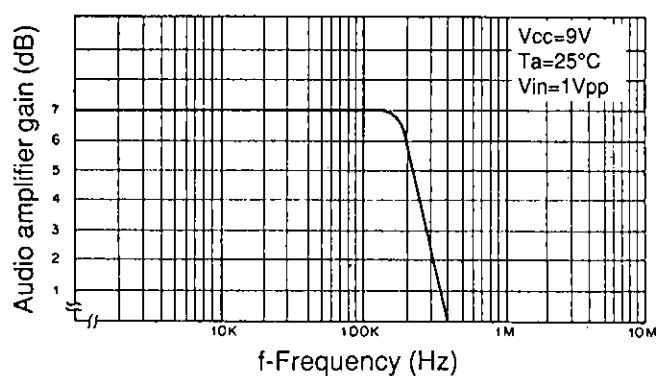
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## Characteristics Diagram

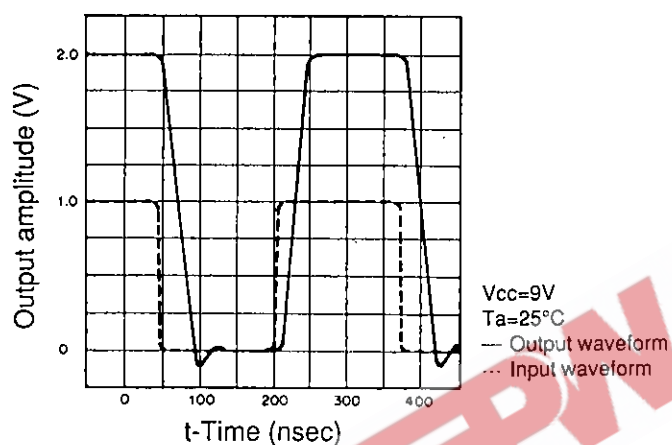
Video amplifier gain vs. Frequency



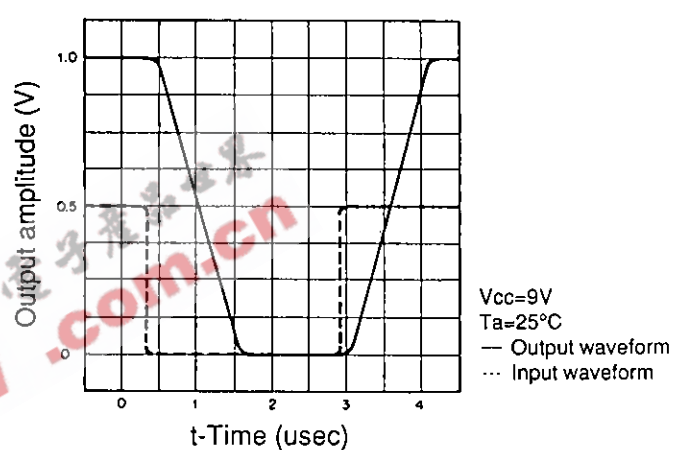
Audio amplifier gain vs. Frequency



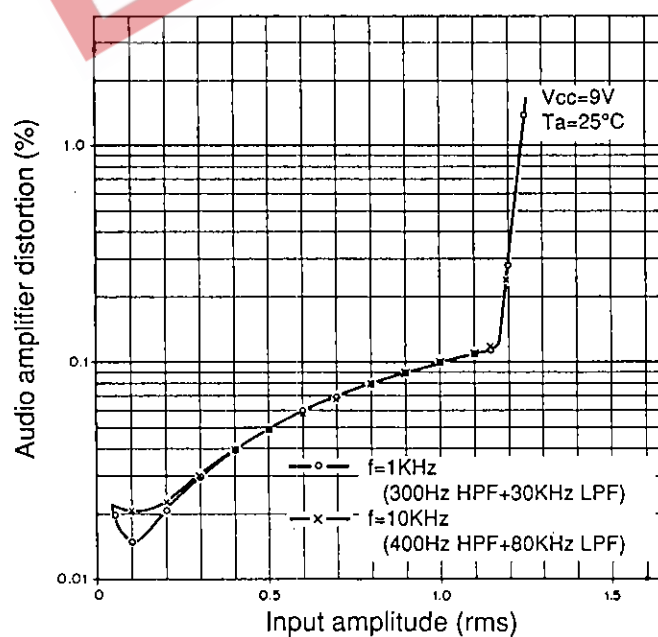
Video amplifier output vs. Rectangular wave input



Audio amplifier output vs. Rectangular wave input



Audio amplifier distortion vs. Input amplitude



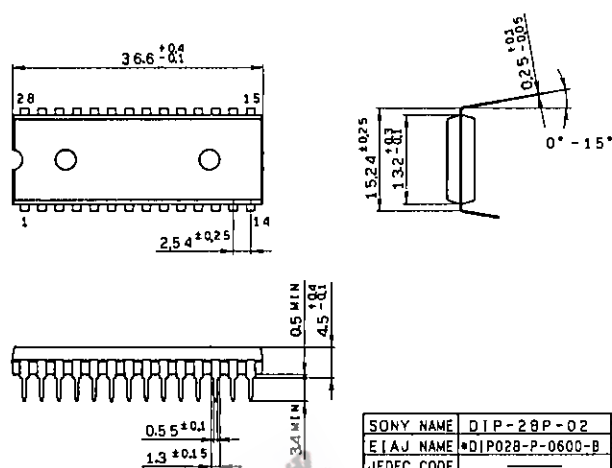
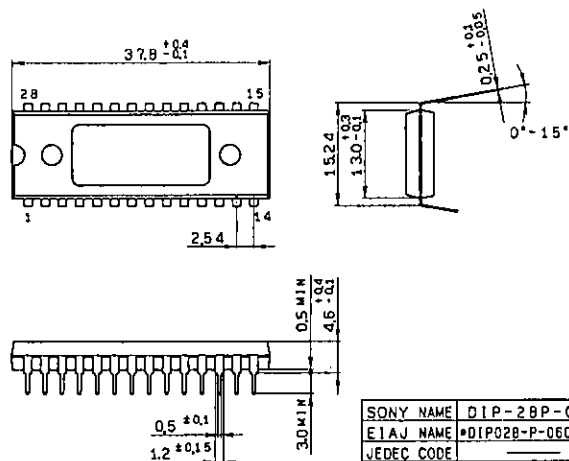
Package Outline Unit: mm

CXA1114P

CXA1434P

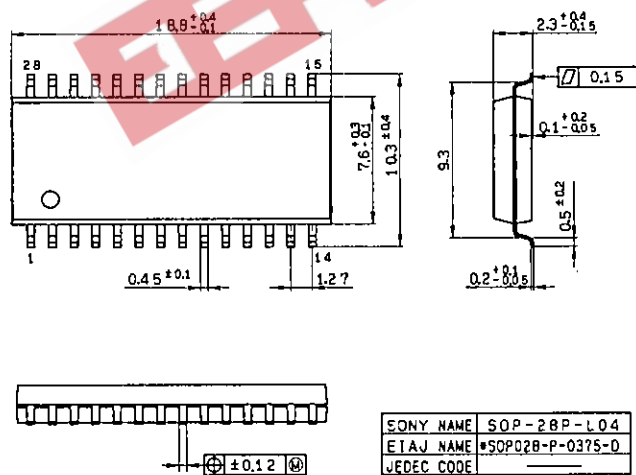
28pin DIP (Plastic) 600mil 4.2g

28pin DIP (Plastic) 600mil 4.0g



CXA1114M

28pin SOP (Plastic) 375mil 0.7g



Purchase of Sony's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.