SONY

CXA2055P

Preamplifier for High Resolution Computer Display

Description

The CXA2055P is a bipolar IC developed for high resolution computer displays.

Features

- Built-in wide band amplifier
  (130 MHz/–3 dB typ.@4 Vp-p)
- Input dynamic range : 1.0 Vp-p (typ.)
- R, G and B in a single package
- I²C bus control
  - Contrast control
  - Subcontrast control
  - Brightness control
  - OSD contrast control
  - Power save function
  - Input clamp pulse polarity selection
  - Output composite sync polarity selection
  - 5-channel, 8-bit D/A
  - Blanking level control
- Built-in sync separator (G channel only)
- Built-in blanking mixing function
- Built-in OSD mixing function
- Built-in ABL function
- Video interval detection function

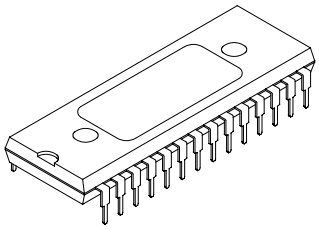
Applications

High resolution computer displays

Structure

Bipolar silicon monolithic IC

28 pin DIP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

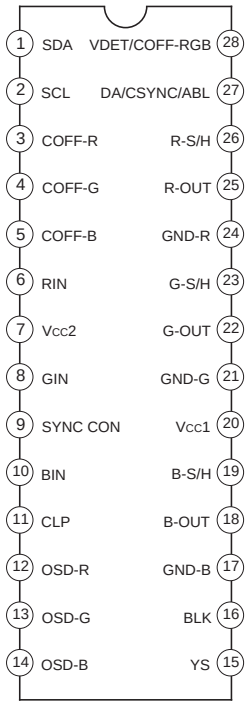
• Supply voltage	V_{CC}	14	V
• Operating temperature	T_{opr}	–20 to +75	°C
• Storage temperature	T_{stg}	–65 to +150	°C
• Allowable power dissipation	P_D	1794	mW

(when mounted on a 11.5 cm × 12.0 cm substrate)

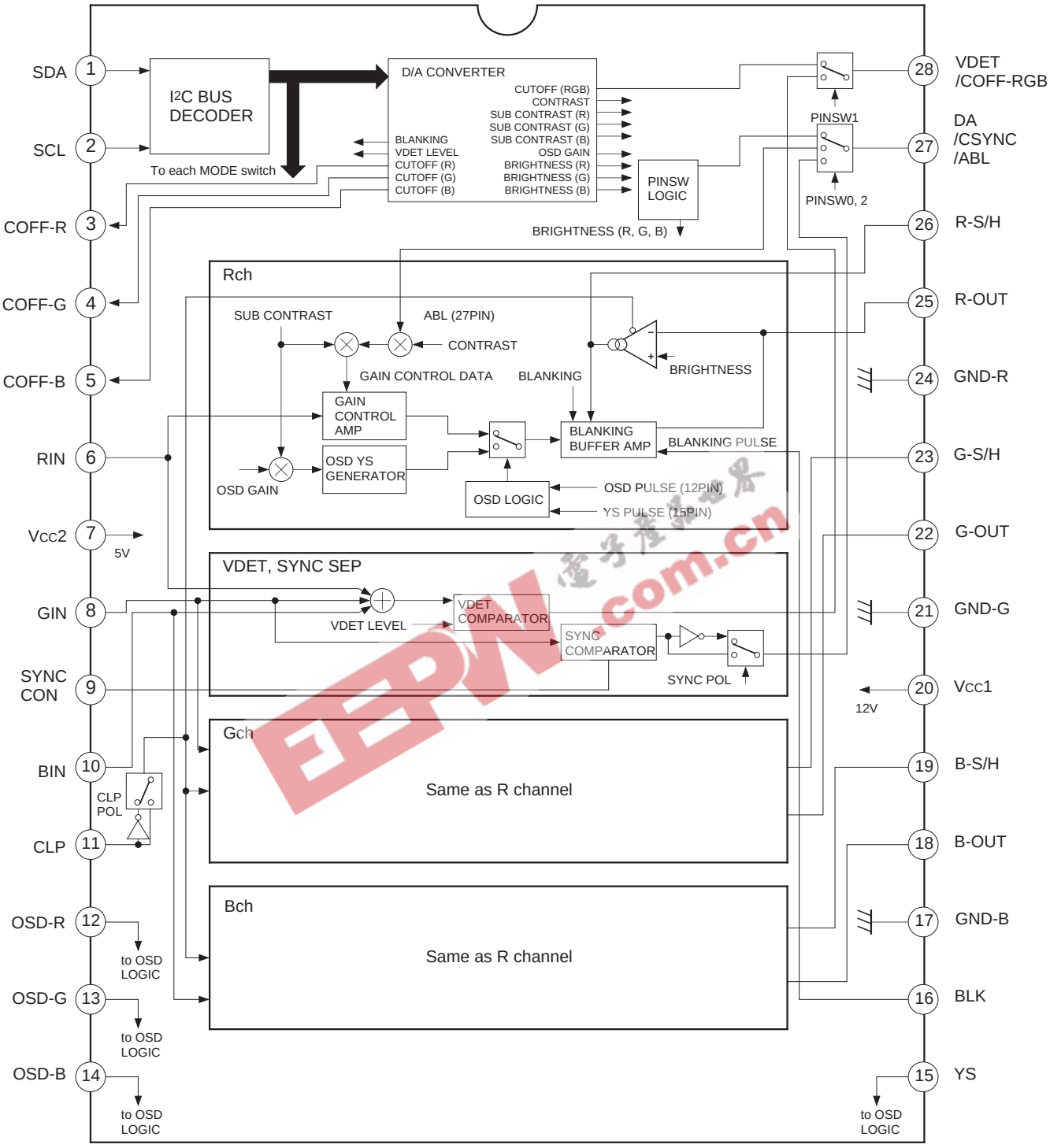
Operating Conditions

Recommended supply voltage

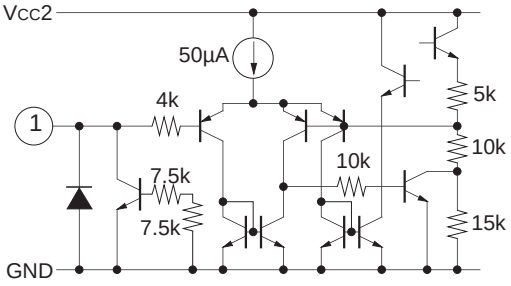
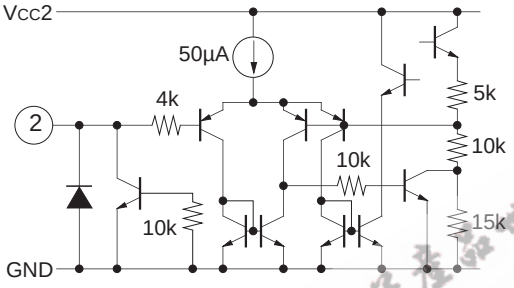
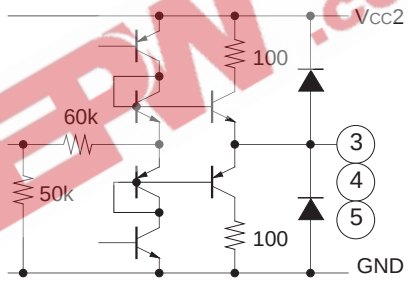
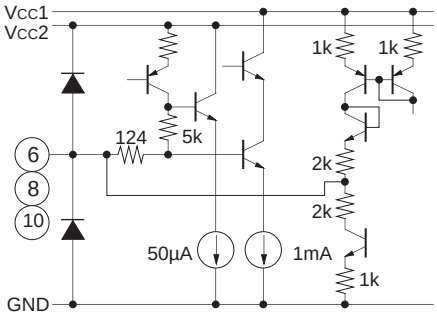
$V_{CC}1$	12±0.5	V
$V_{CC}2$	5±0.25	V

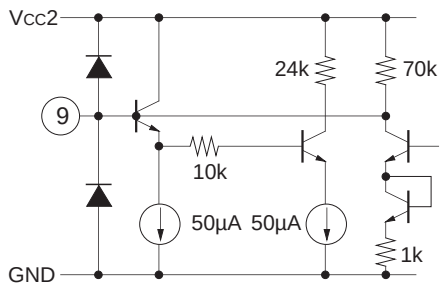
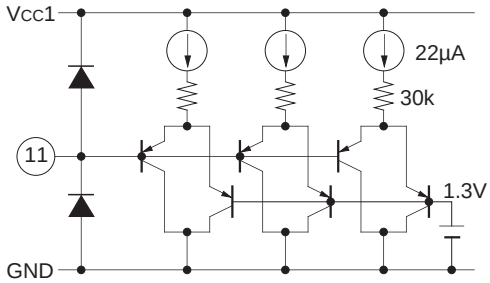
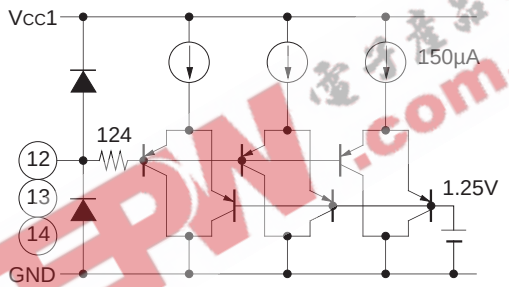
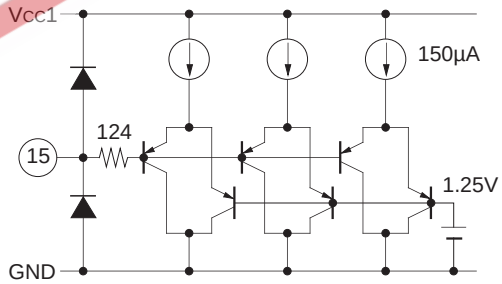
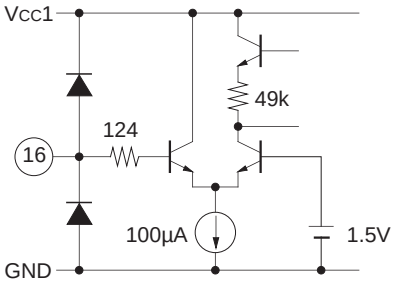


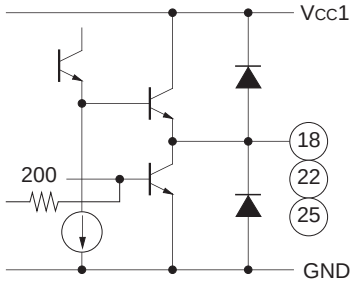
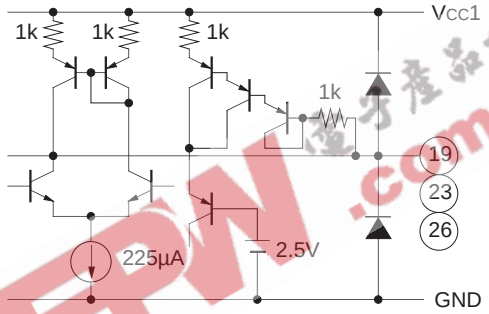
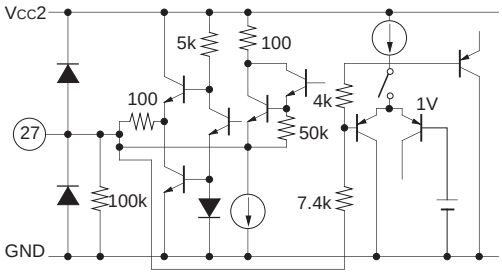
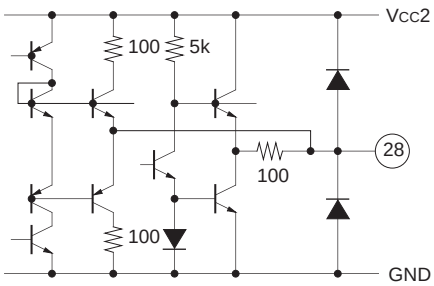
E96Z18-TE


SDA 1
SCL 2
COFF-R 3
COFF-G 4
COFF-B 5
RIN 6
Vcc2 7
5V
GIN 8
SYNC CON 9
BIN 10
CLP 11
OSD-R 12
OSD-G 13
OSD-B 14
to OSD LOGIC
I2C BUS DECODER
To each MODE switch
D/A CONVERTER
CUTOFF (RGB)
CONTRAST
SUB CONTRAST (R)
SUB CONTRAST (G)
SUB CONTRAST (B)
OSD GAIN
BRIGHTNESS (R)
BRIGHTNESS (G)
BRIGHTNESS (B)
BLANKING
VDET LEVEL
CUTOFF (R)
CUTOFF (G)
CUTOFF (B)
PINSW LOGIC
BRIGHTNESS (R, G, B)
PINSW1
PINSW0, 2
28 VDET /COFF-RGB
27 DA /CSYNC /ABL
26 R-S/H
25 R-OUT
24 GND-R
23 G-S/H
22 G-OUT
21 GND-G
20 Vcc1
12V
19 B-S/H
18 B-OUT
17 GND-B
16 BLK
15 YS
Rch
SUB CONTRAST
ABL (27PIN)
CONTRAST
BRIGHTNESS
GAIN CONTROL DATA
BLANKING
GAIN CONTROL AMP
BLANKING BUFFER AMP
BLANKING PULSE
OSD YS GENERATOR
OSD GAIN
OSD LOGIC
OSD PULSE (12PIN)
YS PULSE (15PIN)
VDET, SYNC SEP
VDET COMPARATOR
VDET LEVEL
SYNC COMPARATOR
SYNC POL
Gch
Same as R channel
Bch
Same as R channel
CLP POL

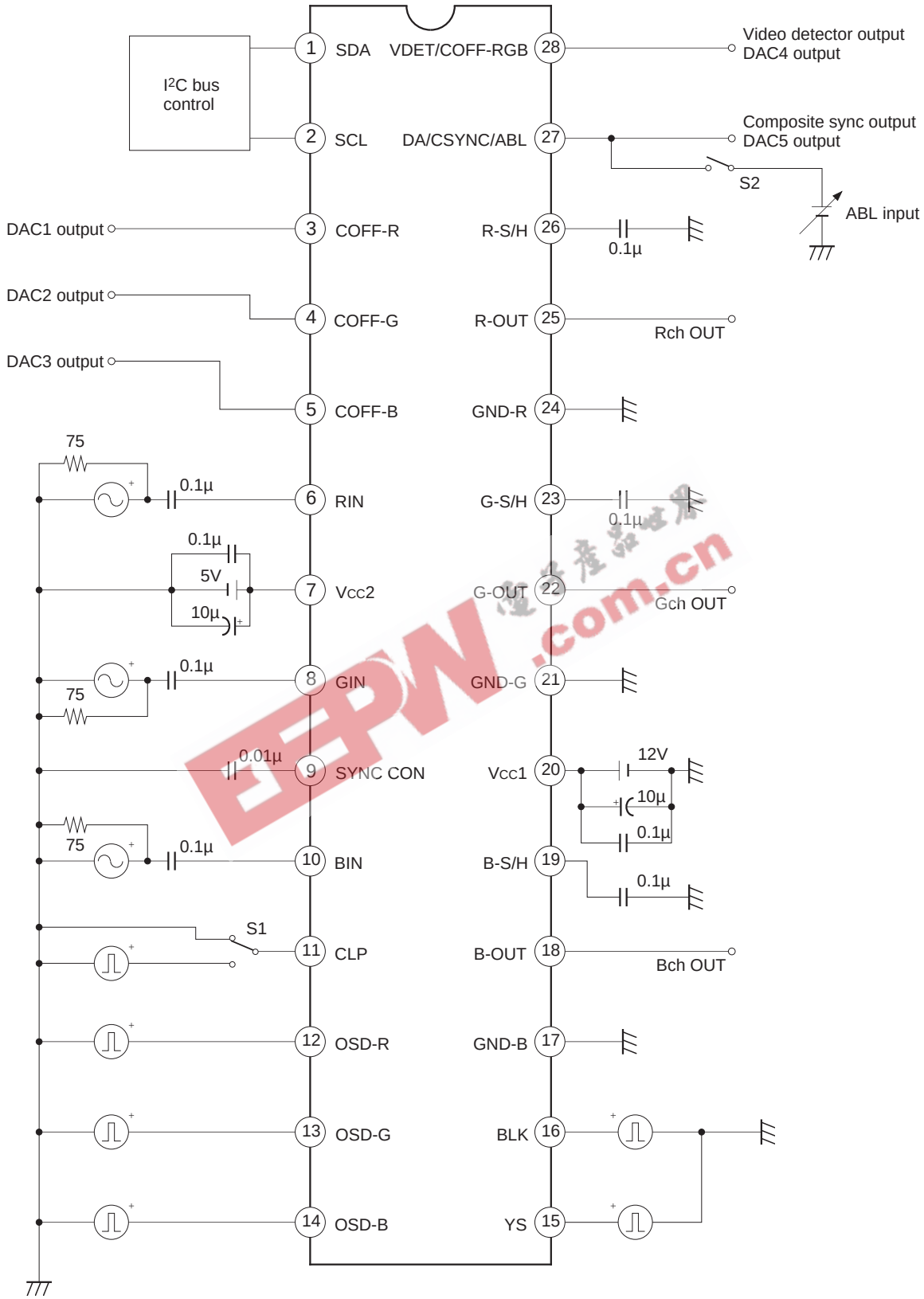
Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	SDA	—		I²C bus address and data input.
2	SCL	—		I²C bus clock signal input.
3 4 5	COFF-R COFF-G COFF-B	—		D/A converter outputs. The variable range is 1 to 4 V. Use as cut-off control voltages is recommended.
6 8 10	RIN GIN BIN	—		R, G and B inputs. When clamped, the input voltage black level is approximately 3.2 V. Connect 0.1 µF or more in series as a clamp capacitor.
7	Vcc2	5 V		5 V power supply.

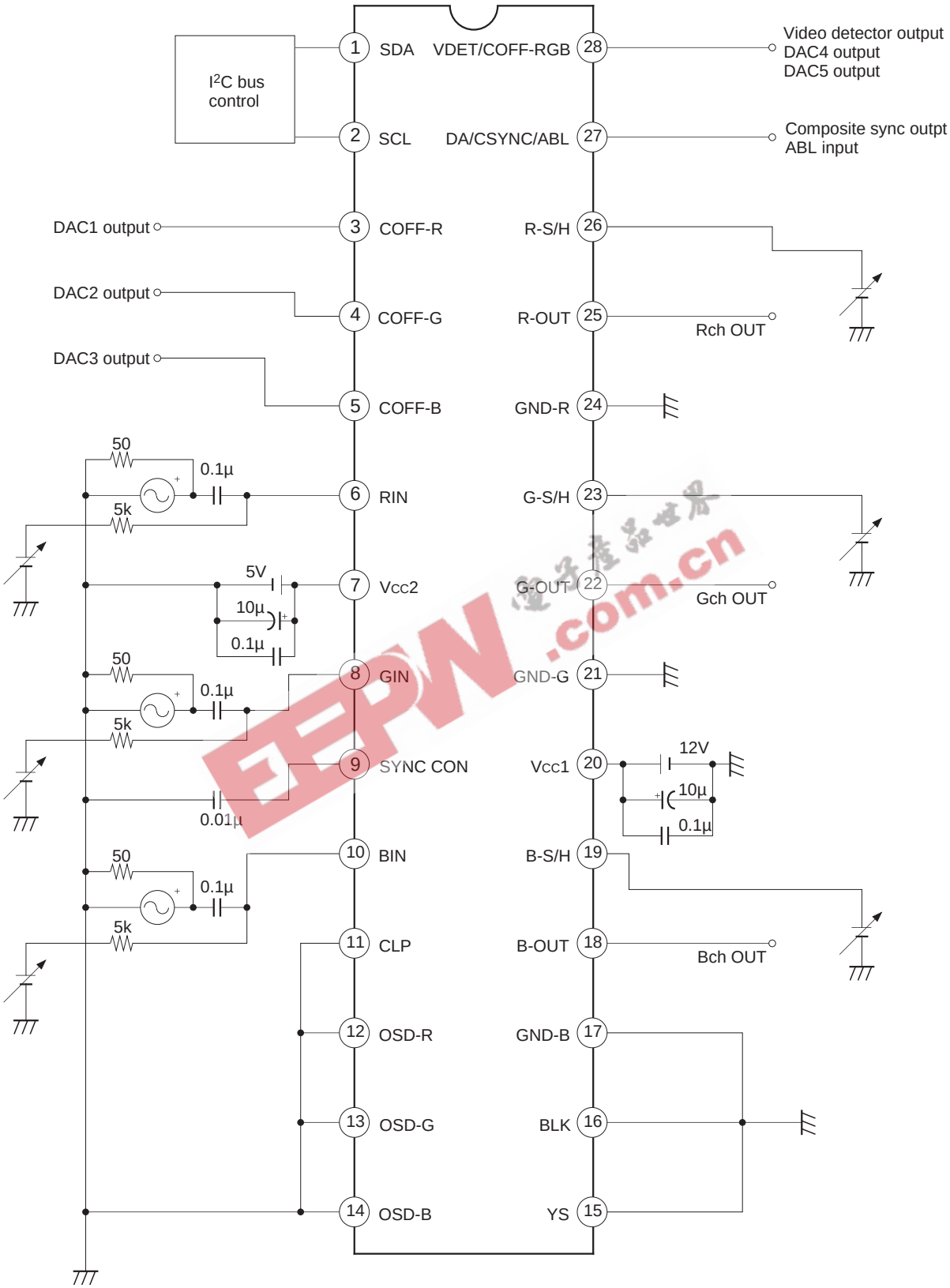
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	SYNC CON			Sync signal separation circuit block during sync-on-video signal input. Connect a sample-and-hold capacitor.
11	CLP	—		Clamp pulse input. The polarity can be switched via the I²C bus. The threshold level is approximately 1.3 V.
12	OSDR	—		R, G and B OSD pulse inputs. The threshold level is approximately 1 V.
13	OSDG			
14	OSDB			
15	YS	—		OSD-BLK pulse input. The threshold level is approximately 1.7 V.
16	BLK	—		BLK pulse input. The threshold level is approximately 1.5 V.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
17	GND-B	0 V		R, G and B independent GND.
21	GND-G			
24	GND-R			
18	B-OUT	—		R, G and B outputs.
22	G-OUT			
25	R-OUT			
19	B-S/H	—		Connection for external sample-and-hold capacitor (0.1 µF).
23	G-S/H			
26	R-S/H			
21	Vcc1	12 V		12 V power supply.
27	DA /CSYNC /ABL			General-purpose D/A converter output. Composite sync output. TTL drive is possible. VL=0.5 V or less, VH=4.0 V or more RGB output amplitude gain compensation input. (common for all three channels) Function switching is performed via the I²C bus.
28	VDET /COF-RGB	—		Video signal detection output. VL=0.5 V or less, VH=4.0 V or more General-purpose D/A converter output. The variable range is 1 to 4 V. Function switching is performed via the I²C bus.

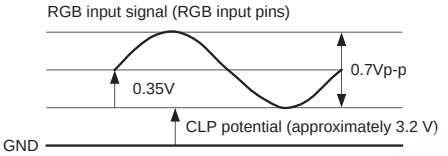
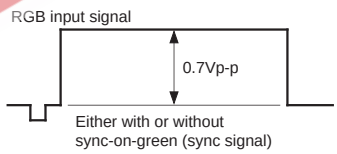
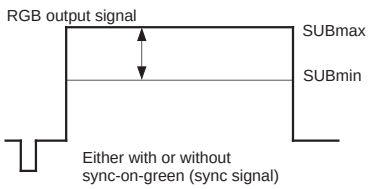
Electrical Characteristics Measurement Circuit

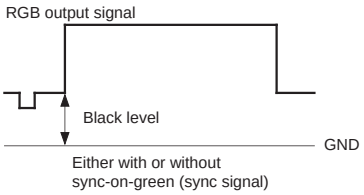
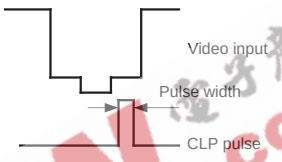
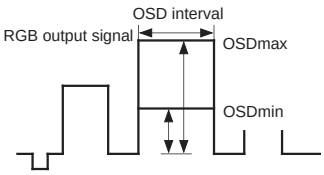
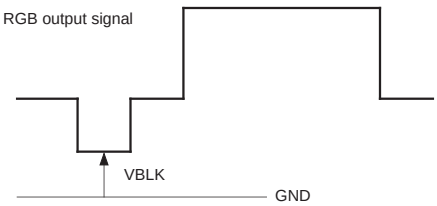


Electrical Characteristics Measurement Circuit (For AC Measurement)



Electrical Characteristics Ta=25 °C $V_{CC}1$=12 V $V_{CC}2$=5 V

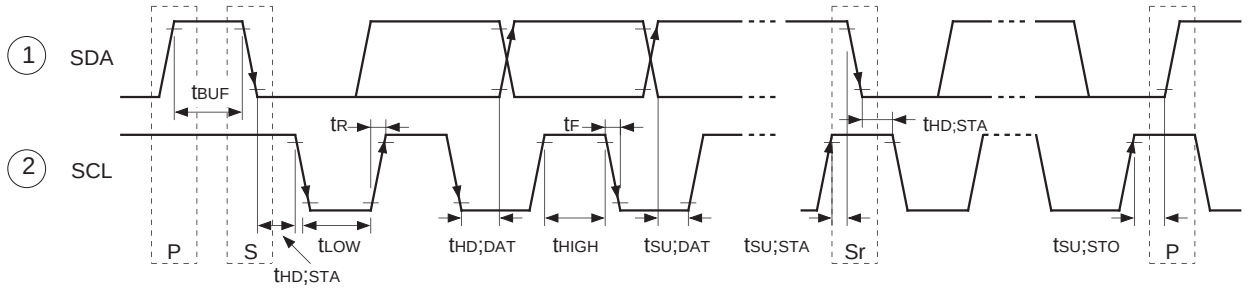
No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption	$I_{CC}1$ (12 V)	S1 : GND, S2 : OFF Input signal : none	—	82	115	mA
		$I_{CC}2$ (5 V)		—	40	55	mA
2	Frequency response	f 130 MHz	Input continuous 1 MHz and 130 MHz sine waves at 0.7 Vp-p. Measure the output amplitude gain difference at this time. Gain difference [dB] =20log $\left(\frac{V_{OUT}\ 130M}{V_{OUT}\ 1M}\right)$ 	—	–3.0	—	dB
3	Contrast control	CONTMAX	S1 : Pulse, S2 : OFF Measure the output signal amplitude V_{OUT} when a 0.7 Vp-p video signal is input. Calculate the contrast gain from this V_{OUT}. CONTMAX [dB] =20log $\left(\frac{V_{OUT}}{0.7}\right)$ 	16.0	16.5	—	dB
4	Subcontrast gain	SUBgain	S1 : Pulse, S2 : OFF Measure the variable width of the output signal amplitude V_{OUT} when a 0.7 Vp-p video signal is input. Gain difference [dB]= CONTMAX [dB] –20log $\left(\frac{V_{OUT}SUBmin}{0.7}\right)$ 	10.5	13.5	—	dB

No.	Measurement item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
5	Brightness control	BRTmax	S1 : Pulse, S2 : OFF CLP pulse width: 350 ns Measure the black level of the RGB output signal.  	3.4	3.7	—	V
		BRTmin		—	0.5	0.7	
6	Input dynamic range	Drang	S1 : Pulse, S2 : OFF Measure the level at which the output gain can be secured when the input video signal level is varied.	0.9	1	1.2	Vp-p
7	Minimum clamp pulse width	CLPmin	S1 : Pulse, S2 : OFF Measure the clamp pulse width over which the black level of the output signal VOUT does not change.  	200	—	—	nsec
8	OSD control range	OSDcont	S1 : Pulse, S2 : OFF Measure the variable width of the output signal VOUT when a 0.7 Vp-p video signal is input. Gain difference [dB] =20log $\left(\frac{\text{OSDmax}}{\text{OSDmin}}\right)$  	4.0	5.0	—	dB
9	BLK control	BLKmax	S1 : Pulse, S2 : OFF Measure the BLK level of the output signal when a 5.0 Vp-p BLK signal is input  	1.7	1.9	—	V
		BLKmin		—	0.1	0.4	

(I²C BUS Logic System)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	V
3	Low level output voltage SDA, during current inflow of 3 mA	V_{OL}	0	—	0.4	V
4	Maximum clock frequency	f_{SCL}	0	—	100	kHz
5	Minimum waiting time for data change	t_{BUF}	4.7	—	—	µs
6	Minimum waiting time for data transfer start	$t_{HD;STA}$	4.0	—	—	µs
7	Low level clock pulse width	t_{LOW}	4.7	—	—	µs
8	High level clock pulse width	t_{HIGH}	4.0	—	—	µs
9	Minimum waiting time for start preparation	$t_{SU;STA}$	4.7	—	—	µs
10	Minimum data hold time	$t_{HD;DAT}$	5	—	—	µs
11	Minimum data preparation time	$t_{SU;DAT}$	250	—	—	ns
12	Rise time	t_R	—	—	1000	ns
13	Fall time	t_F	—	—	300	ns
14	Minimum waiting time for stop preparation	$t_{SU;STO}$	4.0	—	—	µs

I²C BUS Control Signal

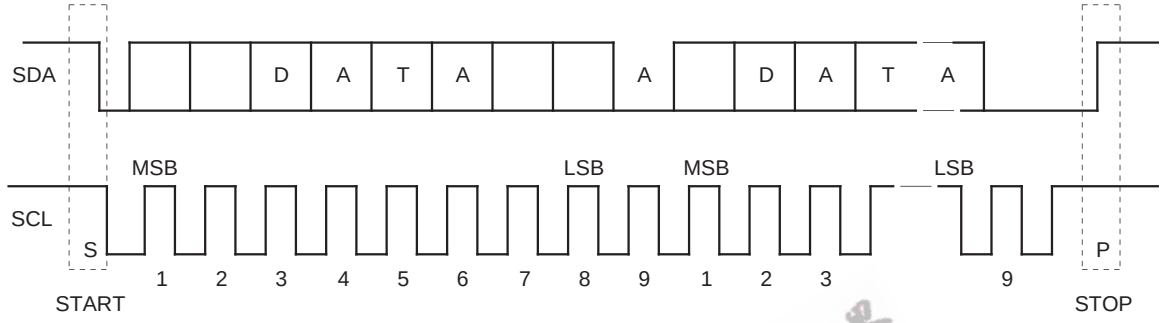


1. Application

The CXA2055P is a preamplifier for computer displays, and combines three R, G and B channels into a single package. All controls such as the contrast and black level for each channel are performed via I²C bus control.

1) I²C bus

Two wires (SDA, SCL) provide control over start, stop, data transfer, synchronization and collision avoidance. The IC outputs are either open collector or open drain, forming a bus line in the wired OR format. The bus signal configuration is as follows.



S : Start condition; SDA is set at "low" when SCL is "high".
P : Stop condition; SDA is set at "high" when SCL is "high".
A : Acknowledge; Signal sent from the slave.

Data is transmitted by MSB-first. One data unit consists of 8 bits, to which the acknowledge signal, which indicates that the data has been accepted by the slave, is attached at the end. Normally, the slave *1 IC receives data at the rising edge of SCL and the master *2 IC changes data at the falling edge of SCL. The actual data format is as follows.

S	Slave address 40H	A	Subaddress **H	A	DATA0	A	DATA1	A	DATA2	A	P

Slave address configuration

BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1
Slave address							R/W

The slave address is an address unique to each IC, and is assigned according to the IC functions. The upper 7 of the 8 bits are the unique address and the final bit is the R/W bit. The R/W bit indicates read *3 when 1 and write *4 when 0. 40H is allotted as the slave address for the CXA2055P. (This is write only and there is no read mode.)

The subaddress is the assigned address within the IC, and is used for the various IC adjustments. The subaddress is sent just once following the slave address, and is automatically incremented thereafter until a stop condition is sent.

*1 Slave : An IC that is placed under the control of the master.
In a normal system, all devices excluding the central microcomputer are slaves.
*2 Master : A central microcomputer or other controlling IC.
*3 Read : Mode where data is read from master to slave.
*4 Write : Mode where data is written from master to slave.

2) Register map
- Slave address : 40H
- "*" indicates undefined.
- Values inside parentheses ( ) are the initial setting values (during power-on reset) (undetermined when not indicated)

Slave address configuration

BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1
0	1	0	0	0	0	0	R/W

SUB ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	CONTRAST							
01H	SUB CONTRAST R							
02H	SUB CONTRAST G							
03H	SUB CONTRAST B							
04H	*	*	OSD GAIN				BRT MODE (2)	
05H	BRIGHTNESS R (DA)							
06H	BRIGHTNESS G							
07H	BRIGHTNESS B							
08H	CUT OFF RGB							
09H	CUT OFF R							
0AH	CUT OFF G							
0BH	CUT OFF B							
0CH	BLK (0) MODE	*	BLANKING LEVEL (0)					
0DH	BRT SW (0)	SYNC POL (0)	VDET MODE (0)	POWER SAVE (0)	*	CLP (0)	VDET LEVEL	
0EH	*	*	*	*	D/A TEST (0)	PINSW2 (0)	PINSW1 (0)	PINSW0 (0)

3) Description of registers (Numbers inside parentheses ( ) indicate the number of bits.)

CONTRAST (8) : Adjusts the R, G and B-OUT (Pins 25, 22 and 18) output amplitude gain commonly for all three channels.

SUB CONTRAST (8) : Adjusts the R, G and B-OUT (Pins 25, 22 and 18) output amplitude gain independently for each channel.

OSD GAIN (4) : Adjusts the OSD R, G and B (Pins 12, 13 and 14) OSD interval output signal gain commonly for all three channels.

BRTMODE (2) : This register changes the output dynamic range.
The 2H setting is recommended.
0H : Output dynamic range 0.5 V to 4.5 V
1H : Output dynamic range 0.5 V to 5.5 V
2H : Output dynamic range 1.0 V to 6.5 V (recommended)
3H : Output dynamic range 2.0 V to 7.5 V

BRIGHTNESS (8) : Controls the output black level potential.
(Three-channel independent and common control can be selected by BRTSW.
During three-channel common mode, control is performed by the G channel.)

CUT OFF (8) : This is a general-purpose DAC. Use as a cut-off control is recommended.

BLK MODE (1) : Switches the blanking level mode
0H : BLK LEVEL=fixed
1H : BLK LEVEL=variable

BLANKING LEVEL (6) : Sets the blanking level when BLK MODE is set to 1H.

BRTSW (1) : Switches the brightness control between three-channel independent and three-channel common control. When using three-channel common mode, the BRIGHTNESS G channel is valid.
0H : Three-channel independent mode
1H : Three-channel common mode

SYNC POL (1) : Switches the sync separator output polarity during sync-on-green input.
0H : Positive polarity
1H : Negative polarity

VDET MODE (1) : Switches the video signal detection mode.
0H : B channel only is detected
1H : Signal obtained by adding R, G and B signals is detected

POWER SAVE (1) : Power save mode selector switch.
0H : Power save not performed
1H : Power save performed

CLP (1) : Selects the input clamp pulse polarity.
0H : Positive polarity input
1H : Negative polarity input

VDET LEVEL (2) : Threshold level selector switch for video interval detection. The threshold level changes as follows.
(An input pulse width of as narrow as 10 ns can be detected.)

When VDET MOD=0H	When VDET MOD=1H
0H : 300 mV or more	0H : Undetectable
1H : Undetectable	1H : Undetectable
2H : Undetectable	2H : 300 mV or more
3H : Undetectable	3H : 600 mV or more

Note) The threshold level when VDET MOD=1H is the total of the three channel inputs.

D/A TEST (1) : DA TEST switch for IC measurement. Set to 0H.

PINSW : Switches the Pins 27 and 28 functions. ("∗" indicates don't care.)

PINSW			Pin 28 output	Pin 27 output
2	1	0		
0	0	0	DA (COFF_RGB)	C-SYNC
1	0	0	DA (COFF_RGB)	ABL (CONTRAST)
0	1	0	VDET	C-SYNC
1	1	0	VDET	ABL (CONTRAST)
∗	0	1	DA (COFF_RGB)	DA (BRIGHTNESS)
∗	1	1	VDET	DA (BRIGHTNESS)

Note) When the Pin 27 output is set to DA (BRIGHTNESS), BRIGHTNESS is forcibly set to the three-channel common mode.

2. Blanking addition function

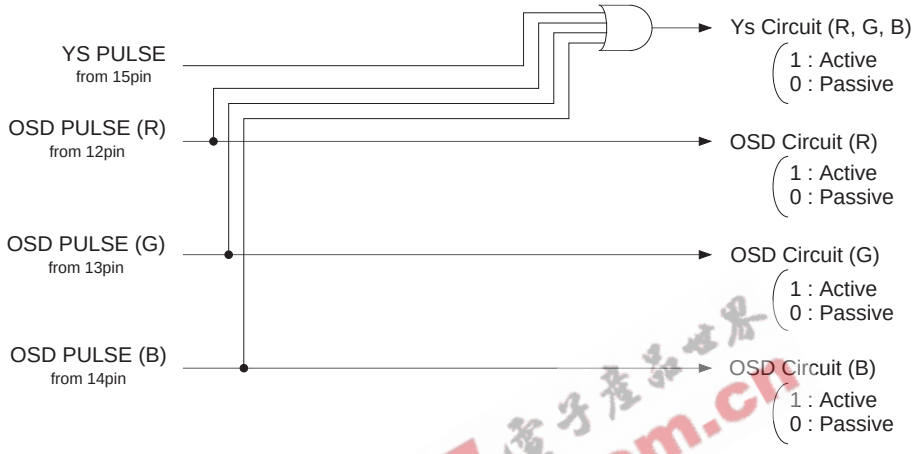
The output is blanked while the BLK pin (Pin 16) is high level.

The BLK pin threshold level is approximately 1.5 V.

3. OSD addition function and OSD contrast control

OSD can be added to the video signal while the OSD-R, G and B pins (Pins 12, 13 and 14) are high level. OSD blanking is added when any of these three channels is high level.

OSD blanking is also added to all three channels while the YS pin (Pin 15) is high level. See the following logic.



4. CONTRAST function

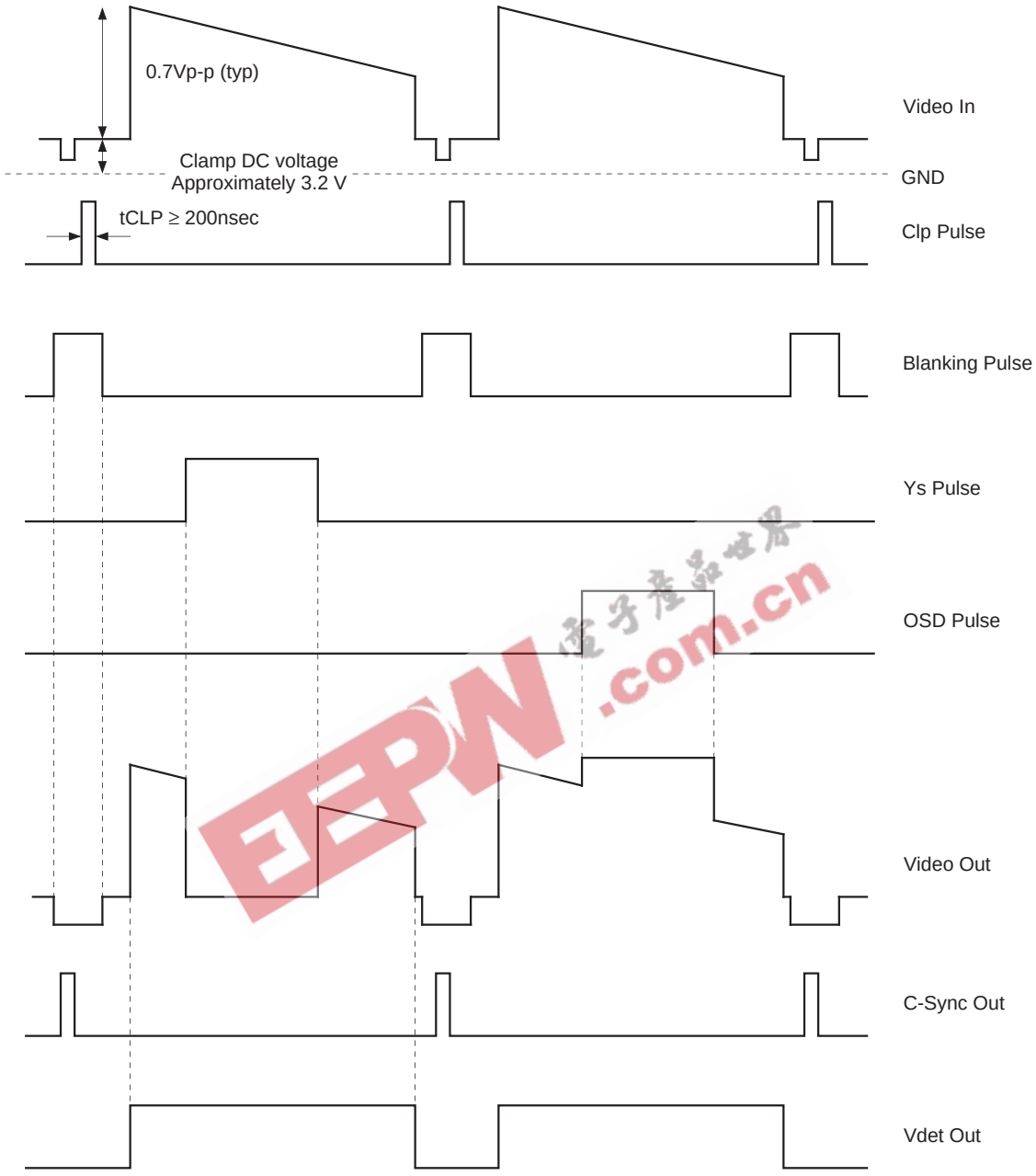
The CONTRAST function performs gain control for the R, G and B-OUT output amplitudes.

5. ABL function

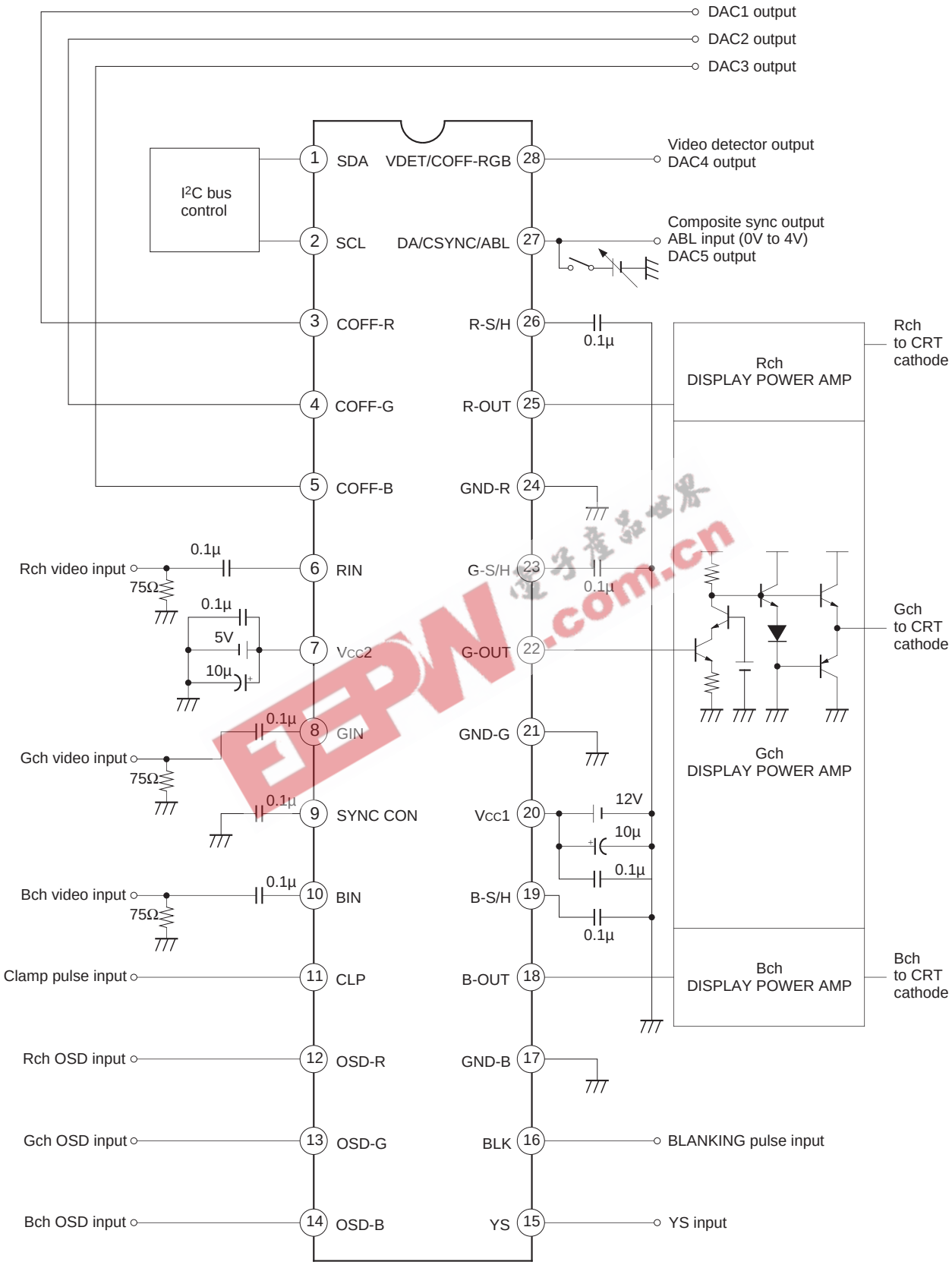
ABL control can be performed by Pin 27 by setting PINSW. The variable range is approximately 13.7 dB.

See the characteristics diagrams hereafter for the control characteristics.

I/O Signal Example



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Board Pattern and Layout

1. When not using the OSD, YS or BLK pins, connect these pins to GND.

2. Care should be taken for the following items regarding the output signals from R, G and BOUT.
   1) Connect these signal lines so that they are high impedance to external circuits.
   2) Do not allow current to flow into the IC side.
   3) Arrange the signal lines so that the distance to the power amplifier is as short as possible.

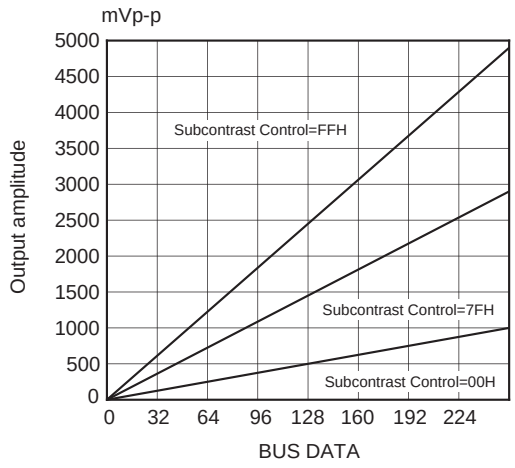
3. The $V_{CC}1$ and $V_{CC}2$ decoupling capacitors should consist of ceramic capacitors and electrolytic capacitors connected in parallel, and should be connected as close to the IC as possible.

4. The R, G and BIN clamp capacitors should be located as close to the IC as possible.

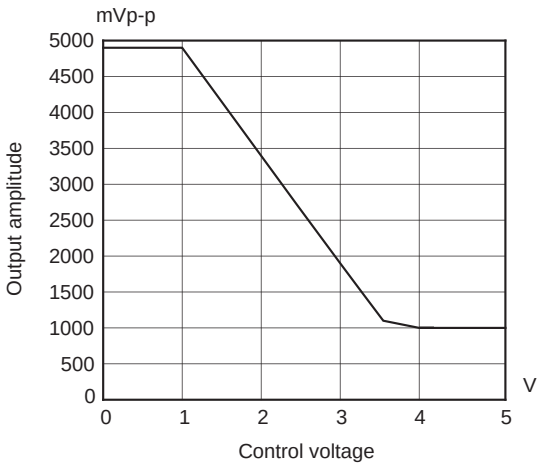
5. The sample-and-hold capacitors connected to the R, G and B-S/H pins should be connected as close to the IC as possible.

6. The output signals from COFF-R, G and B should be arranged so that capacitance of 20 pF or more is not applied to the pins or the pattern.

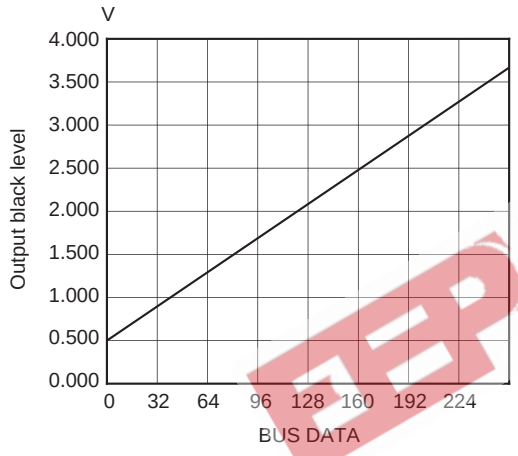
Contrast control characteristics, subcontrast control characteristics
Input amplitude 700mVp-p



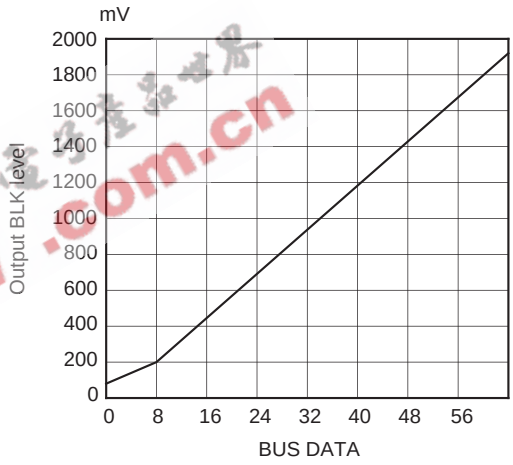
ABL characteristics



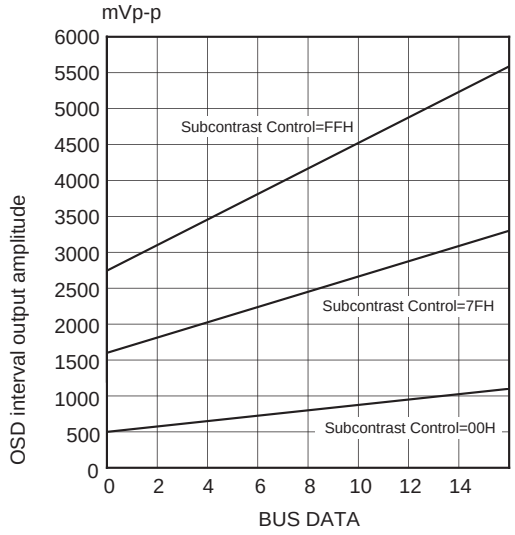
Brightness control characteristics



BLK control characteristics

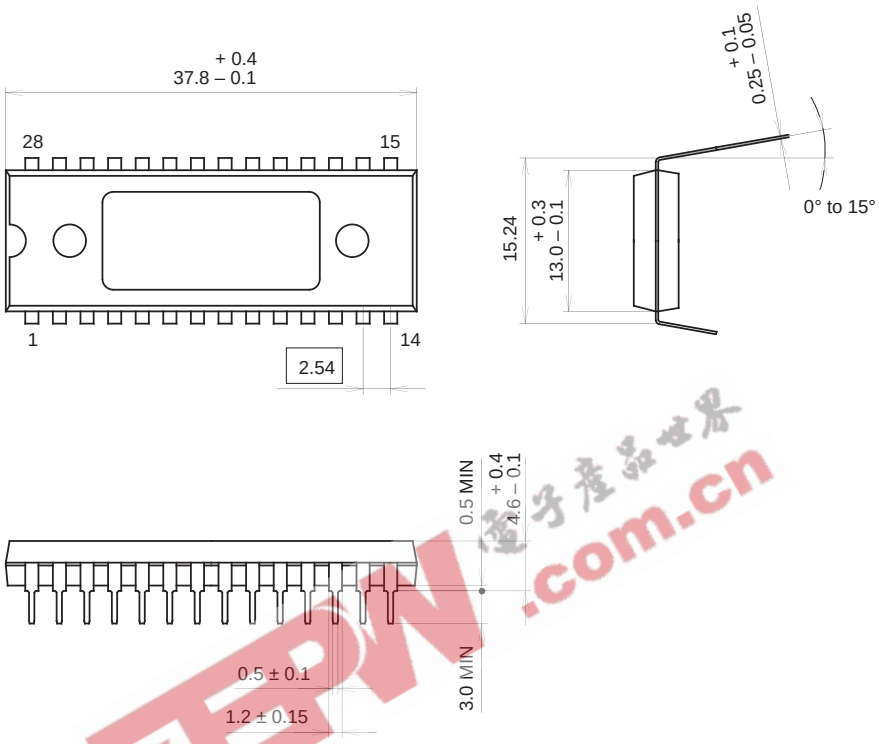


OSD control characteristics



Package Outline Unit : mm

28PIN DIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.Center part is mirror surface.

SONY CODE	DIP-28P-03
EIAJ CODE	DIP028-P-0600
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	4.2g