

## RF Signal Processing Servo Amplifier for CD Player

**Description**

The CXA2542Q is a bipolar IC developed for CD player RF signal processing and servo control.

**Features**

- Automatic focus bias adjustment circuit
- Automatic tracking balance and gain adjustment circuits
- RF level control circuit
- Interruption countermeasure circuit
- Anti-shock circuit
- Defect detection and prevention circuits
- RF 1-V amplifier, RF amplifier
- APC circuit
- Focus and tracking error amplifier
- Focus, tracking and sled servo control circuits
- Focus OK circuit
- Mirror detection circuit
- Single power supply and dual power supplies

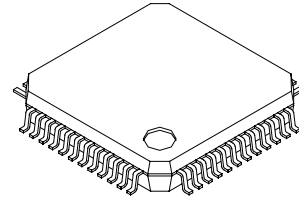
**Applications**

CD players

**Structure**

Bipolar silicon monolithic IC

48 pin QFP (Plastic)

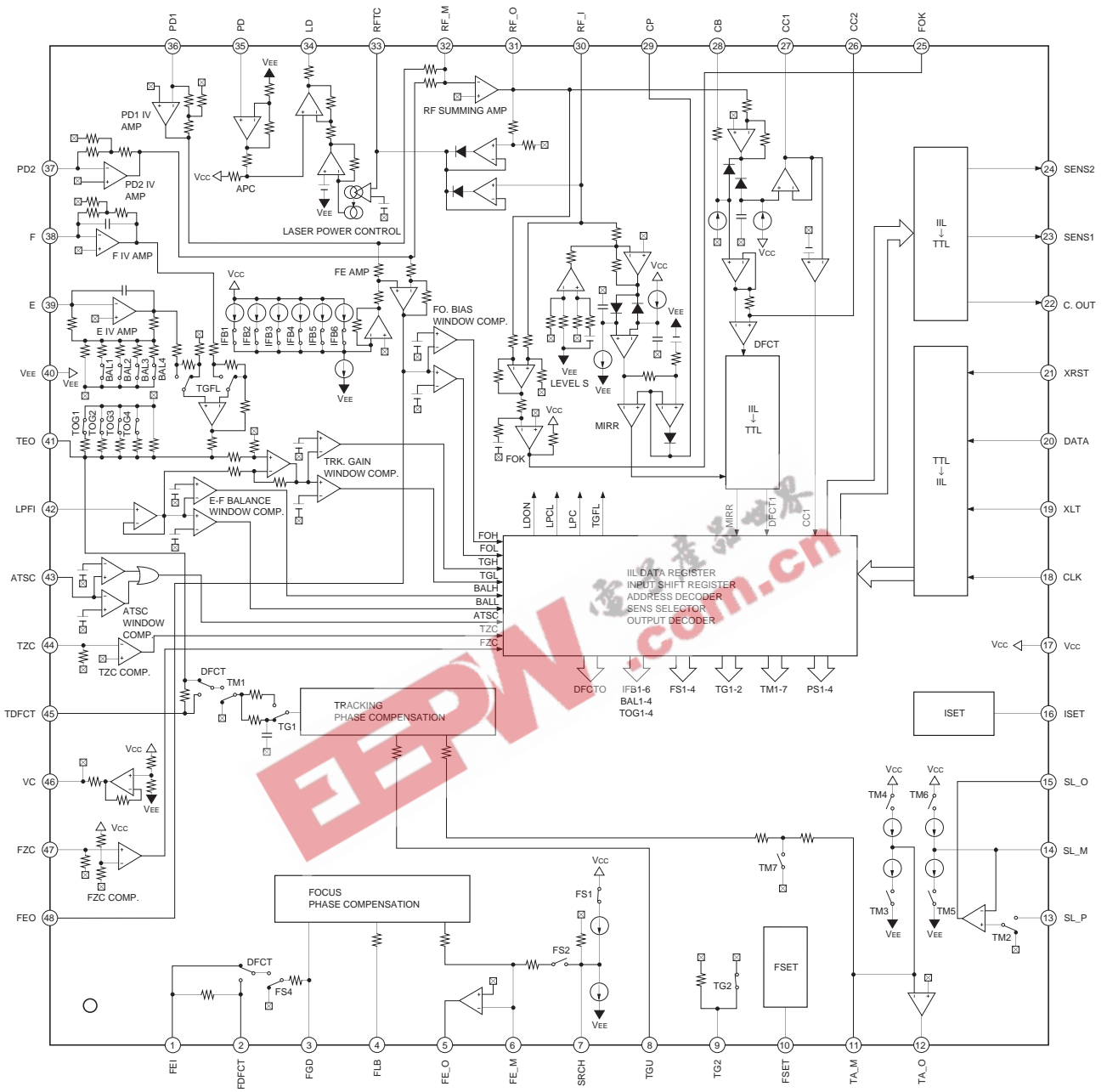
**Absolute Maximum Ratings** (Ta = 25°C)

- |                               |                  |             |    |
|-------------------------------|------------------|-------------|----|
| • Supply voltage              | V <sub>CC</sub>  | 12          | V  |
| • Operating temperature       | T <sub>opr</sub> | -20 to +75  | °C |
| • Storage temperature         | T <sub>stg</sub> | -65 to +150 | °C |
| • Allowable power dissipation | P <sub>D</sub>   | 1400        | mW |

**Recommended Operating Conditions**

Operating supply voltage V<sub>CC</sub> – V<sub>EE</sub> 3.0 to 5.5 V


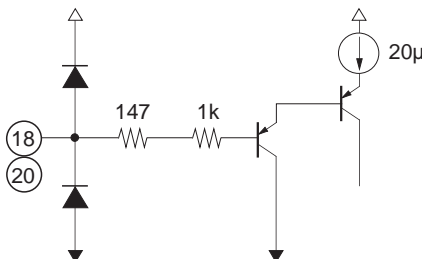
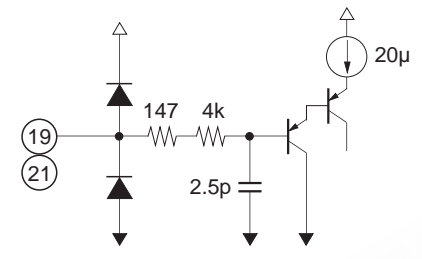
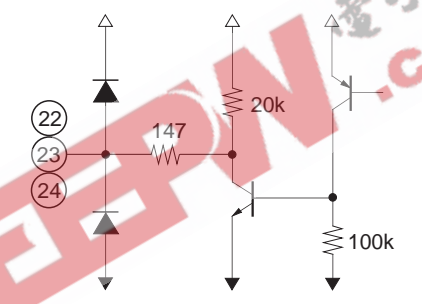
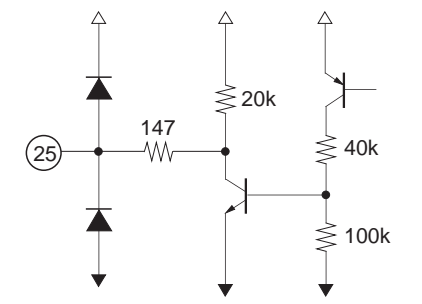
Block Diagram



Pin Description

| Pin No. | Symbol | I/O | Equivalent circuit | Description  |
|---------|--------|-----|--------------------|--|
| 1       | FEI    | I   |                    | Focus error input.   |
| 2       | FDFCT  | I   |                    | Connects the capacitor for defect time constant.                                     |
| 3       | FGD    | I   |                    | Ground this pin through a capacitor for cutting the focus servo high-frequency gain. |
| 4       | FLB    | I   |                    | External time constant setting pin for boosting the focus servo low-frequency.       |
| 5       | FE_O   | O   |                    | Focus drive output.  |
| 12      | TA_O   | O   |                    | Tracking drive output.   |
| 15      | SL_O   | O   |                    | Sled drive output.   |
| 6       | FE_M   | I   |                    | Focus amplifier inverted input.  |
| 7       | SRCH   | I   |                    | External time constant setting pin for generating focus search waveform.             |

| Pin No. | Symbol | I/O | Equivalent circuit | Description   |
|---------|--------|-----|--------------------|---|
| 8       | TGU    | I   |                    | External time constant setting pin for switching tracking high-frequency gain.  |
| 9       | TG2    | I   |                    | External time constant setting pin for switching tracking high-frequency gain.  |
| 10      | FSET   | I   |                    | Peak frequency setting pin for focus and tracking phase compensation amplifier.   |
| 11      | TA_M   | I   |                    | Tracking amplifier inverted input.  |
| 13      | SL_P   | I   |                    | Sled amplifier non-inverted input.  |
| 14      | SL_M   | I   |                    | Sled amplifier inverted input.  |
| 16      | ISET   | I   |                    | Connects the external capacitor to set the current which determines the Focus search, Track jump, and Sled kick levels. |

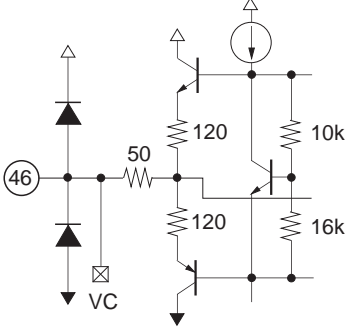
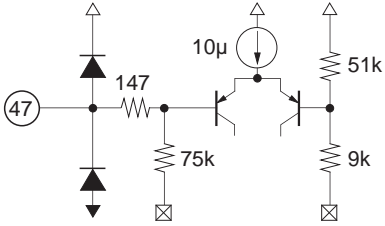
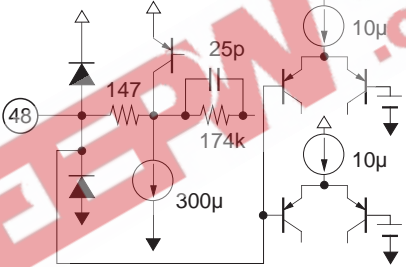
| Pin No. | Symbol | I/O | Equivalent circuit  | Description  |
|---------|--------|-----|---|--|
| 17      | Vcc    | I   |    | Positive power supply.   |
| 18      | CLK    | I   |    | Serial data transfer clock input from CPU. (no pull-up resistance)                           |
| 20      | DATA   | I   |   | Serial data input from CPU. (no pull-up resistance)  |
| 19      | XLT    | I   |    | Latch input from CPU. (no pull-up resistance)  |
| 21      | XRST   | I   |   | Reset input; resets at Low. (no pull-up resistance)  |
| 22      | C. OUT | O   |  | Track number count signal output.  |
| 23      | SENS1  | O   |   | Outputs FZC, DFCT1, TZC, BALH, TGH, FOH, ATSC, and others according to the command from CPU. |
| 24      | SENS2  | O   |   | Outputs DFCT2, MIRR, BALL, TGL, FOL, and others according to the command from the CPU.       |
| 25      | FOK    | O   |  | Focus OK comparator output.  |

| Pin No. | Symbol | I/O | Equivalent circuit | Description  |
|---------|--------|-----|--------------------|--|
| 26      | CC2    | I   |                    | Input for the defect bottom hold output with capacitance coupled.  |
| 27      | CC1    | O   |                    | Defect bottom hold output. Connected internally to the interruption comparator input.  |
| 28      | CB     | I   |                    | Connects the defect bottom hold capacitor.   |
| 29      | CP     | I   |                    | Connects the MIRR hold capacitor. MIRR comparator non-inverted input.  |
| 30      | RF_I   | I   |                    | Input for the RF summing amplifier output with capacitance coupled.  |
| 31      | RF_O   | O   |                    | RF summing amplifier output. Eye-pattern check point.  |
| 32      | RF_M   | I   |                    | RF summing amplifier inverted input. The RF amplifier gain is determined by the resistance connected between this pin and RFO pin. |
| 33      | RFTC   | I   |                    | External time constant setting pin during RF level control.  |

| Pin No.  | Symbol          | I/O    | Equivalent circuit | Description   |
|----------|-----------------|--------|--------------------|---|
| 34       | LD              | O      |                    | APC amplifier output.   |
| 35       | PD              | I      |                    | APC amplifier input.  |
| 36<br>37 | PD1<br>PD2      | I<br>I |                    | RF I-V amplifier inverted input.<br>Connect these pins to the photo diode A + C and B + D pins. |
| 38<br>39 | F<br>E          | I<br>I |                    | F I-V and E I-V amplifier inverted input.<br>Connects these pins to photo diodes F and E.       |
| 40       | V <sub>EE</sub> | —      |                    | Negative power supply.  |

| Pin No. | Symbol | I/O | Equivalent circuit | Description   |
|---------|--------|-----|--------------------|---|
| 41      | TEO    | O   |                    | Tracking error amplifier output. E-F signal is output.                |
| 45      | TDFCT  | I   |                    | Connects the capacitor for defect time constant.                      |
| 42      | LPFI   | I   |                    | Comparator input for balance adjustment. (Input from TEO through LPF) |
| 43      | ATSC   | I   |                    | Window comparator input for ATSC detection.                           |
| 44      | TZC    | I   |                    | Tracking zero-cross comparator input.                                 |



| Pin No. | Symbol | I/O | Equivalent circuit  | Description   |
|---------|--------|-----|---|---|
| 46      | VC     | O   |    | <p><math>(V_{CC} + V_{EE})/2</math> direct voltage output.</p>  |
| 47      | FZC    | I   |    | <p>Focus zero-cross comparator input.</p>   |
| 48      | FEO    | O   |  | <p>Focus error amplifier output.<br/>Connected internally to the window comparator input for bias adjustment.</p> |

Electrical Characteristics

(V<sub>CC</sub> = 1.5V, V<sub>EE</sub> = 1.5V, T<sub>opr</sub> = 25°C)

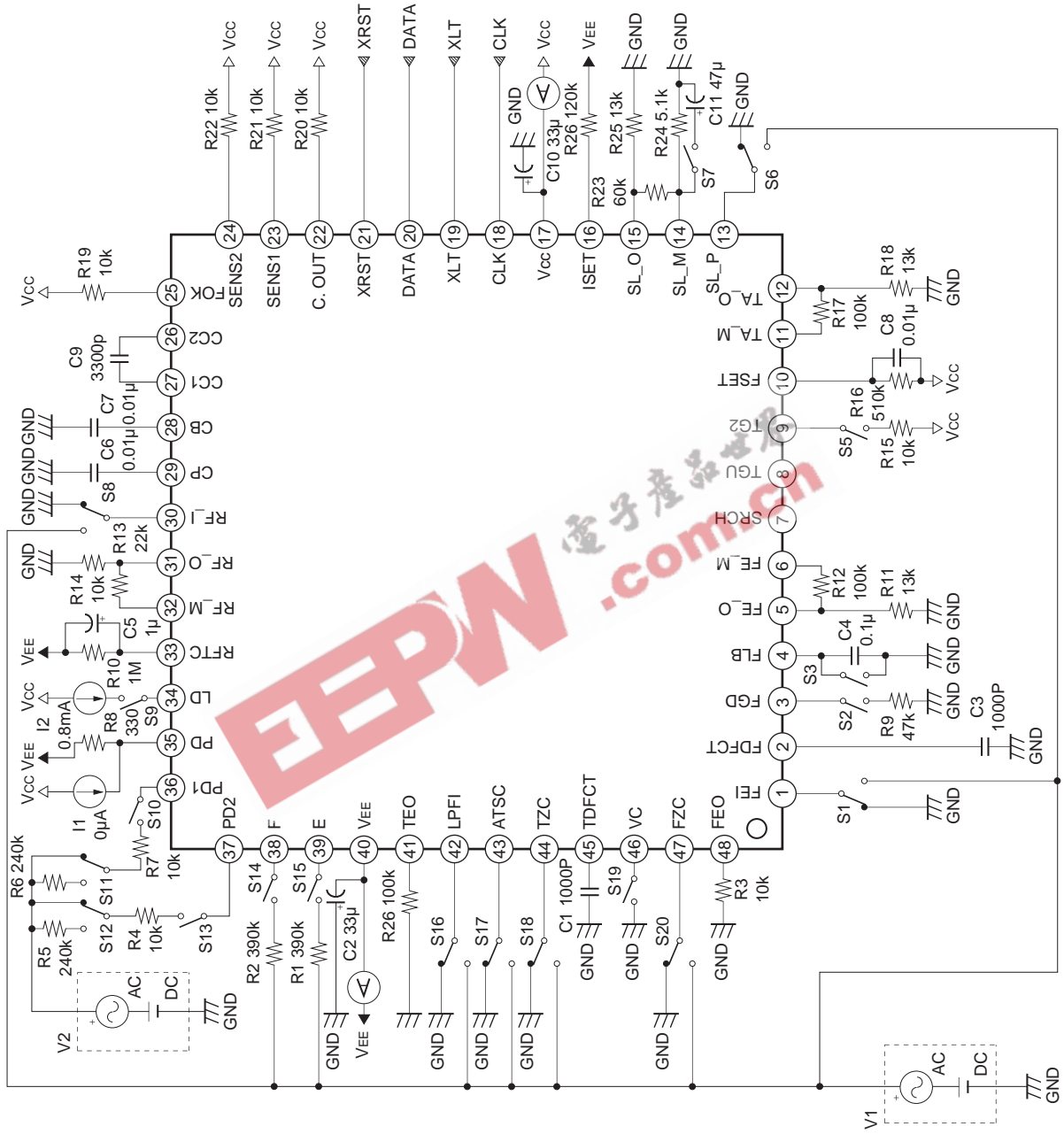
| TEST | Item                                       | SW conditions<br>(ON switches) | SD  | Input<br>pin | Measure-<br>ment pin | Measurement<br>conditions                                     | Min.  | Typ.  | Max.  | Unit |
|------|--|--------------------------------|-----|--------------|----------------------|---|-------|-------|-------|------|
| T1   | Current consumption 1                      | 19 (OFF)                       | RST | 17           | 17                   |   | 12.2  | 18.8  | 25.4  | mA   |
| T2   | Current consumption 2                      | 19 (OFF)                       | RST | 40           | 40                   |   | -25.4 | -18.8 | -12.2 | mA   |
| T3   | Center amplifier output offset             | 19 (OFF)                       | RST | —            | 46                   |   | -100  | 0     | 100   | mV   |
| T4   | Offset                                     |                                | RST |              | 31                   |   | -50   | 0     | 50    | mV   |
| T5   | RF amplifier<br>Voltage gain               | 10, 13                         | RST | 36<br>37     | 31                   | 1kHz I/O ratio  | 24.5  | 27.5  | 30.5  | dB   |
| T6   |  | 10, 13                         | RST | 36<br>37     | 31                   | V <sub>2</sub> = 0.2VDC                                       | 1.2   | 1.3   | —     | V    |
| T7   |  | 10, 13                         | RST | 36<br>37     | 31                   | V <sub>2</sub> = 0.2VDC                                       | —     | -0.6  | -0.3  | V    |
| T8   | Offset                                     |                                | 39F |              | 48                   | 1FB6: ON  | -120  | 0     | 120   | mV   |
| T9   | Voltage gain 1                             | 10                             | 39F | 36           | 48                   | 1kHz I/O ratio  | 26    | 29    | 32    | dB   |
| T10  | Voltage gain 2                             | 13                             | 39F | 37           | 48                   | 1kHz I/O ratio  | 26    | 29    | 32    | dB   |
| T11  | Voltage gain difference                    |                                | 39F |              |                      |   | -3    | 0     | 3     | dB   |
| T12  | FE amplifier<br>Max. output voltage – High | 13                             | 39F | 37           | 48                   | V <sub>2</sub> = 100mVDC                                      | 1     | 1.3   | —     | V    |
| T13  |  | 10                             | 39F | 36           | 48                   | V <sub>2</sub> = 100mVDC                                      | —     | -1.3  | -1    | V    |
| T14  | BIAS0                                      |                                | 3BF |              | 48                   | IFB1, 2, 3, 4, 5, 6: OFF                                      | 560   | 718   | 1042  | mV   |
| T15  | BIAS1                                      |                                | 3BE |              | 48                   | IFB1: ON, BIAS0: reference                                    | -29.0 | -22.7 | -16.5 | mV   |
| T16  | BIAS2                                      |                                | 3BD |              | 48                   | IFB2: ON, BIAS0: reference<br>Output gain difference with T15 | 5     | 6     | 7     | dB   |
| T17  | BIAS3                                      |                                | 3BB |              | 48                   | IFB3: ON, BIAS0: reference<br>Output gain difference with V17 | 5     | 6     | 7     | dB   |
| T18  | BIAS4                                      |                                | 3B7 |              | 48                   | IFB4: ON, BIAS0: reference<br>Output gain difference with V18 | 5     | 6     | 7     | dB   |
| T19  | BIAS5                                      |                                | 3AF |              | 48                   | IFB5: ON, BIAS0: reference<br>Output gain difference with V19 | 5     | 6     | 7     | dB   |
| T20  | BIAS6                                      |                                | 39F |              | 48                   | IFB6: ON, BIAS0: reference<br>Output gain difference with V20 | 5     | 6     | 7     | dB   |

| TEST | Item                          | SW conditions<br>(ON switches) | SD               | Input<br>pin | Measure-<br>ment pin | Measurement<br>conditions  | Min.  | Typ.  | Max.  | Unit |
|------|-------------------------------|--------------------------------|------------------|--------------|----------------------|--|-------|-------|-------|------|
| T21  | FE amplifier<br>FOH threshold |                                | 39F              |              | 48                   | IFB6: ON<br>Pin 1 voltage when SENS1<br>(Pin 23) goes from High to Low | 5     | 20    | 35    | mV   |
| T22  |                               | FOL threshold                  | 39F              |              | 48                   | IFB6: ON<br>Pin 1 voltage when SENS2<br>(Pin 24) goes from High to Low | -35   | -20   | -5    | mV   |
| T23  | Offset                        |                                | 34F<br>308       | 38<br>39     | 41                   | TOG: OFF,<br>BAL1, 2, 3: ON  | -25   | 0     | 25    | mV   |
| T24  | GAIN UP (F)                   | 14                             | 36F<br>308       | 38           | 41                   | V1 = 2 kHz, I/O ratio<br>TOG: OFF, BAL1, 2, 3: ON                      | 7.2   | 10.2  | 13.2  | dB   |
| T25  | GAIN UP (E)                   | 15                             | 36F<br>308       | 39           | 41                   | V1 = 2 kHz, I/O ratio<br>TOG: OFF, BAL1, 2, 3: ON                      | 7.2   | 10.2  | 13.2  | dB   |
| T26  | Voltage gain<br>F0            | 14                             | 34F              | 38           | 41                   | V1 = 2kHz, TOG: OFF<br>I/O ratio                                       | 1.2   | 4.2   | 7.2   | dB   |
| T27  | Voltage gain<br>F1            | 14                             | 34E<br>30F       | 38           | 41                   | V1 = 2kHz, TOG1: ON<br>Reference to F0                                 | -2.3  | -1.8  | -1.3  | dB   |
| T28  | Voltage gain<br>F2            | 14                             | 34D              | 38           | 41                   | V1 = 2kHz, TOG2: ON<br>Reference to F0                                 | -3.9  | -3.4  | -2.9  | dB   |
| T29  | Voltage gain<br>F3            | 14                             | 34B              | 38           | 41                   | V1 = 2kHz, TOG3: ON<br>Reference to F0                                 | -6.9  | -6.4  | -5.9  | dB   |
| T30  | Voltage gain<br>F4            | 14                             | 347              | 38           | 41                   | V1 = 2kHz, TOG4: ON<br>Reference to F0                                 | -11.1 | -10.6 | -10.1 | dB   |
| T31  | Voltage gain<br>E0            | 15                             | 34F<br>30F<br>00 | 39           | 41                   | V1 = 2kHz, BAL: OFF<br>I/O ratio                                       | -1.6  | 1.4   | 4.4   | dB   |
| T32  | Voltage gain<br>E1            | 15                             | 30E              | 39           | 41                   | V1 = 2kHz, BAL1: ON<br>Reference to E0                                 | 0.16  | 0.46  | 0.76  | dB   |
| T33  | Voltage gain<br>E2            | 15                             | 30D              | 39           | 41                   | V1 = 2kHz, BAL2: ON<br>Reference to E0                                 | 0.58  | 0.88  | 1.18  | dB   |
| T34  | Voltage gain<br>E3            | 15                             | 30B              | 39           | 41                   | V1 = 2kHz, BAL3: ON<br>Reference to E0                                 | 1.43  | 1.73  | 2.03  | dB   |
| T35  | Voltage gain<br>E4            | 15                             | 307              | 39           | 41                   | V1 = 2kHz, BAL4: ON<br>Reference to E0                                 | 2.96  | 3.26  | 3.56  | dB   |
| T36  | Max. output<br>voltage – High | 1                              | 34F<br>308       | 38           | 41                   | V1 = 1VDC, TOG: OFF,<br>BAL1, 2, 3: ON                                 | 0.5   | 0.7   | —     | V    |
| T37  | Max. output<br>voltage – Low  | 1                              | 34F<br>308       | 39           | 41                   | V1 = 1VDC, TOG: OFF,<br>BAL1, 2, 3: ON                                 | —     | -0.8  | -0.5  | V    |
| T38  | Output voltage<br>1           |                                | 3C4              | 35           | 34                   | I1 = 364 $\mu$ A   | -900  | -704  | -500  | mV   |
| T39  | Output voltage<br>2           |                                | 3C4              | 35           | 34                   | I1 = 439 $\mu$ A   | -693  | -293  | 107   | mV   |
| T40  | Output voltage<br>3           |                                | 3C4              | 35           | 34                   | I1 = 515 $\mu$ A   | 163   | 613   | 1063  | mV   |
| T41  | Output voltage<br>4           | 9                              | 3C4              | 35           | 34                   | 0.8mA sink   | -200  | 132   | 500   | mV   |
| T42  | LD OFF                        |                                | 3C0              | 35           | 34                   | I1 = 515 $\mu$ A,<br>LD: OFF   | 1.1   | 1.3   | —     | V    |

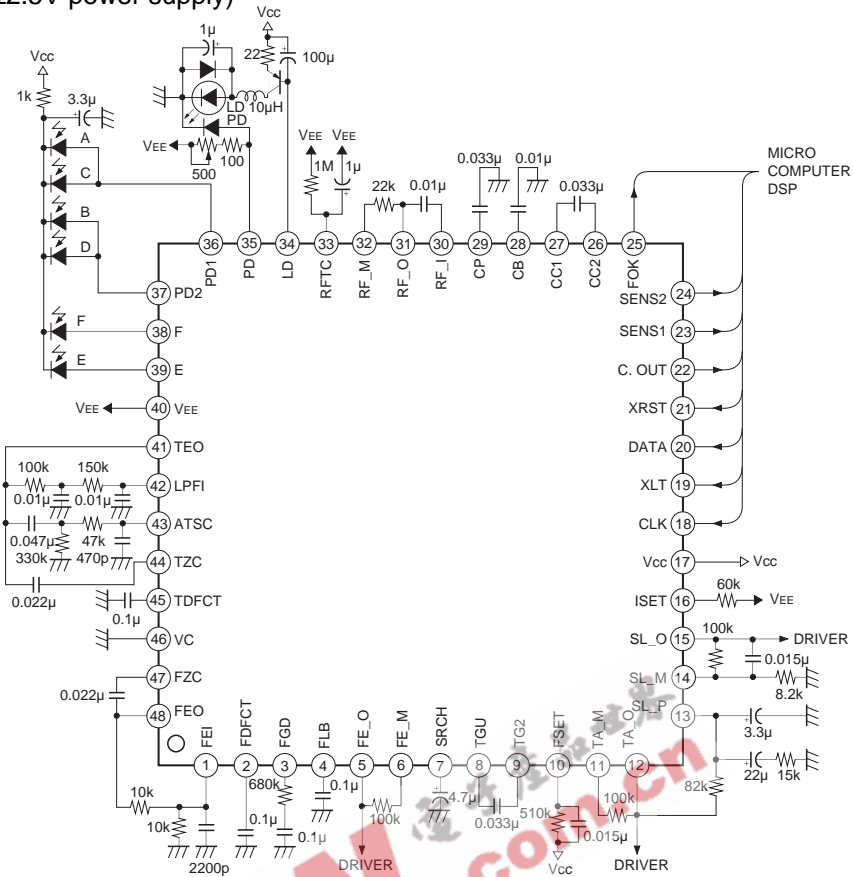
| TEST | Item                       | SW conditions (ON switches) | SD       | Input pin      | Measurement pin | Measurement conditions                                   | Min.  | Typ. | Max. | Unit |
|------|----------------------------|-----------------------------|----------|----------------|-----------------|--|-------|------|------|------|
| T43  | 50% limit                  | 8                           | 3C7      | 35<br>30       | 34              | I1 = 273 $\mu$ A<br>Output difference with LPC ON/OFF    | 725   | 1330 | 1935 | mV   |
| T44  | 17% limit                  | 8                           | 3C5      | 35<br>30       | 34              | I1 = 394 $\mu$ A<br>Output difference with LPC ON/OFF    | 476   | 886  | 1296 | mV   |
| T45  | -50% limit                 | 10, 13                      | 3C7      | 35<br>36<br>37 | 34              | I1 = 742 $\mu$ A<br>Output difference with LPC ON/OFF    | -1421 | -816 | -211 | mV   |
| T46  | -17% limit                 | 10, 13                      | 3C5      | 35<br>36<br>37 | 34              | I1 = 621 $\mu$ A<br>Output difference with LPC ON/OFF    | -803  | -393 | 17   | mV   |
| T47  | Direct voltage gain        | 1                           | 08       | 1              | 5               |  | 17.4  | 20.9 | 24.4 | dB   |
| T48  | FCS total gain             |                             | —        | —              | —               | T9 + T47   | 47.9  | 49.9 | 51.9 | dB   |
| T49  | Feed through 1             | 1                           | 00<br>08 | 1              | 5               | I/O gain difference between SD = 00 and SD = 08.         | —     | —    | -30  | dB   |
| T50  | FZC threshold              | 18                          | 00       | 47             | 47              | Pin 47 voltage when SENS1 (Pin 23) goes from Low to High | 191   | 231  | 271  | mV   |
| T51  | Max. output voltage – High | 1                           | 08       | 1              | 5               | V1 = 200mVDC   | 1     | 1.3  | —    | V    |
| T52  | Max. output voltage – Low  | 1                           | 08       | 1              | 5               | V1 = -200mVDC  | —     | -1.3 | -1   | V    |
| T53  | Search voltage (-)         |                             | 02       | —              | 5               |  | -721  | -581 | -441 | mV   |
| T54  | Search voltage (+)         |                             | 03       | —              | 5               |  | 399   | 539  | 679  | mV   |
| T55  | Direct voltage gain        |                             | 25       | 38             | 12              | DC gain between TEO and TA_O                             | 11.4  | 14.6 | 17.8 | dB   |
| T56  | TRK total gain             |                             | —        | —              | —               | T26 + T55  | 16.8  | 18.8 | 20.8 | dB   |
| T57  | Feed through 1             |                             | 20<br>25 | 38             | 12              | Output gain difference between SD = 20 and SD = 25.      | —     | —    | -39  | dB   |
| T58  | Max. output voltage – High |                             | 20<br>25 | 38             | 12              | V1 = -0.3VDC   | 1     | 1.3  | —    | V    |
| T59  | Max. output voltage – Low  |                             | 20<br>25 | 38             | 12              | V1 = 0.3VDC  | —     | -1.3 | -1   | V    |
| T60  | Jump output voltage (-)    |                             | 2C       |                | 12              |  | -652  | -512 | -372 | mV   |
| T61  | Jump output voltage (+)    |                             | 28       |                | 12              |  | 437   | 577  | 717  | mV   |
| T62  | ATSC threshold (-)         | 5, 17                       | 10       | 43             | 43              | Input voltage when TG2 (Pin 9) goes from Vcc/2 to Vcc    | -25   | -15  | -7   | mV   |
| T63  | ATSC threshold (+)         | 5, 17                       | 10       | 43             | 43              | Input voltage when TG2 (Pin 9) goes from Vcc/2 to Vcc    | 7     | 15   | 25   | mV   |
| T64  | TZC threshold              | 18                          | 20       | 44             | 44              | Pin 44 voltage when SENS1 (Pin 23) is 0V                 | -20   | 0    | 20   | mV   |

| TEST | Item                              | SW conditions<br>(ON switches) | SD         | Input<br>pin | Measure-<br>ment pin | Measurement<br>conditions                                   | Min. | Typ. | Max. | Unit |
|------|-----------------------------------|--------------------------------|------------|--------------|----------------------|---|------|------|------|------|
| T65  | BAL COMP<br>threshold – High      | 16                             | 300        | 42           | 42                   | Pin 42 voltage when SENS1<br>(Pin 23) goes from High to Low | 5    | 20   | 35   | mV   |
| T66  | BAL COMP<br>threshold – Low       | 16                             | 300        | 42           | 42                   | Pin 42 voltage when SENS2<br>(Pin 24) goes from High to Low | -35  | -20  | -5   | mV   |
| T67  | GAIN COMP<br>threshold – High     | 14                             | 308<br>34F | 38           | 41                   | Pin 41 voltage when SENS1<br>(Pin 23) goes from High to Low | 168  | 193  | 218  | mV   |
| T68  | GAIN COMP<br>threshold – Low      | 14                             | 308<br>34F | 38           | 41                   | Pin 41 voltage when SENS2<br>(Pin 24) goes from Low to High | 127  | 145  | 163  | mV   |
| T69  | FOK<br>threshold                  | 8                              | —          | 30           | 25                   | Pin 30 voltage when<br>Pin 25 is 0V                         | -400 | -367 | -330 | mV   |
| T70  | Voltage gain                      | 6, 7                           | 25         | 13           | 15                   | V1 = 100Hz, I/O ratio                                       | 50   | —    | —    | dB   |
| T71  | Feed through                      | 6                              | 20<br>25   | 13           | 15                   | Output gain difference between<br>SD = 20 and SD = 25.      | —    | —    | -34  | dB   |
| T72  | Max. output<br>voltage – High     | 6                              | 25         | 13           | 15                   | V1 = 400mVDC  | 1    | 1.3  | —    | V    |
| T73  | Max. output<br>voltage – Low      | 6                              | 25         | 13           | 15                   | V1 = 400mVDC  | —    | -1.3 | -1   | V    |
| T74  | Kick voltage 1                    |                                | 20         | —            | 15                   | REV × 1   | -750 | -600 | -450 | mV   |
| T75  | Kick voltage 2                    |                                | 20         | —            | 15                   | FWD × 1   | 450  | 600  | 750  | mV   |
| T76  | Max. operating<br>frequency 1     | 8                              | 20         | 30           | 24                   | Measures at SENS2<br>pin.                                   | 30   | —    | —    | kHz  |
| T77  | Min. input<br>operating voltage 1 | 8                              | 20         | 30           | 24                   | Measures at SENS2<br>pin.                                   | —    | —    | 0.3  | Vp-p |
| T78  | Max. input<br>operating voltage 1 | 8                              | 20         | 30           | 24                   | Measures at SENS2<br>pin.                                   | 1.8  | —    | —    | Vp-p |
| T79  | Min. operating<br>frequency 1     | 10, 11, 12,<br>13              | 10         | 36<br>37     | 23                   | Measures at SENS1<br>pin.                                   | —    | —    | 1    | kHz  |
| T80  | Max. operating<br>frequency 1     | 10, 11, 12,<br>13              | 10         | 36<br>37     | 23                   | Measures at SENS1<br>pin.                                   | 2.5  | —    | —    | kHz  |
| T81  | Min. input<br>operating voltage 1 | 10, 11, 12,<br>13              | 10         | 36<br>37     | 23                   | Measures at SENS1<br>pin.                                   | —    | —    | 0.5  | Vp-p |
| T82  | Max. input<br>operating voltage 1 | 10, 11, 12,<br>13              | 10         | 36<br>37     | 23                   | Measures at SENS1<br>pin.                                   | 1.8  | —    | —    | Vp-p |

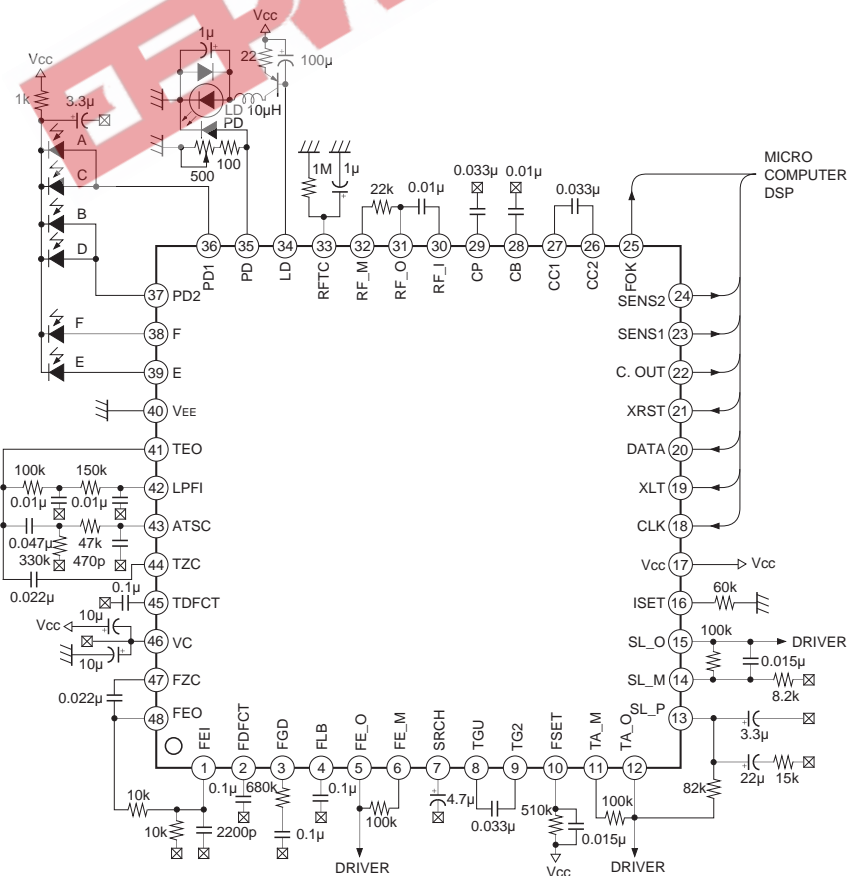
Electrical Characteristics Measurement Circuit



Application Circuit 1 ( $\pm 2.5V$  power supply)



Application Circuit 2 (Single +5V power supply)

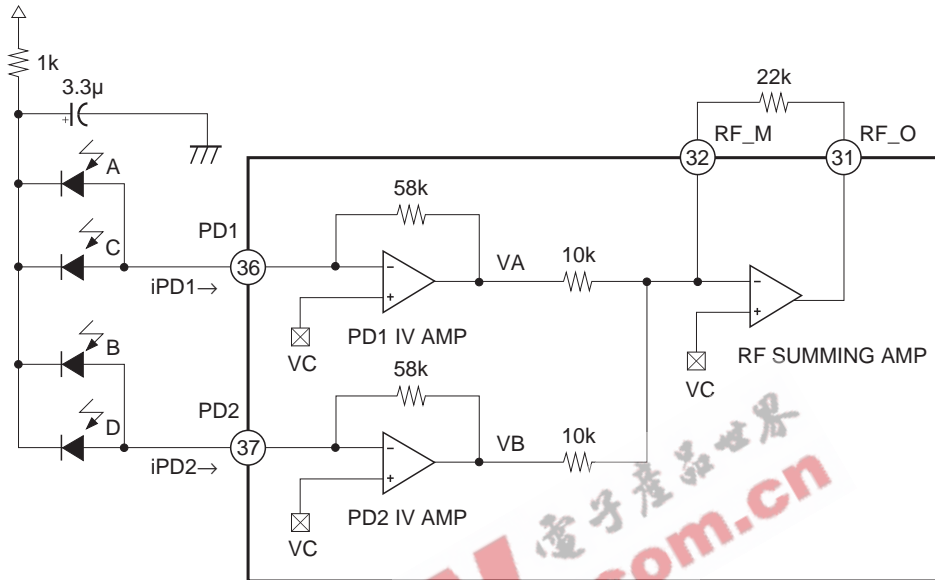


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Description of Functions**

**RF Amplifier**

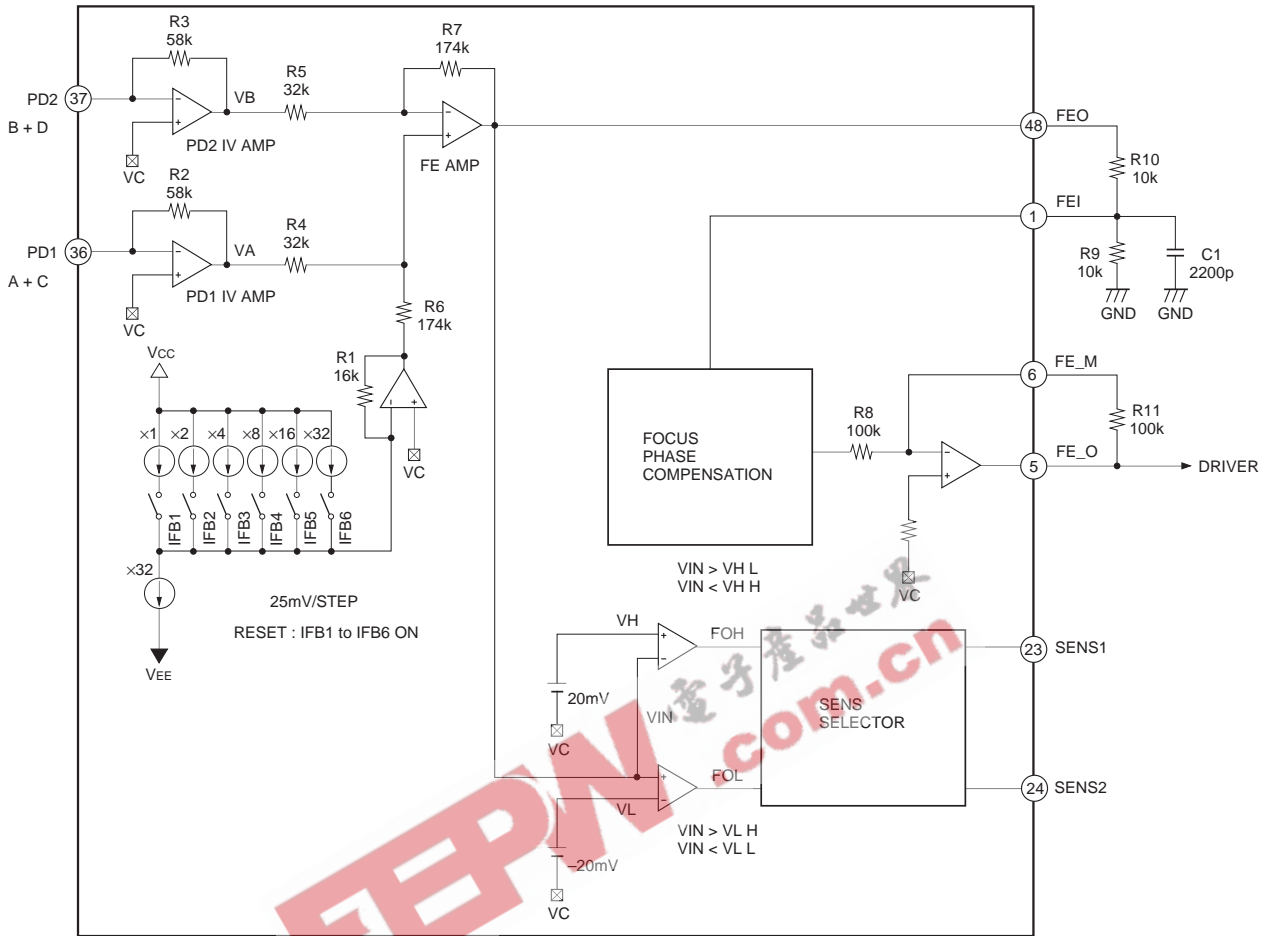
The photodiode currents input to the input pins (PD1 and PD2) are each I-V converted through a 58kΩ equivalent resistor by the PD I-V amplifiers. These signals are added by the RF summing amplifier, and the photodiode (A + B + C + D) current-voltage converted voltage is output to the RFO pin. An eye-pattern check can be performed at this pin.



The low frequency component of the RFO output voltage is  $V_{RFO} = -2.2 \times (V_A + V_B) = 127.6k\Omega \times (i_{PD1} + i_{PD2})$ .



Focus Error Amplifier



The focus error amplifier calculates the difference between output VA and VB of the RF I-V amplifier, and output current-voltage converted voltage of the photodiode (A + C – B – D).

The FEO output voltage:

$$\begin{aligned}
 V_{FEO} &= \frac{174k\Omega}{32k\Omega} (VA - VB) \\
 &= \frac{174k\Omega}{32k\Omega} \{(-58k\Omega \times i_{PD1}) - (-58k\Omega \times i_{PD2})\} \\
 &= 315.4k\Omega (i_{PD2} - i_{PD1})
 \end{aligned}$$

The focus error amplifier has a built-in bias adjustment circuit to enable software-based automatic adjustment. The focus bias adjustment is performed by turning the focus bias adjustment switches (IFB1 to IFB6) ON and OFF.

The 6-bit focus bias adjustment switches are controlled with commands.

IFB1 to IFB6 are all ON after a reset.

The voltage is varied by approximately 25mV per step.

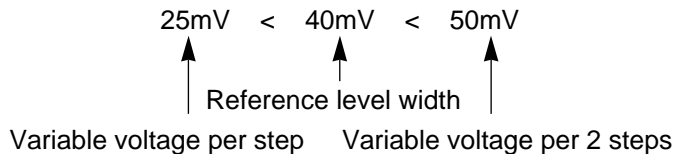
### • Focus error amplifier offset adjustment (when adjusting the IC offset)

The offset adjustment is performed by comparing the FEO when the focus servo is OFF with the reference level.

The FEO and reference level are compared by the window comparator, and the comparison results are output from SENS1 and SENS2. (ADDRESS  $D^{11}001110^{D6}$ )

Adjust the offset so that SENS1 and SENS2 are both High.

Set the reference level to the center  $\pm 20\text{mV}$ .



### • Focus bias fine adjustment

Fine adjustment is performed by turning the focus bias adjustment switches (IFB1 to IFB6) ON and OFF while monitoring a DSP jitter meter with the microcomputer.

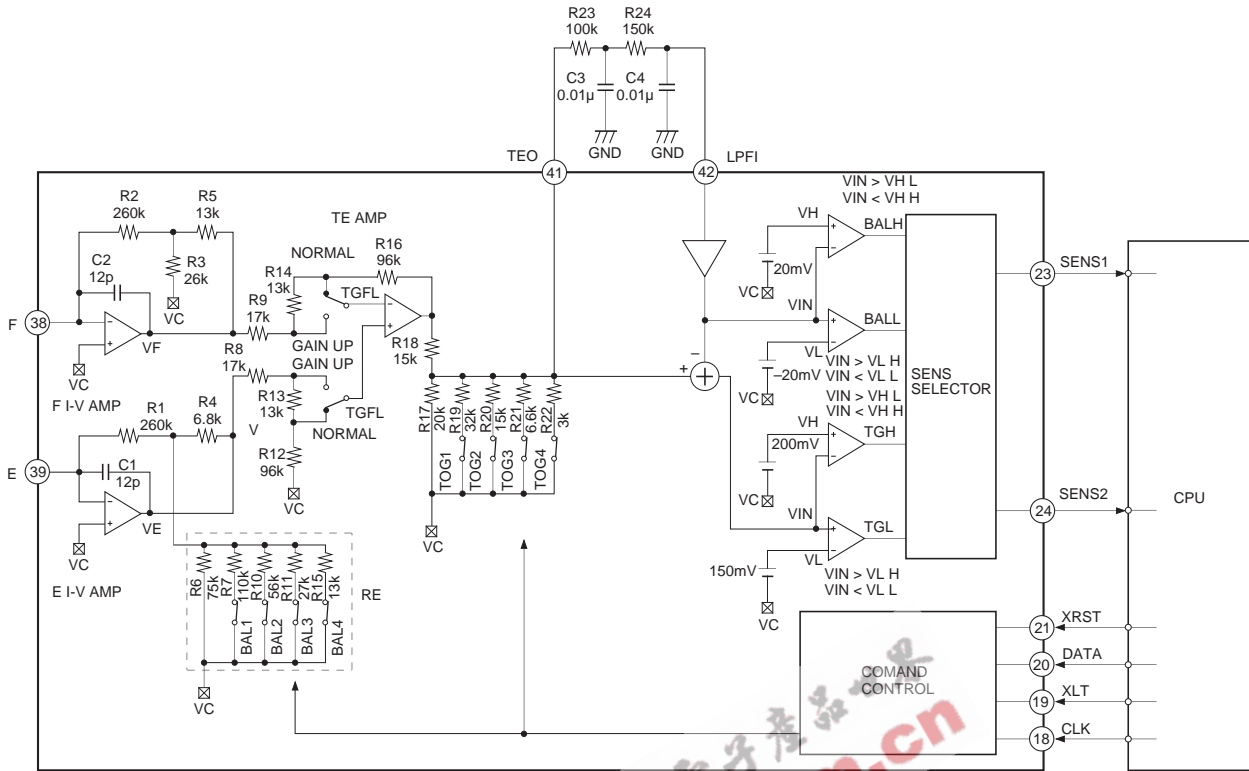
The 6-bit focus bias adjustment switches are controlled with commands.

### • When performing conventional focus bias adjustment

Fix the focus bias adjustment switches to the desired settings. (for example, IFB6 ON)

In this condition, adjust the focus bias by turning a volume connected to FE\_BIAS (Pin 40).

Tracking Error Amplifier



The difference between E I-V amplifier output VE and F I-V amplifier output VF is taken and output from TEO.

The tracking error amplifier has built-in balance and gain adjustment circuits to enable software-based automatic adjustment.

The balance adjustment is performed by varying the combined resistance value of the T-configured feedback resistance at the E I-V amplifier.

$$\text{E I-V AMP feedback resistance} = R1 + R4 + \frac{R1 \times R4}{RE}$$

$$\text{F I-V AMP feedback resistance} = R2 + R5 + \frac{R2 \times R5}{R3} = 403k\Omega$$

Vary the combined resistance value of the E I-V amplifier's feedback resistance by using the balance adjustment switches (BAL1 to BAL4).

The gain adjustment is performed by resistance dividing the TE AMP output by the gain adjustment switches (TOG1 to TOG4).

The balance and gain adjustment switches are controlled with commands.

Set the cut-off frequency of the external LPF between 10Hz to 100Hz.

• Balance adjustment

The balance adjustment is performed by passing the tracking error signal (TEO signal) through the external LPF, extracting the offset DC, and comparing it to the reference level.

However, the TEO signal frequency distribution ranges from DC to 2kHz. Merely sending the signal through the LPF leaves lower frequency components, and the complete offset DC can not be extracted.

To extract it, monitor the TEO signal frequency at all times, and perform adjustment only when a frequency that can lower a sufficient gain appears on the LPF.

Use the C.OUT output to check this frequency.

The offset DC and reference level are compared by the window comparator.

The comparison signal is output from the SENS1 and SENS2 pins. (ADDRESS <sup>D11</sup>001100<sup>D6</sup>)

Adjust the balance so that the SENS1 and SENS2 pins are both High.

|                   | $V_{IN} < V_L < V_H$ | $V_L < V_{IN} < V_H$ | $V_L < V_H < V_{IN}$ |
|-------------------|----------------------|----------------------|----------------------|
| SENS1 pin<br>BALH | H                    | H                    | L                    |
| SENS2 pin<br>BALL | L                    | H                    | H                    |

V<sub>H</sub>: High level threshold value

V<sub>IN</sub>: Window comparator input signal

V<sub>L</sub>: Low level threshold value

• Gain adjustment

Gain adjustment is performed by passing the TEO signal through the HPF and comparing the AC component to the reference level.

The AC component is generated by taking the difference between TE and the offset DC input to Pin 42.

The AC component and reference level are compared by the window comparator.

The comparison signal is output from the SENS1 and SENS2 pins. (ADDRESS <sup>D11</sup>001101<sup>D6</sup>)

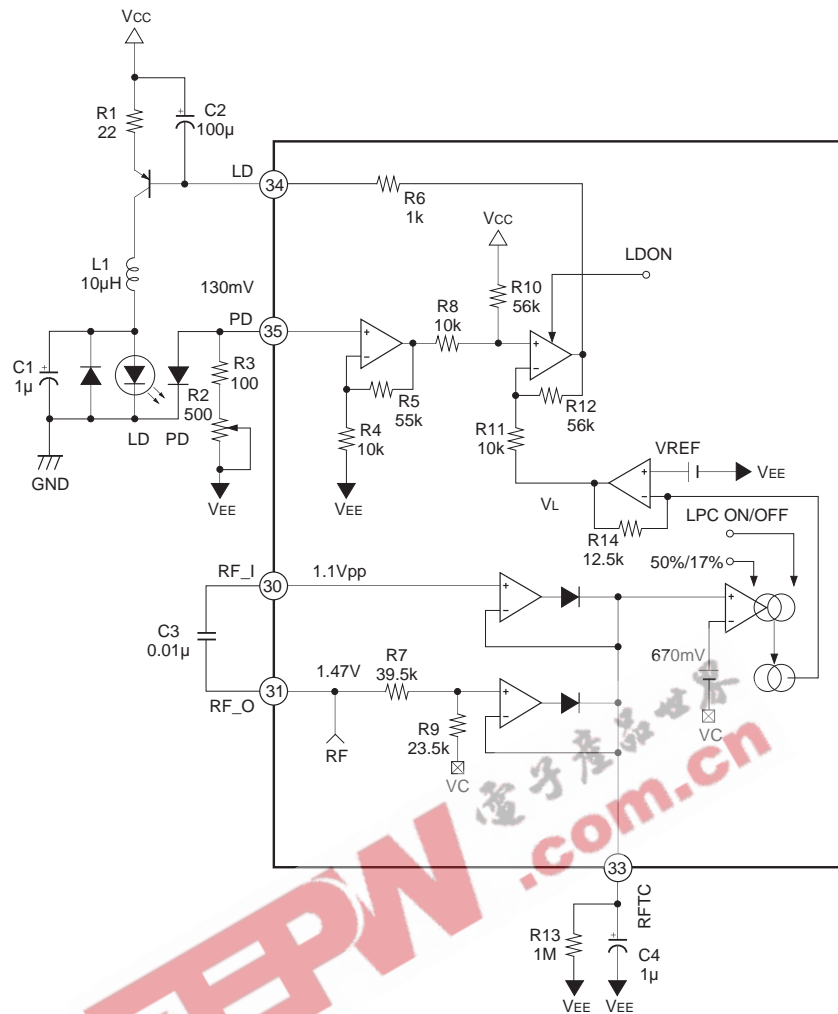
The comparison signal is as follows.

|                  | (1) | (2)  | (3)  |
|------------------|-----|------|------|
|                  |     |      |      |
| SENS1 pin<br>TGH | H   | H    | Low  |
| SENS1 pin<br>TGL | L   | High | High |

The gain should be adjusted so that the SENS1 and SENS2 pins are as shown in status (2).

When the TEO signal level is low and TGH (SENS1 pin) does not go Low, the gain should be raised with the TGFL command for adjustment. If the adjustment does not bring the result of Low, check the pulse duty of TGL (SENS2 pin).

APC & Laser Power Control



• APC

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics.

The APC circuit is used to maintain the optical power output at a constant level.

The laser diode current is controlled according to the monitor photodiode output.

• Laser power control

The RF level is stabilized by attaching an offset to the APC VL and controlling the laser power in sync with the RF level fluctuations.

The RF\_O and RF\_I levels are compared and the larger of the two is smoothed by the RFTC's external CR.

This signal is then compared with the reference level.

The laser power is controlled by attaching an offset to VL according to the results of comparison with the reference level.

Set the reference level to 670mV. (center voltage reference)

LPC ON/OFF and LD ON/OFF control is performed with commands.

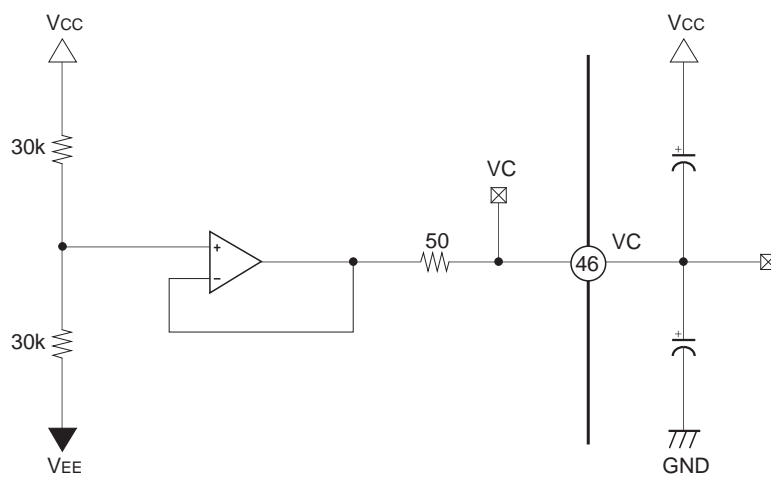
The laser power control limit can also be switched between ±50% and ±17% with commands.

| LPC | LPCL | VL variable range           |
|-----|------|-----------------------------|
| OFF | —    | Approximately 1.27V         |
| ON  | ±50% | Approximately 1.27V ± 625mV |
| ON  | ±17% | Approximately 1.27V ± 208mV |

**Center Voltage Generation Circuit**

(The figure below shows a single voltage application; Connect to GND for dual power supplies.)

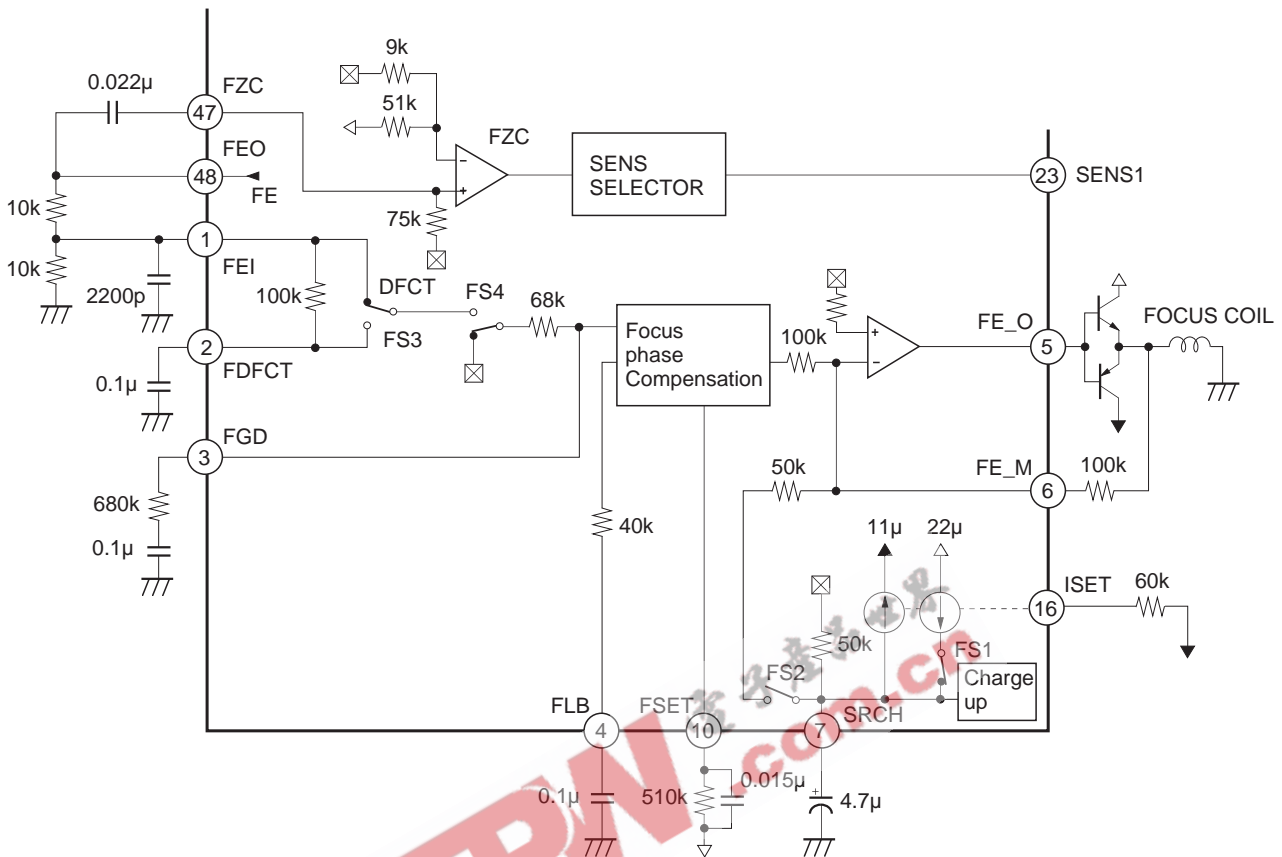
Maximum current is approximately  $\pm 3\text{mA}$ . Output impedance is approximately  $50\Omega$ .



Connected internally to the VEE pin.

EEPW 电子产品世界 .com.cn

Focus Servo



The above figure shows a block diagram of the focus servo.

Ordinarily the FE signal is input to the focus phase compensation circuit through a 68kΩ resistance; however, when DFCT is detected, the FE signal is switched to pass through a low-pass filter formed by the internal 100kΩ resistance and the capacitance connected to Pin 2. When this DFCT prevention circuit is not used, leave Pin 2 open. The defect switch operation can be enabled and disabled with command.

The capacitor connected between Pin 4 and GND is a time constant to boost the low frequency in the normal playback state.

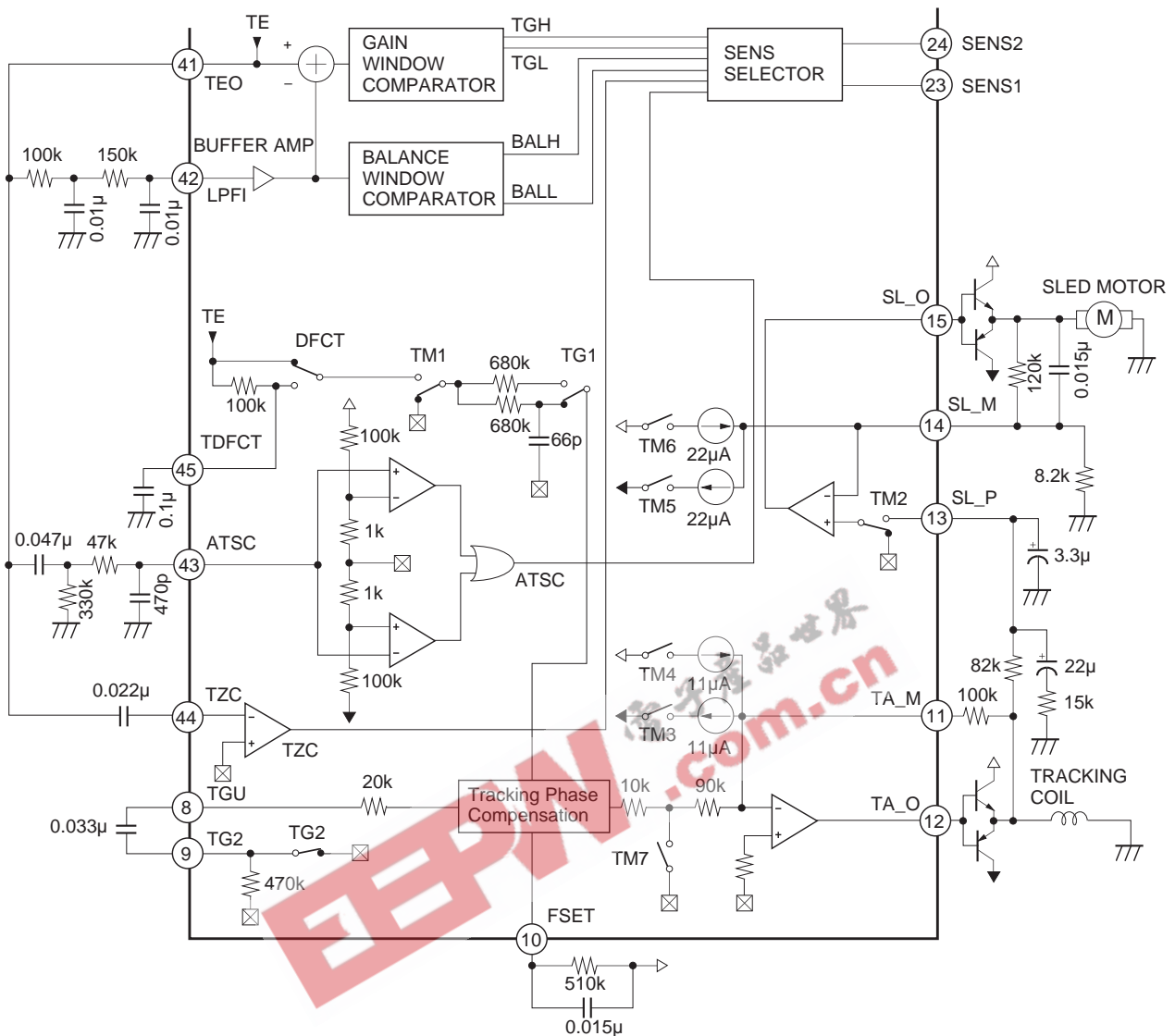
The peak frequency of the focus phase compensation is approximately 1.2kHz when a resistance of 510kΩ is connected to Pin 10.

The focus search height is approximately ±1.1Vp-p when using the constants indicated in the above figure. This height is inversely proportional to the resistance connected between Pin 17 and V<sub>EE</sub>. However, changing this resistance also changes the height of the track jump and sled kick as well.

The FZC comparator inverted input is set to 15% of V<sub>cc</sub> and VC (Pin 46);  $(V_{cc} - VC) \times 15\%$ .

\* 510kΩ resistance is recommended for Pin 10.

Tracking and Sled Servo



The above figure shows a block diagram of the tracking and sled servo.

The capacitor connected between Pins 8 and 9 is a time constant to cut the high-frequency gain when TG2 is OFF. The peak frequency of the tracking phase compensation is approximately 1.2kHz when a 510kΩ resistance is connected to Pin 10. In the CXA2542Q, TG1 and TG2 are inter-linked switches.

To jump tracks in FWD and REV directions, turn TM3 or TM4 ON. During this time, the peak voltage applied to the tracking coil is determined by the TM3 or TM4 current and the feedback resistance from Pin 11. To be more specific,

$$\text{Track jump peak voltage} = \text{TM3 (or TM4) current} \times \text{feedback resistance value}$$

The FWD and REV sled kick is performed by turning TM5 or TM6 ON. During this time, the peak voltage applied to the sled motor is determined by the TM5 or TM6 current and the feedback resistance from Pin 14;

$$\text{Sled kick peak voltage} = \text{TM5 (or TM6) current} \times \text{feedback resistance}$$

The values of the current for each switch are determined by the resistance connected between Pin 16 and V<sub>EE</sub>. When this resistance is 60kΩ :

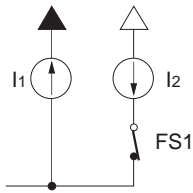
$$\text{TM3 (or TM4)} = \pm 11\mu\text{A}, \text{ and TM5 (or TM6)} = \pm 22\mu\text{A}.$$

As is the case with the FE signal, the TE signal is switched to pass through a low-pass filter formed by the internal resistance (100kΩ) and the capacitance connected to Pin 45.



The ISET pin is used to connect external resistance. This external resistance sets the current which determines the focus search, track jump, and sled kick heights.

- Focus search current



$$I_1 = \frac{V_{BG}}{R} \times \frac{1}{2} \quad (V_{BG}: \text{approximately } 1.27V)$$

$$I_2 = 2I_1$$

- Track jump current (TM3 and TM4 current)

$$I = \frac{V_{BG}}{R} \times \frac{1}{2}$$

- Sled kick current (TM5 and TM6 current, when D1 = D0 = 0 during 1X\$ commands)

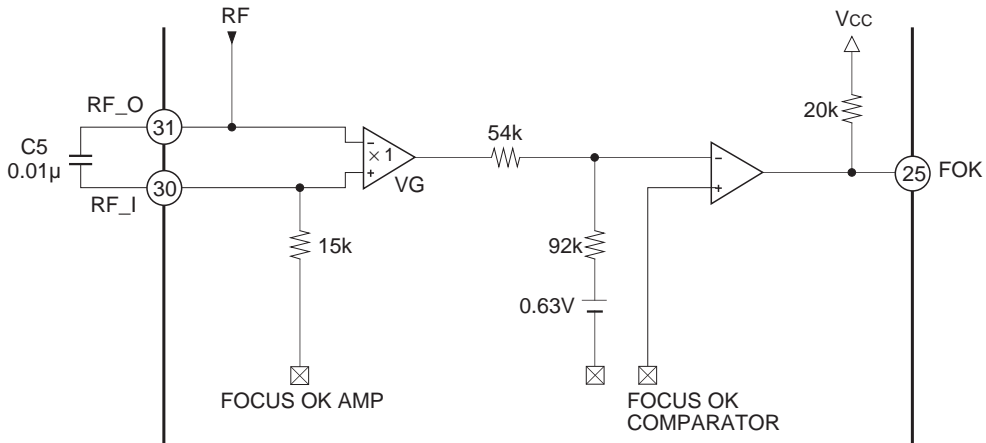
$$I = \frac{V_{BG}}{R}$$

Use external resistance of between 30kΩ to 240kΩ.

Using external resistance outside this range may cause oscillation.

EEPW.com.cn 电子产品世界

Focus OK Circuit



The focus OK circuit creates the timing window okaying the focus servo from the focus search state. The HPF output is obtained at Pin 30 from Pin 31 (RF signal), and the LPF output (opposite phase) of the focus OK amplifier output is also obtained.

The focus OK output is inverted when  $V_{RFI} - V_{RFO} \approx -0.37V$ .

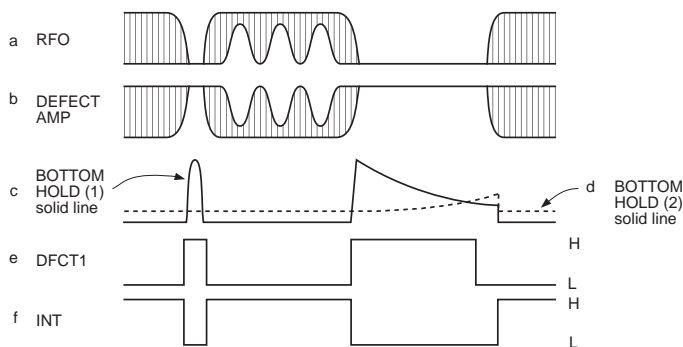
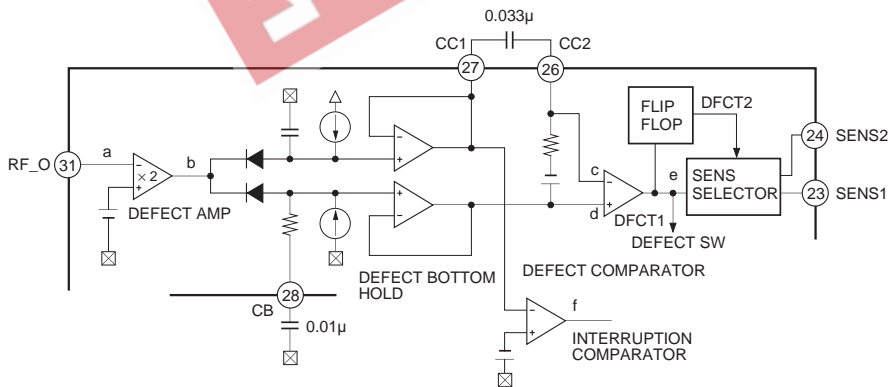
Note that, C5 determines the time constant of the HPF for the mirror circuit and the LPF of the focus OK amplifier. Ordinarily, with a C5 equal to 0.01µF selected, the  $f_c$  is equal to 1kHz, and block error rate degradation brought about by RF envelope defects caused by scratched discs can be prevented.

Defect circuit

After inversion, RF\_O signal is bottom held by means of the long and short time constants. The long time-constant bottom hold keeps the mirror level prior to the defect.

The short time-constant bottom hold responds to a disc mirror defect in excess of 0.1ms, and this is defferentiated and level-shifted through the AC coupling circuit.

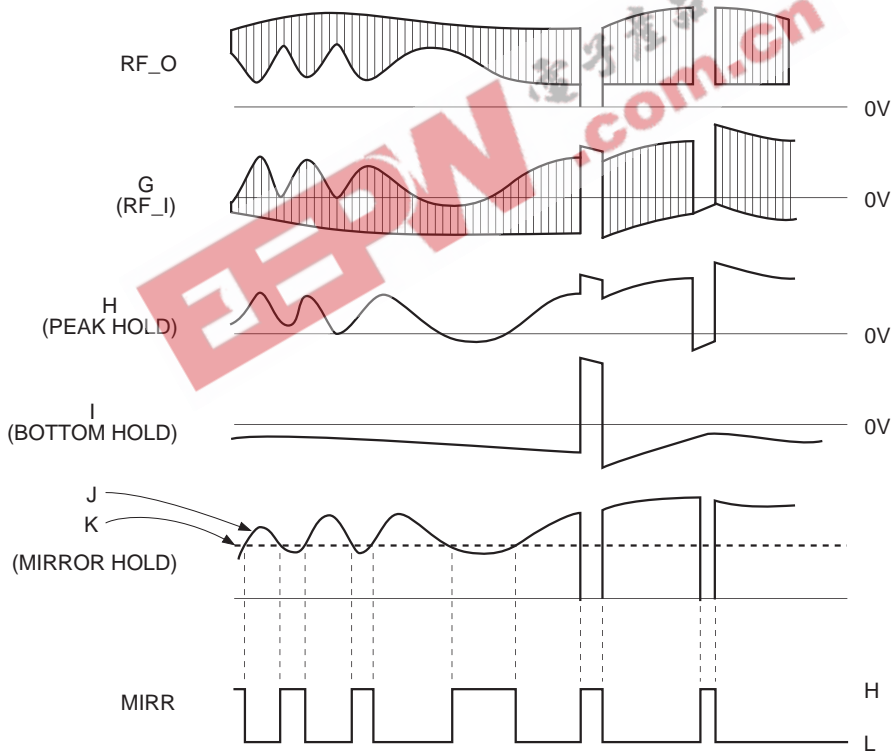
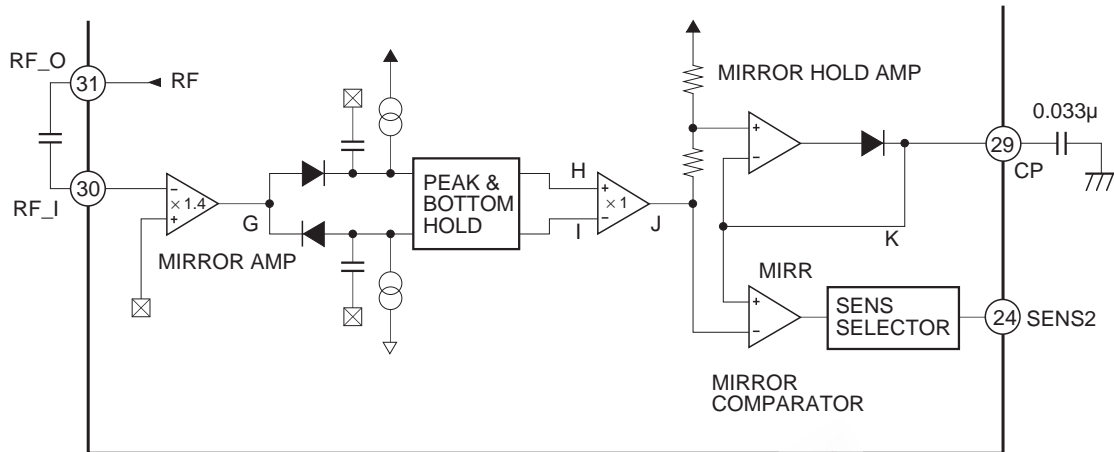
The long and short time-constant signals are compared to generate at mirror defect detection signal.



**Mirror Circuit**

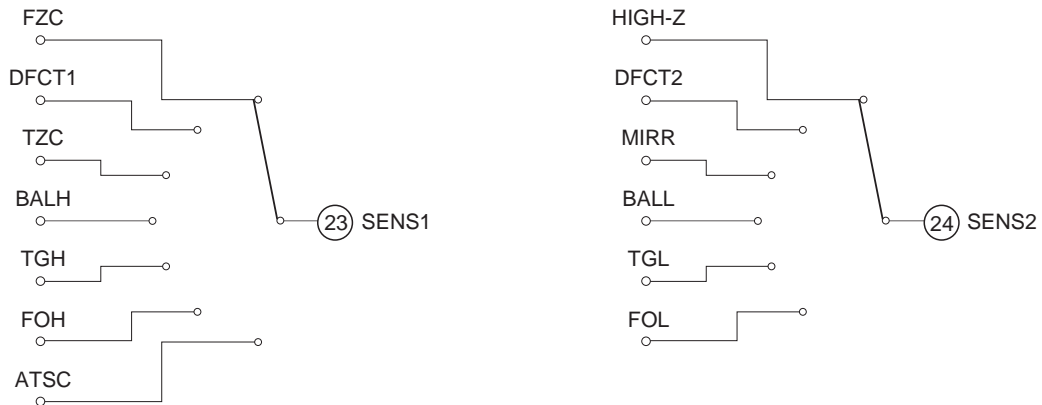
The mirror circuit performs peak and bottom hold after the RFI signal has been amplified.

The peak and bottom holds are both held through the use of a time constant. For the peak hold, a time constant can follow a 30kHz traverse, and, for the bottom hold, one can follow the rotation cycle envelope fluctuation.



The DC playback envelope signal J is obtained by amplifying the difference between the peak and bottom hold signals H and I. Signal J has a large time constant of 2/3 its peak value, and the mirror output is obtained by comparing it to the peak hold signal K. Accordingly, when on the disc track, the mirror output is Low; when between tracks (mirrored portion), it is High; and when a defect is detected, it is High. The mirror hold time constant must be sufficiently large compared with the traverse signal.

**SENS Selector**



What is output to the SENS1 and SENS2 pins varies according to the address input to the DATA pin.

| DATA (Pin 20) 8-bit transfer |    |    |    |      |    |    |    | SENS1      | SENS2      |
|------------------------------|----|----|----|------|----|----|----|------------|------------|
| ADDRESS                      |    |    |    | DATA |    |    |    |            |            |
| D7                           | D6 | D5 | D4 | D3   | D2 | D1 | D0 |            |            |
| 0                            | 0  | 0  | 0  | X    | X  | X  | X  | FZC        | H (HIGH-Z) |
| 0                            | 0  | 0  | 1  | X    | X  | X  | X  | DFCT1      | DFCT2      |
| 0                            | 0  | 1  | 0  | X    | X  | X  | X  | TZC        | MIRR       |
| 0                            | 1  | 0  | 0  | X    | X  | X  | X  | H (HIGH-Z) | H (HIGH-Z) |
| 1                            | 1  | 1  | 1  | X    | X  | X  | X  | H (HIGH-Z) | H (HIGH-Z) |

| DATA (Pin 20) 12-bit transfer |     |    |    |    |    |      |    |    |    |    |    | SENS1 | SENS2      |
|-------------------------------|-----|----|----|----|----|------|----|----|----|----|----|-------|------------|
| ADDRESS                       |     |    |    |    |    | DATA |    |    |    |    |    |       |            |
| D11                           | D10 | D9 | D8 | D7 | D6 | D5   | D4 | D3 | D2 | D1 | D0 |       |            |
| 0                             | 0   | 1  | 1  | 0  | 0  | X    | X  | X  | X  | X  | X  | BALH  | BALL       |
| 0                             | 0   | 1  | 1  | 0  | 1  | X    | X  | X  | X  | X  | X  | TGH   | TGL        |
| 0                             | 0   | 1  | 1  | 1  | 0  | X    | X  | X  | X  | X  | X  | FOH   | FOL        |
| 0                             | 0   | 1  | 1  | 1  | 1  | X    | X  | X  | X  | X  | X  | ATSC  | H (HIGH-Z) |

**Notes)**

- 12-bit transfer should be performed during \$3XX commands. When 8 bits are transferred, SENS1 and SENS2 are switched according to the D3 and D2 data.
- SENS1 and SENS2 are switched without latching.

**Commands**

The input data to operate this IC is configured as 8-bit/12-bit data; however, below, this input data is represented by 2-digit hexadecimal numerals in the form \$XX, where X is a hexadecimal numeral between 0 and F/\$XXX for 12-bit.

Commands for the CXA2542Q can be broadly divided into four groups ranging in value from \$0X, \$1X, \$2X, \$3XX.

**1. \$0X (FZC at SENS1 pin (Pin 23), H (Hi-Z) at SENS2 pin (Pin 24))**

These commands are related to focus servo control.

The bit configuration is as shown below.

|    |    |    |    |     |    |     |     |
|----|----|----|----|-----|----|-----|-----|
| D7 | D6 | D5 | D4 | D3  | D2 | D1  | D0  |
| 0  | 0  | 0  | 0  | FS4 | —  | FS2 | FS1 |

Four focus related switches exist: FS1, FS2, FS4 and DFCT.

\$00 When FS1 = 0, Pin 7 is charged to  $(22\mu\text{A} - 11\mu\text{A}) \times 50\text{k}\Omega = 0.55\text{V}$ .

If, in addition, FS2 = 0, this voltage is no longer transferred, and the output at Pin 5 becomes 0V.

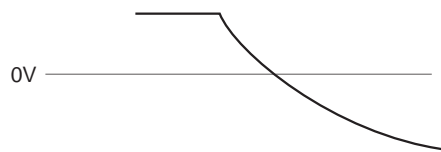
\$02 From the state described above, the only FS2 becomes 1. When this occurs, a negative signal is output to Pin 5. This voltage level is obtained by equation 1 below.

$$(22\mu\text{A} - 11\mu\text{A}) \times 50\text{k}\Omega \times \frac{\text{resistance between Pins 5 and 6}}{50\text{k}\Omega} \dots \text{Equation 1}$$

The SRCH DOWN speed can be increased by the charge up circuit.

\$03 From the state described above, FS1 becomes 1, and a current source of +22μA is split off.

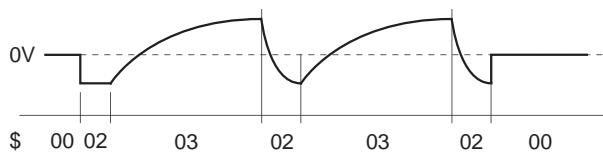
Then, a CR charge/discharge circuit is formed, and the voltage at Pin 7 decreases with the time as shown in Fig. 1 below.



**Fig. 1. Voltage at Pin 7 when FS1 goes from 0 → 1**

This time constant is obtained with the 50kΩ resistance and an external capacitor.

By alternating the commands between \$02 and \$03, the focus search voltage can be constructed. (Fig. 2)



**Fig. 2. Constructing the search voltage by alternating between \$02 and \$03. (Voltage at Pin 5)**

**1-1. FS4**

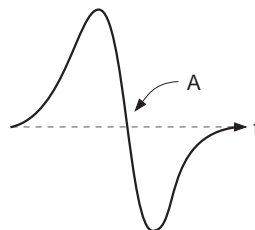
This switch is provided between the focus error input and the focus phase compensation, and is in charge of turning the focus servo ON and OFF.

\$00 → \$08  
 Focus off      Focus on

**1-2. Procedure of focus activation**

For description, suppose that the polarity is as described below.

- a) The lens is searching the disc from far to near;
- b) The output voltage (Pin 5) is changing from negative to positive; and
- c) The focus S-curve is varying as shown below.

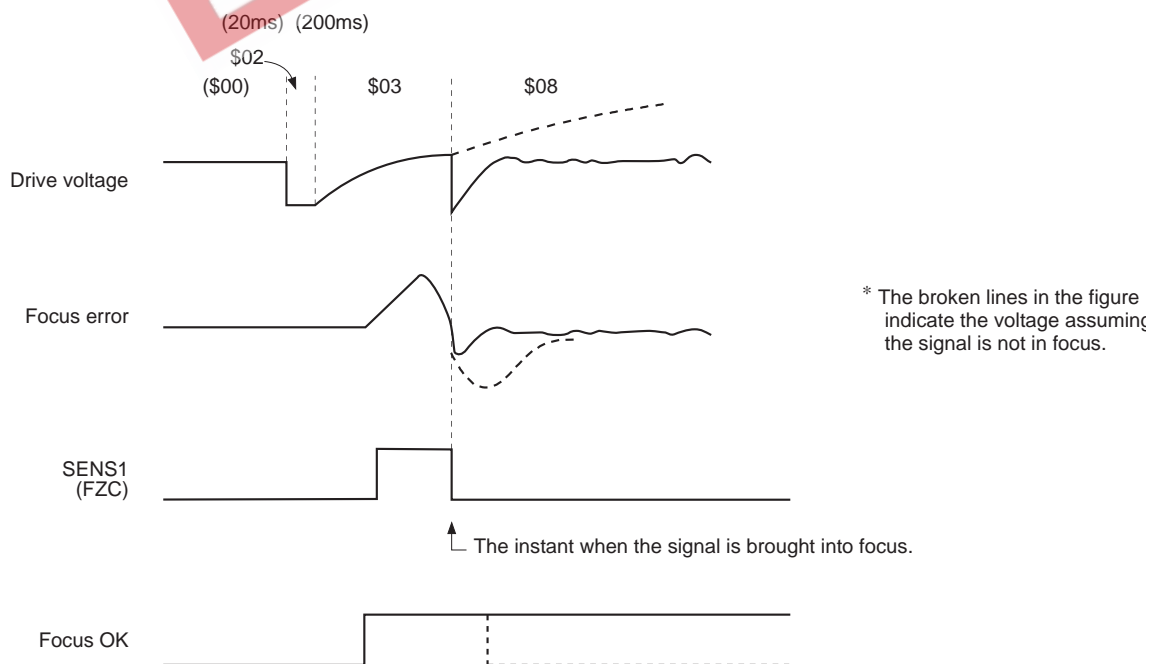


**Fig. 3. S-curve**

The focus servo is activated at the operating point indicated by A in Fig. 3. Ordinarily, focus searching and the turning the focus servo switch ON are performed during the focus S-curve transits the point A indicated in Fig. 3. To prevent misoperation, this signal is ANDed with the focus OK signal.

In this IC, FZC (Focus Zero Cross) signal is output from the SENS1 pin (Pin 23) as the point A transit signal. In addition, focus OK is output as a signal indicating that the signal is in focus (can be in focus in this case).

Following the line of the above description, focusing can be well obtained by observing the following timing chart.



\* The broken lines in the figure indicate the voltage assuming the signal is not in focus.

**Fig. 4. Focus ON timing chart**

Note that the time from the High to Low transition of FZC to the time command \$08 is asserted must be minimized. To do this, the software sequence shown in B is better than the sequence shown in A.

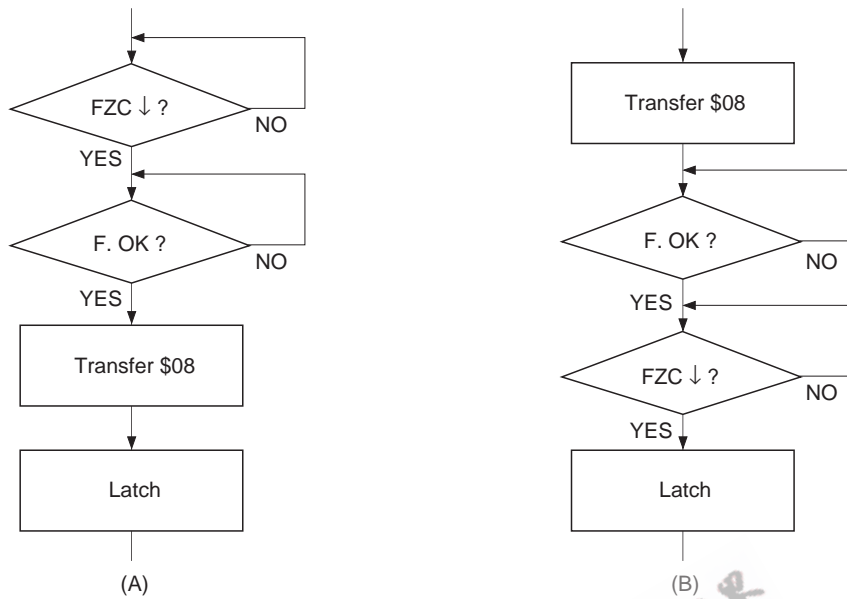


Fig. 5. Poor and good software command sequences

2. \$1X (DFCT1 at SENS1 pin (Pin 23), DFCT2 at SENS2 pin (Pin 24))

These commands deal with switching TG1/TG2, brake circuit ON/OFF, and the sled kick output.

The bit configuration is as follows:

|    |    |    |    |          |         |           |    |
|----|----|----|----|----------|---------|-----------|----|
| D7 | D6 | D5 | D4 | D3       | D2      | D1        | D0 |
| 0  | 0  | 0  | 1  | TG1, TG2 | Break   | Sled kick |    |
|    |    |    |    | ON/OFF   | circuit | height    |    |
|    |    |    |    | ON/OFF   | ON/OFF  |           |    |

| Sled kick height |          | Relative value |
|------------------|----------|----------------|
| D1 (PS1)         | D0 (PS0) |                |
| 0                | 0        | ±1             |
| 0                | 1        | ±2             |
| 1                | 0        | ±3             |
| 1                | 1        | ±4             |

TG1, TG2, TM7

The purpose of TG1 and TG2 is to switch the tracking servo gain Up/Normal. TG1 and TG2 are interlinked switches. The brake circuit (TM7) is to prevent the frequently occurred phenomena where the merely 10-track jump has been performed actually though a 100-track jump was intended to be done due to the extremely degraded actuator settling caused by the servo motor exceeding the linear range after a 100 or 10-track jump. For the prevention method, when the actuator travels radially; that is, when it traverses from the inner track to the outer track of the disc and vice versa, the brake circuit utilizes the fact that the phase relationship between the RF envelope and the tracking error is 180° out-of-phase to cut the unneeded portion of the tracking error and apply braking.

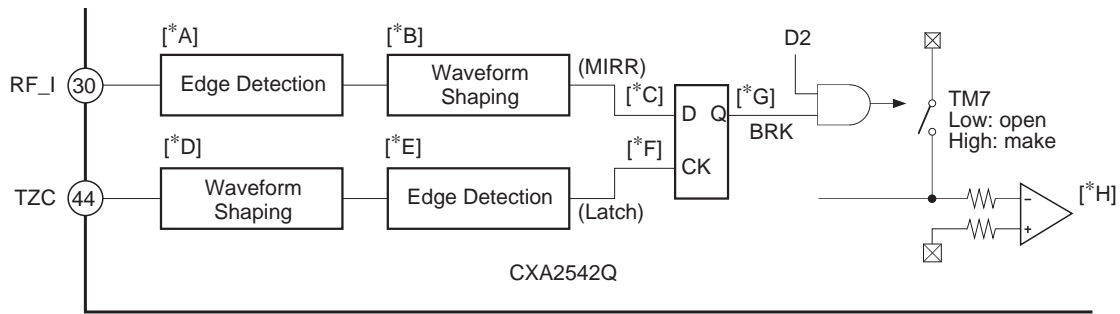


Fig. 6. TM7 movement during braking operation

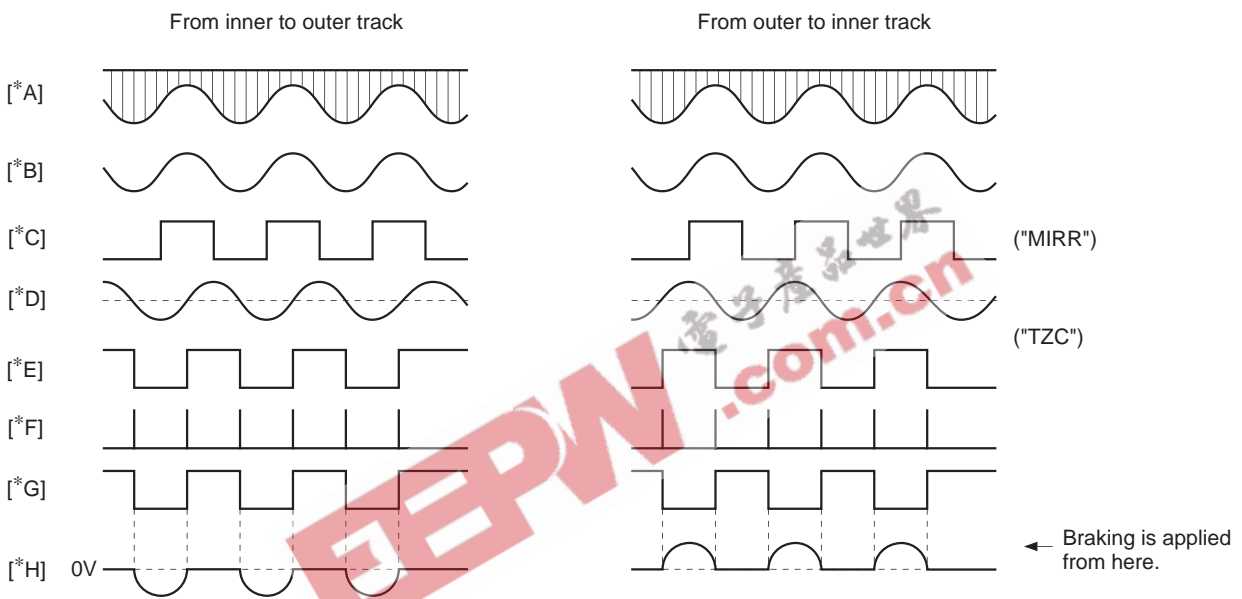


Fig. 7. Internal waveform

3. \$2X (TZC at SENS1 pin (Pin 23), MIRR at SENS2 pin (Pin 24))

These commands deal with turning the tracking servo and sled servo ON/OFF, and creating the jump pulse and fast forward pulse during access operations.

| D7 | D6 | D5 | D4 | D3 D2            |          | D1 D0         |                |
|----|----|----|----|------------------|----------|---------------|----------------|
| 0  | 0  | 1  | 0  | Tracking control |          | Sled control  |                |
|    |    |    |    | 00               | off      | 00            | off            |
|    |    |    |    | 01               | Servo ON | 01            | Servo ON       |
|    |    |    |    | 10               | F-JUMP   | 10            | F-FAST FORWARD |
|    |    |    |    | 11               | R-JUMP   | 11            | R-FAST FORWARD |
|    |    |    |    | ↓                |          | ↓             |                |
|    |    |    |    | TM1, TM3, TM4,   |          | TM2, TM5, TM6 |                |



#### 4. \$3XX

These commands mainly control the balance and gain control circuit switches used during automatic tracking adjustment and the bias circuit switch used during automatic focus bias adjustment.

In the initial resetting state, BAL1 to BAL4 switches and TOG1 to TOG4 switches are ON. Also, the IFB1 to 6 switches are ON.

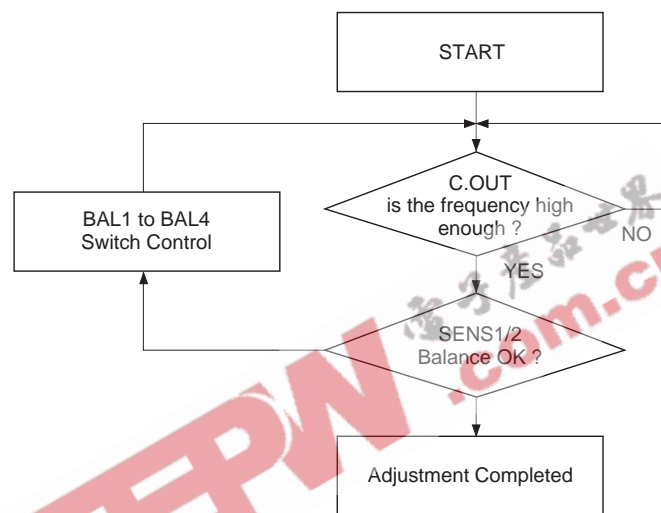
##### • Balance adjustment

The balance adjustment switches BAL1 to BAL4 can be controlled by setting  $D6 = 0$  and  $D7 = 0$ . The switches are set using D0 to D3.

At this time, SENS1 outputs BALH and SENS2 outputs BALL.

Data is set by specifying switch conditions D0 to D3 and sending a latch pulse with  $D6 = 0$  and  $D7 = 0$ .

Sending a latch pulse with  $D6, D7 \approx 0$  does not change the balance switch settings.



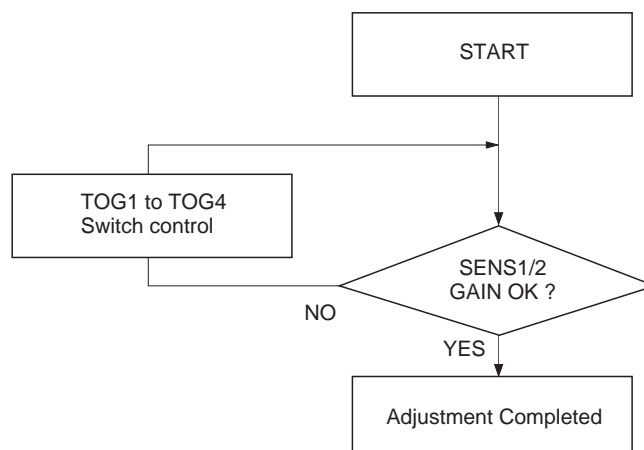
**Balance adjustment**

##### • Gain adjustment

The gain adjustment switches TOG1 to TOG4 can be controlled by setting  $D6 = 1$  and  $D7 = 0$ . These switches are set using D0 to D3.

At this time, SENS1 outputs TGH and SENS2 outputs TGL.

In a fashion similar to the method used with the balance adjustment, set the data by specifying switch conditions D0 to D3 and sending a latch pulse with  $D6 = 1$  and  $D7 = 0$ .



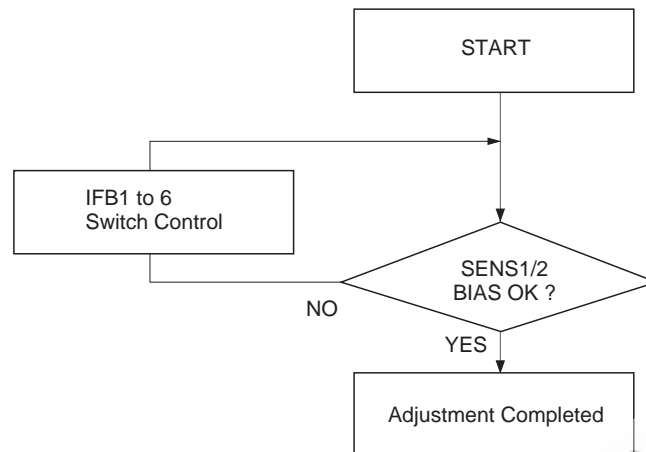
**Gain adjustment**

### • Focus bias adjustment

The focus bias adjustment switches IFB1 to 6 can be controlled by setting  $D6 = 0$  and  $D7 = 1$ . The switches are set using  $D0$  to  $D5$ .

At this time, SENS1 outputs FOH and SENS2 outputs FOL.

Data is set by specifying switch conditions  $D0$  to  $D5$  and sending a latch pulse with  $D6 = 0$  and  $D7 = 1$ .



Focus bias adjustment method

### • TGFL

The tracking gain can be switched by setting  $D5$  with  $D6 = 1$  and  $D7 = 0$ .

The tracking gain is GAIN UP with  $D5 = 1$  and NORMAL GAIN with  $D5 = 0$ .

The TEO signal level can be made higher by approximately 6dB for GAIN UP.

When the TEO signal level is low and TGH (SENS1 pin) does not go Low during tracking adjustment, the gain should be raised with the TGFL command for adjustment.

### • LPC

The laser power control circuit can be turned ON and OFF by setting  $D0$  with  $D6 = 1$  and  $D7 = 1$ .

The circuit is ON with  $D0 = 1$  and OFF with  $D0 = 0$ .

### • LPCL

The laser power control limit can be switched between  $\pm 17\%$  and  $\pm 50\%$  by setting  $D1$  with  $D6 = 1$  and  $D7 = 1$ .

The control limit is  $\pm 17\%$  with  $D1 = 0$  and  $\pm 50\%$  with  $D1 = 1$ .

### • LDON

The laser diode can be turned ON and OFF by setting  $D2$  with  $D6 = 1$  and  $D7 = 1$ .

The laser diode is ON with  $D2 = 1$  and OFF with  $D2 = 0$ .

- ATSC

The anti-shock function can be controlled by setting D3 with D6 = 1 and D7 = 1.

This function is disabled with D3 = 1 and enabled with D3 = 0.

At this time, SENS1 outputs ATSC.

Even if ATSC is disabled, ATSC is output to SENS1.

When an anti-shock signal is generated during the enable status, TG1 and TG2 switch to GAIN UP mode.

(In the Block Diagram, TG1 is set to the ○ side and TG2 is OFF. Even if TG1 and TG2 are NORMAL mode, they switch to GAIN UP mode in conjunction with ATSC.)

When the anti-shock function is not used, Pin 43 (ATSC) should be connected to VC.

- RDFCT2

DFCT2 can be reset by setting D4 with D6 = 1 and D7 = 1.

DFCT2 is reset with D4 = 1.

After a reset, High is held when DFCT1 rises.

During \$1X commands, DFCT2 is output from SENS2.

DFCT2 operates even if DFCT is disabled.

Whether or not DFCT rises at the proper timing for the microcomputer can also be confirmed.

- INT

The interruption (scratched disc) countermeasure circuit can be set to operating status by setting D5 with D6 = 1 and D7 = 1.

This circuit is enabled when D5 = 1 and disabled when D5 = 0.

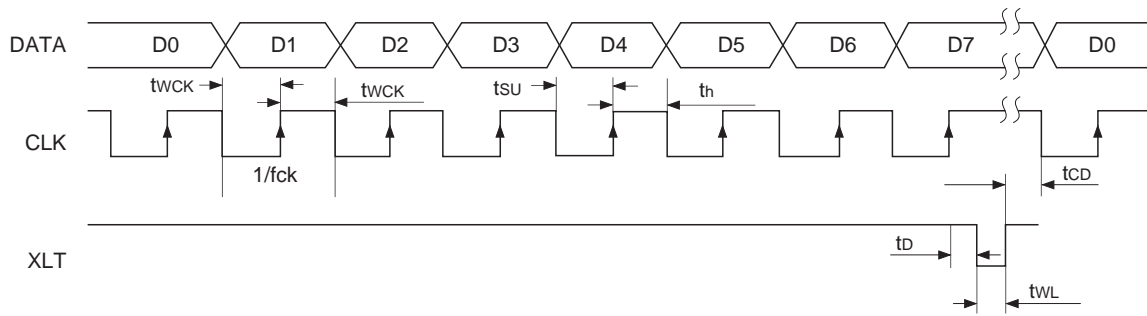
Even if DFCT1 does not rise, this circuit is effective for scratched discs which cause MIRR to rise.

When MIRR rises, the DFCT switch is routed through the low-pass filter.

The interruption countermeasure circuit is forcibly turned OFF regardless of the command when the tracking gain is increased. (including when the gain is increased by ATSC)

Even if DFCT is disabled, the interruption countermeasure circuit operates when INT is enabled.

CPU Serial Interface Timing Chart



( $V_{CC} = 3.0V$ )

| Item                     | Symbol    | Min.                           | Typ. | Max.                           | Unit |
|--------------------------|-----------|--------------------------------|------|--------------------------------|------|
| Clock frequency          | $f_{ck}$  |                                |      | 1                              | MHz  |
| Clock pulse width        | $f_{wck}$ | 500                            |      |                                | ns   |
| Setup time               | $t_{su}$  | 500                            |      |                                | ns   |
| Hold time                | $t_h$     | 500                            |      |                                | ns   |
| Delay time               | $t_d$     | 500                            |      |                                | ns   |
| Latch pulse width        | $t_{wL}$  | 1000                           |      |                                | ns   |
| Data transfer interval   | $t_{CD}$  | 1000                           |      |                                | ns   |
| Low level input voltage  | $V_{IL}$  | 0.0                            |      | $(V_{CC} - V_{EE}) \times 0.1$ | V    |
| High level input voltage | $V_{IH}$  | $(V_{CC} - V_{EE}) \times 0.9$ |      | $V_{CC}$                       | V    |

**System Control**

| Item               | DATA (Pin 20) 8-bit transfer |    |    |    |                                       |                                    |                                     |                                      |       |               | SENS1 | SENS2 |
|--------------------|------------------------------|----|----|----|---------------------------------------|------------------------------------|-------------------------------------|--------------------------------------|-------|---------------|-------|-------|
|                    | ADDRESS                      |    |    |    | DATA                                  |                                    |                                     |                                      |       |               |       |       |
|                    | D7                           | D6 | D5 | D4 | D3                                    | D2                                 | D1                                  | D0                                   |       |               |       |       |
| FOCUS CONTROL      | 0                            | 0  | 0  | 0  | FS4<br>Focus<br>1 = ON<br>0 = OFF     | —                                  | FS2<br>SRCH ON<br>1 = ON<br>0 = OFF | FS2<br>SRCH UP<br>1 = UP<br>0 = DOWN | FZC   | H<br>(HIGH-Z) |       |       |
| TRACKING CONTROL   | 0                            | 0  | 0  | 1  | TG1, TG2<br>1 = GAIN UP<br>0 = NORMAL | BRAKE<br>1 = ENABLE<br>0 = DISABLE | SLED<br>KICK + 2                    | SLED<br>KICK + 1                     | DFCT1 | DFCT2         |       |       |
| TRACKING SLED MODE | 0                            | 0  | 1  | 0  | TRACKING MODE *1                      | SLED MODE *2                       |                                     |                                      |       | TZC           | MIRR  |       |

\*1 TRACKING MODE

|          | D3 | D2 |
|----------|----|----|
| OFF      | 0  | 0  |
| ON       | 0  | 1  |
| FWD JUMP | 1  | 0  |
| REV JUMP | 1  | 1  |

\*2 SLED MODE

|          | D1 | D0 |
|----------|----|----|
| OFF      | 0  | 0  |
| ON       | 0  | 1  |
| FWD MOVE | 1  | 0  |
| REV MOVE | 1  | 1  |

| Item          | DATA (Pin 20) 12-bit transfer |     |    |    |    |    |                                   |                                   |                                   |                           |                              |                           | SENS1 | SENS2         |
|---------------|-------------------------------|-----|----|----|----|----|-----------------------------------|-----------------------------------|-----------------------------------|---------------------------|------------------------------|---------------------------|-------|---------------|
|               | ADDRESS                       |     |    |    |    |    | DATA                              |                                   |                                   |                           |                              |                           |       |               |
|               | D11                           | D10 | D9 | D8 | D7 | D6 | D5                                | D4                                | D3                                | D2                        | D1                           | D0                        |       |               |
| E-F BALANCE   | 0                             | 0   | 1  | 1  | 0  | 0  | —                                 | BAL4<br>1 = OFF<br>0 = ON         | BAL3<br>1 = OFF<br>0 = ON         | BAL2<br>1 = OFF<br>0 = ON | BAL1<br>1 = OFF<br>0 = ON    |                           | BALH  | BALL          |
| TRACKING GAIN | 0                             | 0   | 1  | 1  | 0  | 1  | —                                 | TGFL<br>1 = GAIN UP<br>0 = NORMAL | TOG4<br>1 = OFF<br>0 = ON         | TOG3<br>1 = OFF<br>0 = ON | TOG2<br>1 = OFF<br>0 = ON    | TOG1<br>1 = OFF<br>0 = ON | TGH   | TGL           |
| FOCUS BIAS    | 0                             | 0   | 1  | 1  | 1  | 0  | IFB5<br>1 = OFF<br>0 = ON         | IFB6<br>1 = OFF<br>0 = ON         | IFB4<br>1 = OFF<br>0 = ON         | IFB3<br>1 = OFF<br>0 = ON | IFB2<br>1 = OFF<br>0 = ON    | IFB1<br>1 = OFF<br>0 = ON | FOH   | FOL           |
| Others        | 0                             | 0   | 1  | 1  | 1  | 1  | RDFCT2<br>1 = RESET<br>0 = NORMAL | INT<br>1 = ENABLE<br>0 = DISABLE  | ATSC<br>1 = DISABLE<br>0 = ENABLE | LDON<br>1 = ON<br>0 = OFF | LPCL<br>1 = ±50%<br>0 = ±17% | LPC<br>1 = ON<br>0 = OFF  | ATSC  | H<br>(HIGH-Z) |

**Notes)**

- When ATSC is enabled, even if TG1 and TG2 are NORMAL mode, TG1 and TG2 switch to GAIN UP mode in conjunction with ATSC.
- INT is forcibly disabled regardless of the command when the tracking gain is increased. (including when the gain is increased by ATSC)

**When reset**

- SENS1 = FZC
- SENS2 = High (Hi-Z)
- RDFCT2 = 1 (Reset)
- IFB1 to IFB6 = 0 (switch ON)
- TOG1 to TOG4 = 0 (switch ON)
- BAL1 to BAL4 = 1 (switch ON)
- Other data is "0".

Serial Data Truth Table

| Serial Data             | HEX  | Functions |              |          |      |
|-------------------------|------|-----------|--------------|----------|------|
|                         |      | FS4       |              | FS2      | FS1  |
| <b>FOCUS CONTROL</b>    |      |           |              |          |      |
| 0000 0000               | \$00 | 0         |              | 0        | 0    |
| 0000 0001               | \$01 | 0         |              | 0        | 1    |
| 0000 0010               | \$02 | 0         |              | 1        | 0    |
| 0000 0011               | \$03 | 0         |              | 1        | 1    |
| 0000 0100               | \$04 | 0         |              | 0        | 0    |
| 0000 0101               | \$05 | 0         |              | 0        | 1    |
| 0000 0110               | \$06 | 0         |              | 1        | 0    |
| 0000 0111               | \$07 | 0         |              | 1        | 1    |
| 0000 1000               | \$08 | 1         |              | 0        | 0    |
| 0000 1001               | \$09 | 1         |              | 0        | 1    |
| 0000 1010               | \$0A | 1         |              | 1        | 0    |
| 0000 1011               | \$0B | 1         |              | 1        | 1    |
| 0000 1100               | \$0C | 1         |              | 0        | 0    |
| 0000 1101               | \$0D | 1         |              | 0        | 1    |
| 0000 1110               | \$0E | 1         |              | 1        | 0    |
| 0000 1111               | \$0F | 1         |              | 1        | 1    |
| <b>TRACKING CONTROL</b> |      |           |              |          |      |
|                         |      |           | BRAK         | SLD KICK |      |
|                         |      | TG1       | Fig. 6<br>D2 | KICK     | KICK |
|                         |      | TG2       |              | +2       | +1   |
| 0001 0000               | \$10 | 0         | 0            | 0        | 0    |
| 0001 0001               | \$11 | 0         | 0            | 0        | 1    |
| 0001 0010               | \$12 | 0         | 0            | 1        | 0    |
| 0001 0011               | \$13 | 0         | 0            | 1        | 1    |
| 0001 0100               | \$14 | 0         | 1            | 0        | 0    |
| 0001 0101               | \$15 | 0         | 1            | 0        | 1    |
| 0001 0110               | \$16 | 0         | 1            | 1        | 0    |
| 0001 0111               | \$17 | 0         | 1            | 1        | 1    |
| 0001 1000               | \$18 | 1         | 0            | 0        | 0    |
| 0001 1001               | \$19 | 1         | 0            | 0        | 1    |
| 0001 1010               | \$1A | 1         | 0            | 1        | 0    |
| 0001 1011               | \$1B | 1         | 0            | 1        | 1    |
| 0001 1100               | \$1C | 1         | 1            | 0        | 0    |
| 0001 1101               | \$1D | 1         | 1            | 0        | 1    |
| 0001 1110               | \$1E | 1         | 1            | 1        | 0    |
| 0001 1111               | \$1F | 1         | 1            | 1        | 1    |

Notes) • FS1  
1: OFF  
0: ON

• FS2  
1: ON  
0: OFF

• FS4  
In the Block Diagram:  
1:SW ○ side  
0:SW ● side

Notes) • TG1  
In the Block Diagram:  
1:SW ○ side  
0:SW ● side

• TG2  
1: OFF  
0: ON

• BRAKE  
When D2 in Fig. 6 is:  
1: 1  
0: 0

• Sled kick height

| D1 | D0 | Relative value |
|----|----|----------------|
| 0  | 0  | ±1             |
| 0  | 1  | ±2             |
| 1  | 0  | ±3             |
| 1  | 1  | ±4             |

| Serial Data        | HEX  | Function |     |     |     |     |     |
|--------------------|------|----------|-----|-----|-----|-----|-----|
|                    |      | TM6      | TM5 | TM4 | TM3 | TM2 | TM1 |
| TRACKING/SLED MODE |      |          |     |     |     |     |     |
| 0010 0000          | \$20 | 0        | 0   | 0   | 0   | 0   | 0   |
| 0010 0001          | \$21 | 0        | 0   | 0   | 0   | 1   | 0   |
| 0010 0010          | \$22 | 0        | 1   | 0   | 0   | 0   | 0   |
| 0010 0011          | \$23 | 1        | 0   | 0   | 0   | 0   | 0   |
| 0010 0100          | \$24 | 0        | 0   | 0   | 0   | 0   | 1   |
| 0010 0101          | \$25 | 0        | 0   | 0   | 0   | 1   | 1   |
| 0010 0110          | \$26 | 0        | 1   | 0   | 0   | 0   | 1   |
| 0010 0111          | \$27 | 1        | 0   | 0   | 0   | 0   | 1   |
| 0010 1000          | \$28 | 0        | 0   | 0   | 1   | 0   | 0   |
| 0010 1001          | \$29 | 0        | 0   | 0   | 1   | 1   | 0   |
| 0010 1010          | \$2A | 0        | 1   | 0   | 1   | 0   | 0   |
| 0010 1011          | \$2B | 1        | 0   | 0   | 1   | 0   | 0   |
| 0010 1100          | \$2C | 0        | 0   | 1   | 0   | 0   | 0   |
| 0010 1101          | \$2D | 0        | 0   | 1   | 0   | 1   | 0   |
| 0010 1110          | \$2E | 0        | 1   | 1   | 0   | 0   | 0   |
| 0010 1111          | \$2F | 1        | 0   | 1   | 0   | 0   | 0   |

Notes) • TM1/TM2

In the Block Diagram:

1:SW ○ side

0:SW ● side

• TM3/TM4/TM5/TM6

1: ON

0: OFF

EEPW.com.cn 电子产品世界





| Serial Data<br>\$3XX | HEX   | BAL SW |     |     |     | TOG SW | TGFL | IFB SW |     |     |     |     | INT | RDF<br>CT2 | ATSC | LDON | LPCL | LPC | DFCT |
|----------------------|-------|--------|-----|-----|-----|--------|------|--------|-----|-----|-----|-----|-----|------------|------|------|------|-----|------|
|                      |       | 4      | 3   | 2   | 1   |        |      | 4      | 3   | 2   | 1   | 6   |     |            |      |      |      |     |      |
| 0011 0011 0000       | \$330 | 1      | 1   | 1   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 0001       | \$331 | 1      | 1   | 1   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 0010       | \$332 | 1      | 1   | 0   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 0011       | \$333 | 1      | 1   | 0   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 0100       | \$334 | 1      | 0   | 1   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 0101       | \$335 | 1      | 0   | 1   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 0110       | \$336 | 1      | 0   | 0   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 0111       | \$337 | 1      | 0   | 0   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1000       | \$338 | 0      | 1   | 1   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1001       | \$339 | 0      | 1   | 1   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1010       | \$33A | 0      | 1   | 0   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1011       | \$33B | 0      | 1   | 0   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1100       | \$33C | 0      | 0   | 1   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1101       | \$33D | 0      | 0   | 1   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1110       | \$33E | 0      | 0   | 0   | 1   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0011 1111       | \$33F | 0      | 0   | 0   | 0   | ---    | ---  | ---    | --- | --- | --- | --- | --- | ---        | ---  | ---  | ---  | --- | D    |
| 0011 0100 0000       | \$340 | ---    | --- | --- | --- | 1      | 1    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 0001       | \$341 | ---    | --- | --- | --- | 1      | 1    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 0010       | \$342 | ---    | --- | --- | --- | 1      | 1    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 0011       | \$343 | ---    | --- | --- | --- | 1      | 1    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 0100       | \$344 | ---    | --- | --- | --- | 1      | 0    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 0101       | \$345 | ---    | --- | --- | --- | 1      | 0    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 0110       | \$346 | ---    | --- | --- | --- | 1      | 0    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 0111       | \$347 | ---    | --- | --- | --- | 1      | 0    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1000       | \$348 | ---    | --- | --- | --- | 0      | 1    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1001       | \$349 | ---    | --- | --- | --- | 0      | 1    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1010       | \$34A | ---    | --- | --- | --- | 0      | 1    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1011       | \$34B | ---    | --- | --- | --- | 0      | 1    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1100       | \$34C | ---    | --- | --- | --- | 0      | 0    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1101       | \$34D | ---    | --- | --- | --- | 0      | 0    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1110       | \$34E | ---    | --- | --- | --- | 0      | 0    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0100 1111       | \$34F | ---    | --- | --- | --- | 0      | 0    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0000       | \$350 | ---    | --- | --- | --- | 1      | 1    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0001       | \$351 | ---    | --- | --- | --- | 1      | 1    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0010       | \$352 | ---    | --- | --- | --- | 1      | 1    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0011       | \$353 | ---    | --- | --- | --- | 1      | 1    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0100       | \$354 | ---    | --- | --- | --- | 1      | 0    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0101       | \$355 | ---    | --- | --- | --- | 1      | 0    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0110       | \$356 | ---    | --- | --- | --- | 1      | 0    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 0111       | \$357 | ---    | --- | --- | --- | 1      | 0    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1000       | \$358 | ---    | --- | --- | --- | 0      | 1    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1001       | \$359 | ---    | --- | --- | --- | 0      | 1    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1010       | \$35A | ---    | --- | --- | --- | 0      | 1    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1011       | \$35B | ---    | --- | --- | --- | 0      | 1    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1100       | \$35C | ---    | --- | --- | --- | 0      | 0    | 1      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1101       | \$35D | ---    | --- | --- | --- | 0      | 0    | 1      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1110       | \$35E | ---    | --- | --- | --- | 0      | 0    | 0      | 1   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |
| 0011 0101 1111       | \$35F | ---    | --- | --- | --- | 0      | 0    | 0      | 0   | 0   | --- | --- | --- | ---        | ---  | ---  | ---  | --- | ---  |

| Serial Data<br>\$3XX | HEX   | BAL SW  | TOG SW  | TGFL | IFB SW      | INT | RDF<br>CT2 | ATSC | LDON | LPCL | LPC | DFCT |
|----------------------|-------|---------|---------|------|-------------|-----|------------|------|------|------|-----|------|
|                      |       | 4 3 2 1 | 4 3 2 1 |      | 6 5 4 3 2 1 |     |            |      |      |      |     |      |
| 0011 0110 0000       | \$360 | ----    | 1 1 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 0001       | \$361 | ----    | 1 1 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 0010       | \$362 | ----    | 1 1 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 0011       | \$363 | ----    | 1 1 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 0100       | \$364 | ----    | 1 0 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 0101       | \$365 | ----    | 1 0 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 0110       | \$366 | ----    | 1 0 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 0111       | \$367 | ----    | 1 0 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1000       | \$368 | ----    | 0 1 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1001       | \$369 | ----    | 0 1 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1010       | \$36A | ----    | 0 1 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1011       | \$36B | ----    | 0 1 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1100       | \$36C | ----    | 0 0 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1101       | \$36D | ----    | 0 0 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1110       | \$36E | ----    | 0 0 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0110 1111       | \$36F | ----    | 0 0 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0000       | \$370 | ----    | 1 1 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0001       | \$371 | ----    | 1 1 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0010       | \$372 | ----    | 1 1 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0011       | \$373 | ----    | 1 1 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0100       | \$374 | ----    | 1 0 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0101       | \$375 | ----    | 1 0 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0110       | \$376 | ----    | 1 0 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 0111       | \$377 | ----    | 1 0 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1000       | \$378 | ----    | 0 1 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1001       | \$379 | ----    | 0 1 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1010       | \$37A | ----    | 0 1 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1011       | \$37B | ----    | 0 1 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1100       | \$37C | ----    | 0 0 1 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1101       | \$37D | ----    | 0 0 1 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1110       | \$37E | ----    | 0 0 0 1 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 0111 1111       | \$37F | ----    | 0 0 0 0 | 1    | -----       | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0000       | \$380 | ----    | -----   | —    | 1 1 1 1 1 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0001       | \$381 | ----    | -----   | —    | 1 1 1 1 1 0 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0010       | \$382 | ----    | -----   | —    | 1 1 1 1 0 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0011       | \$383 | ----    | -----   | —    | 1 1 1 1 0 0 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0100       | \$384 | ----    | -----   | —    | 1 1 1 0 1 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0101       | \$385 | ----    | -----   | —    | 1 1 1 0 1 0 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0110       | \$386 | ----    | -----   | —    | 1 1 1 0 0 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 0111       | \$387 | ----    | -----   | —    | 1 1 1 0 0 0 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1000       | \$388 | ----    | -----   | —    | 1 1 0 1 1 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1001       | \$389 | ----    | -----   | —    | 1 1 0 1 1 0 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1010       | \$38A | ----    | -----   | —    | 1 1 0 1 0 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1011       | \$38B | ----    | -----   | —    | 1 1 0 1 0 0 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1100       | \$38C | ----    | -----   | —    | 1 1 0 0 1 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1101       | \$38D | ----    | -----   | —    | 1 1 0 0 1 0 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1110       | \$38E | ----    | -----   | —    | 1 1 0 0 0 1 | —   | —          | —    | —    | —    | —   | —    |
| 0011 1000 1111       | \$38F | ----    | -----   | —    | 1 1 0 0 0 0 | —   | —          | —    | —    | —    | —   | —    |



| Serial Data<br>\$3XX | HEX   | BAL SW |     |     | TOG SW |     |     | TGFL | IFB SW |     |     |     |   | INT | RDF<br>CT2 | ATSC | LDON | LPCL | LPC | DFCT |
|----------------------|-------|--------|-----|-----|--------|-----|-----|------|--------|-----|-----|-----|---|-----|------------|------|------|------|-----|------|
|                      |       | 4      | 3   | 2   | 1      | 4   | 3   |      | 2      | 1   | 6   | 5   | 4 |     |            |      |      |      |     |      |
| 0011 1100 0000       | \$3C0 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 0    | 0    | 0    | --- |      |
| 0011 1100 0001       | \$3C1 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 0    | 0    | 1    | --- |      |
| 0011 1100 0010       | \$3C2 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 0    | 1    | 0    | --- |      |
| 0011 1100 0011       | \$3C3 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 0    | 1    | 1    | --- |      |
| 0011 1100 0100       | \$3C4 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 1    | 0    | 0    | --- |      |
| 0011 1100 0101       | \$3C5 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 1    | 0    | 1    | --- |      |
| 0011 1100 0110       | \$3C6 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 1    | 1    | 0    | --- |      |
| 0011 1100 0111       | \$3C7 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | E          | 1    | 1    | 1    | --- |      |
| 0011 1100 1000       | \$3C8 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 0    | 0    | 0    | --- |      |
| 0011 1100 1001       | \$3C9 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 0    | 0    | 1    | --- |      |
| 0011 1100 1010       | \$3CA | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 0    | 1    | 0    | --- |      |
| 0011 1100 1011       | \$3CB | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 0    | 1    | 1    | --- |      |
| 0011 1100 1100       | \$3CC | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 1    | 0    | 0    | --- |      |
| 0011 1100 1101       | \$3CD | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 1    | 0    | 1    | --- |      |
| 0011 1100 1110       | \$3CE | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 1    | 1    | 0    | --- |      |
| 0011 1100 1111       | \$3CF | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 0   | D          | 1    | 1    | 1    | --- |      |
| 0011 1101 0000       | \$3D0 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 0    | 0    | 0    | --- |      |
| 0011 1101 0001       | \$3D1 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 0    | 0    | 1    | --- |      |
| 0011 1101 0010       | \$3D2 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 0    | 1    | 0    | --- |      |
| 0011 1101 0011       | \$3D3 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 0    | 1    | 1    | --- |      |
| 0011 1101 0100       | \$3D4 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 1    | 0    | 0    | --- |      |
| 0011 1101 0101       | \$3D5 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 1    | 0    | 1    | --- |      |
| 0011 1101 0110       | \$3D6 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 1    | 1    | 0    | --- |      |
| 0011 1101 0111       | \$3D7 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | E          | 1    | 1    | 1    | --- |      |
| 0011 1101 1000       | \$3D8 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 0    | 0    | 0    | --- |      |
| 0011 1101 1001       | \$3D9 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 0    | 0    | 1    | --- |      |
| 0011 1101 1010       | \$3DA | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 0    | 1    | 0    | --- |      |
| 0011 1101 1011       | \$3DB | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 0    | 1    | 1    | --- |      |
| 0011 1101 1100       | \$3DC | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 1    | 0    | 0    | --- |      |
| 0011 1101 1101       | \$3DD | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 1    | 0    | 1    | --- |      |
| 0011 1101 1110       | \$3DE | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 1    | 1    | 0    | --- |      |
| 0011 1101 1111       | \$3DF | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 0 | 1   | D          | 1    | 1    | 1    | --- |      |
| 0011 1110 0000       | \$3E0 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 0    | 0    | 0    | --- |      |
| 0011 1110 0001       | \$3E1 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 0    | 0    | 1    | --- |      |
| 0011 1110 0010       | \$3E2 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 0    | 1    | 0    | --- |      |
| 0011 1110 0011       | \$3E3 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 0    | 1    | 1    | --- |      |
| 0011 1110 0100       | \$3E4 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 1    | 0    | 0    | --- |      |
| 0011 1110 0101       | \$3E5 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 1    | 0    | 1    | --- |      |
| 0011 1110 0110       | \$3E6 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 1    | 1    | 0    | --- |      |
| 0011 1110 0111       | \$3E7 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | E          | 1    | 1    | 1    | --- |      |
| 0011 1110 1000       | \$3E8 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 0    | 0    | 0    | --- |      |
| 0011 1110 1001       | \$3E9 | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 0    | 0    | 1    | --- |      |
| 0011 1110 1010       | \$3EA | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 0    | 1    | 0    | --- |      |
| 0011 1110 1011       | \$3EB | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 0    | 1    | 1    | --- |      |
| 0011 1110 1100       | \$3EC | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 1    | 0    | 0    | --- |      |
| 0011 1110 1101       | \$3ED | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 1    | 0    | 1    | --- |      |
| 0011 1110 1110       | \$3EE | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 1    | 1    | 0    | --- |      |
| 0011 1110 1111       | \$3EF | ---    | --- | --- | ---    | --- | --- | ---  | ---    | --- | --- | --- | 1 | 0   | D          | 1    | 1    | 1    | --- |      |

| Serial Data<br>\$3XX | HEX   | BAL SW |   |   |   | TOG SW | TGFL | IFB SW |   |   |   |   | INT | RDF<br>CT2 | ATSC | LDON | LPCL | LPC | DFCT |
|----------------------|-------|--------|---|---|---|--------|------|--------|---|---|---|---|-----|------------|------|------|------|-----|------|
|                      |       | 4      | 3 | 2 | 1 |        |      | 4      | 3 | 2 | 1 | 6 |     |            |      |      |      |     |      |
| 0011 1111 0000       | \$3F0 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 0    | 0    | 0   | —    |
| 0011 1111 0001       | \$3F1 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 0    | 0    | 1   | —    |
| 0011 1111 0010       | \$3F2 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 0    | 1    | 0   | —    |
| 0011 1111 0011       | \$3F3 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 0    | 1    | 1   | —    |
| 0011 1111 0100       | \$3F4 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 1    | 0    | 0   | —    |
| 0011 1111 0101       | \$3F5 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 1    | 0    | 1   | —    |
| 0011 1111 0110       | \$3F6 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 1    | 1    | 0   | —    |
| 0011 1111 0111       | \$3F7 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | E    | 1    | 1    | 1   | —    |
| 0011 1111 1000       | \$3F8 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 0    | 0    | 0   | —    |
| 0011 1111 1001       | \$3F9 | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 0    | 0    | 1   | —    |
| 0011 1111 1010       | \$3FA | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 0    | 1    | 0   | —    |
| 0011 1111 1011       | \$3FB | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 0    | 1    | 1   | —    |
| 0011 1111 1100       | \$3FC | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 1    | 0    | 0   | —    |
| 0011 1111 1101       | \$3FD | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 1    | 0    | 1   | —    |
| 0011 1111 1110       | \$3FE | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 1    | 1    | 0   | —    |
| 0011 1111 1111       | \$3FF | —      | — | — | — | —      | —    | —      | — | — | — | — | 1   | 1          | D    | 1    | 1    | 1   | —    |

**Notes)** • 0 means OFF and 1 means ON for TOG SW and BAL SW. These are not equal to the setting values of each bit for serial data.

• "—" in the Truth Table indicates that the status does not change.

• TGFL

In the Block Diagram:

1:SW ○ side

0:SW ● side

• ATSC E: enable/D: disable

• DFCT E: enable/D: disable



**Initial State (resetting state)**

| Item               | ADDRESS |    |    |    | DATA |    |    |    | HEX  |
|--------------------|---------|----|----|----|------|----|----|----|------|
|                    | D7      | D6 | D5 | D4 | D3   | D2 | D1 | D0 |      |
| FOCUS CONTROL      | 0       | 0  | 0  | 0  | 0    | 0  | 0  | 0  | \$00 |
| TRACKING CONTROL   | 0       | 0  | 0  | 1  | 0    | 0  | 0  | 0  | \$10 |
| TRACKING SLED MODE | 0       | 0  | 1  | 0  | 0    | 0  | 0  | 0  | \$20 |

| Item          | ADDRESS |     |    |    |    |    | DATA |    |    |    |    |    | HEX   |
|---------------|---------|-----|----|----|----|----|------|----|----|----|----|----|-------|
|               | D11     | D10 | D9 | D8 | D7 | D6 | D5   | D4 | D3 | D2 | D1 | D0 |       |
| E-F BALANCE   | 0       | 0   | 1  | 1  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | \$300 |
| TRACKING GAIN | 0       | 0   | 1  | 1  | 0  | 1  | 0    | 0  | 0  | 0  | 0  | 0  | \$340 |
| FOCUS BIAS    | 0       | 0   | 1  | 1  | 1  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | \$380 |
| Others        | 0       | 0   | 1  | 1  | 1  | 1  | 0    | 1  | 0  | 0  | 0  | 0  | \$3D0 |

The above data means the following operation modes.

- FOCUS CONTROL : FOCUS OFF, FOCUS SEARCH OFF, FOCUS SEACH DOWN
- TRACKING CONTROL : TG1-TG2 NORMAL, BRAKE DISABLE, SLED KICK relative height value  $\pm 1$
- TRACKING SLED MODE : TRACKING OFF, SLED OFF
- E-F BALANCE : BAL1 to BAL4 = 0 (switch ON). DFCT ENABLE
- TRACKING GAIN : TOG1 to TOG4 = 0 (switch ON), TGFL NORMAL
- FOCUS BIAS : IFB1 to IFB6 = 0 (switch ON)
- Others : INT DISABLE, DFCT2 RESET, ATSC ENABLE, LDON OFF, LPCL  $\pm 17\%$ , LPC OFF

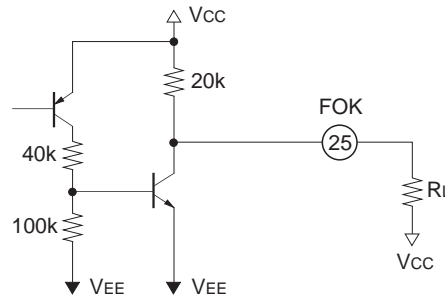
**Notes on Operation**

1. Focus OK circuit

- 1) Refer to the "Description of Operation" for the time constant setting of the focus OK amplifier LPF and the mirror amplifier HPF.
- 2) The equivalent circuit for the output pin (FOK) is shown in the diagram below.

The FOK and comparator output are as follows:

- Output voltage High :  $V_{FOKH} \approx \text{near } V_{CC}$
- Output voltage Low :  $V_{FOKL} \approx V_{sat} (\text{NPN}) + V_{EE}$



2. Sled amplifier

The sled amplifier may oscillate when used by the buffer amplifier. Use with a gain of approximately 20dB.

3. Focus/Tracking internal phase compensation and reference design material

|     | Item         | SD      | Measurement pin | Conditions                                   | Typ. | Unit |
|-----|--------------|---------|-----------------|--|------|------|
| FCS | 1.2kHz gain  | 08      | 6               | $C_{FLB} = 0.1\mu F$<br>$C_{FGD} = 0.1\mu F$ | 21.5 | dB   |
|     | 1.2kHz phase | 08      |                 |  | 63   | deg  |
| TRK | 1.2kHz gain  | 25      | 13              | $C_{TGU} = 0.1\mu F$                         | 13   | dB   |
|     | 1.2kHz phase | 25      |                 |  | -125 | deg  |
|     | 2.7kHz gain  | 25 → 13 |                 |  | 26.5 | dB   |
|     | 2.7kHz phase | 25 → 13 |                 |  | -130 | deg  |

4. Laser Poser Control

The RF level is stabilized by attaching an offset to the APC  $V_L$  and controlling the laser power in sync with the RF level fluctuations.

The laser life is shortened by increasing the laser power when the less light is reflected from the disc.

It is recommended that the typical laser power value is set lower to maintain the laser life.

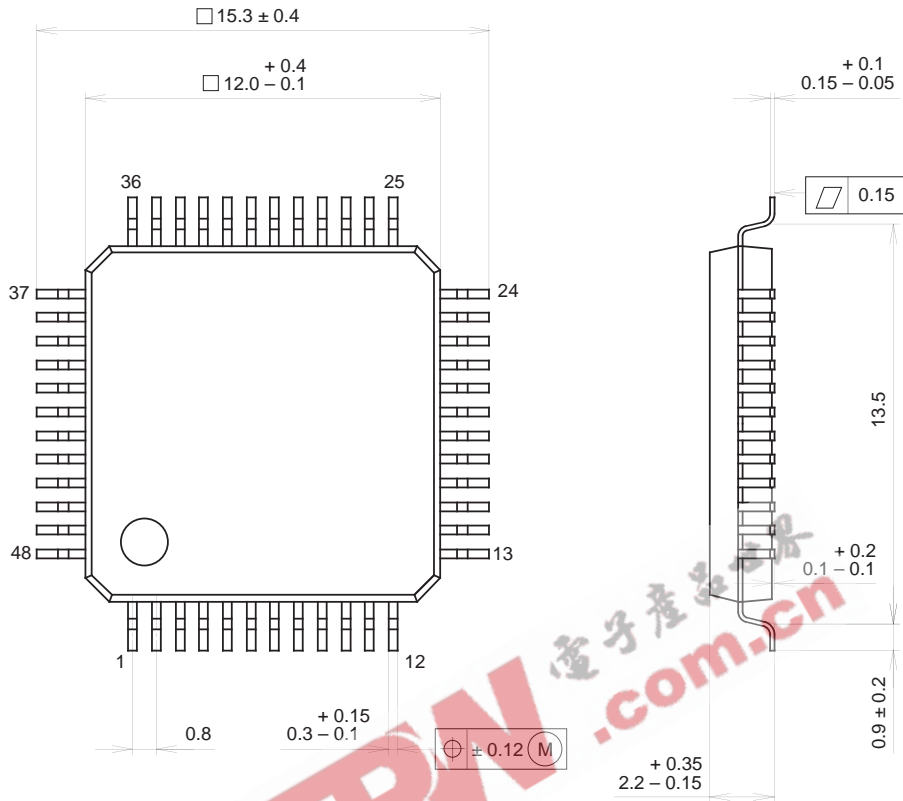
Take care of the laser maximum ratings when using the laser power control circuit.



Package Outline

Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

|            |                  |
|------------|------------------|
| SONY CODE  | QFP-48P-L04      |
| EIAJ CODE  | *QFP048-P-1212-B |
| JEDEC CODE | —                |

|                  |                            |
|------------------|----------------------------|
| PACKAGE MATERIAL | EPOXY RESIN                |
| LEAD TREATMENT   | SOLDER / PALLADIUM PLATING |
| LEAD MATERIAL    | COPPER / 42 ALLOY          |
| PACKAGE WEIGHT   | 0.7g                       |