SONY

CXA3268AR

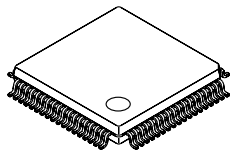
Driver/Timing Generator for Color LCD Panels

Description

The CXA3268AR is an IC designed to drive the color LCD panels ACX300, ACX301, ACX302 and ACX703.

This IC greatly reduces the number of peripheral circuits and parts by incorporating a RGB driver and timing generator for video signals onto a single chip. This chip has a built-in serial interface circuit and electronic attenuators which allow various settings to be performed by microcomputer control, etc.

72 pin LQFP (Plastic)



Features

- Color LCD panel ACX300, ACX301, ACX302 and ACX703 driver
- Supports NTSC and PAL systems
- Supports 16:9 wide display (letter box and pulse elimination display)
- Supports Y/color difference and RGB inputs
- Supports OSD input (digital input)
- Power saving function
- Serial interface circuit
- Electronic attenuators (D/A converter)
- Trap and LPF (f0, fc variable)
- COMMON and PSIG output circuits
- Sharpness function
- 2-point γ correction circuit
- R, G, B signal delay time adjustment circuit
- D/A output pin (0 to 3V, 8 level output)
- Output polarity inversion circuit
- Supports AC drive for LCD panel during no signal

Applications

Compact LCD monitors, etc.

Absolute Maximum Ratings (Ta = 25°C)

- Supply voltage
  - $V_{CC}1$: 6 V
  - $V_{CC}2$: 15 V
  - $V_{CC}3$: 15 V
  - V_{DD}: 5.5 V
- Analog input pin voltage
  - VINA (Pins 57, 58 and 59): GND – 0.3 to $V_{CC}1$ + 0.3 V
  - VINA (Pins 3, 69): $V_{CC}1$ V
  - VINA (Pin 30): 1.5 to $V_{CC}2$ – 4 V
  - VINA (Pin 71): 0.9 Vp-p
  - VINA (Pins 70, 72): 0.8 Vp-p
- Digital input pin voltage
  - VIND (other than Pins 5, 10, 14, 15 and 16): V_{SS} – 0.3 to V_{DD} + 0.3 V
  - VIND (Pins 5, 10): V_{SS} – 0.3 to +5.5 V
- Common input pin voltage
  - VINAD (Pins 14, 15 and 16): GND, V_{SS} – 0.3 to +5.5 V
- Operating temperature
  - Topr: –15 to +75 °C
- Storage temperature
  - Tstg: –55 to +150 °C
- Allowable power dissipation
  - P_D (Ta ≤ 25°C): 737 mW

Operating conditions

- Supply voltage

$V_{CC}1$ – GND1	2.7 to 3.6	V
$V_{CC}2$ – GND2	11.0 to 14.0	V
$V_{CC}3$ – GND3	11.0 to 14.0	V
V_{DD} – Vss	2.7 to 3.6	V

- Input voltage

SIG.C voltage

VSIG.C	5.0 to 6.5	V

RGB input signal voltage (Pins 70, 71 and 72)*1

VRGB	0 to 0.7 (0.5 typ.)	Vp-p

Y input signal voltage (Pin 71)*2

VY	0 to 0.5 (0.35 typ.)	Vp-p

R-Y input voltage (Pin 72)*2

VR-Y	0 to 0.49 (0.245 typ.)	Vp-p

B-Y input voltage (Pin 70)*2

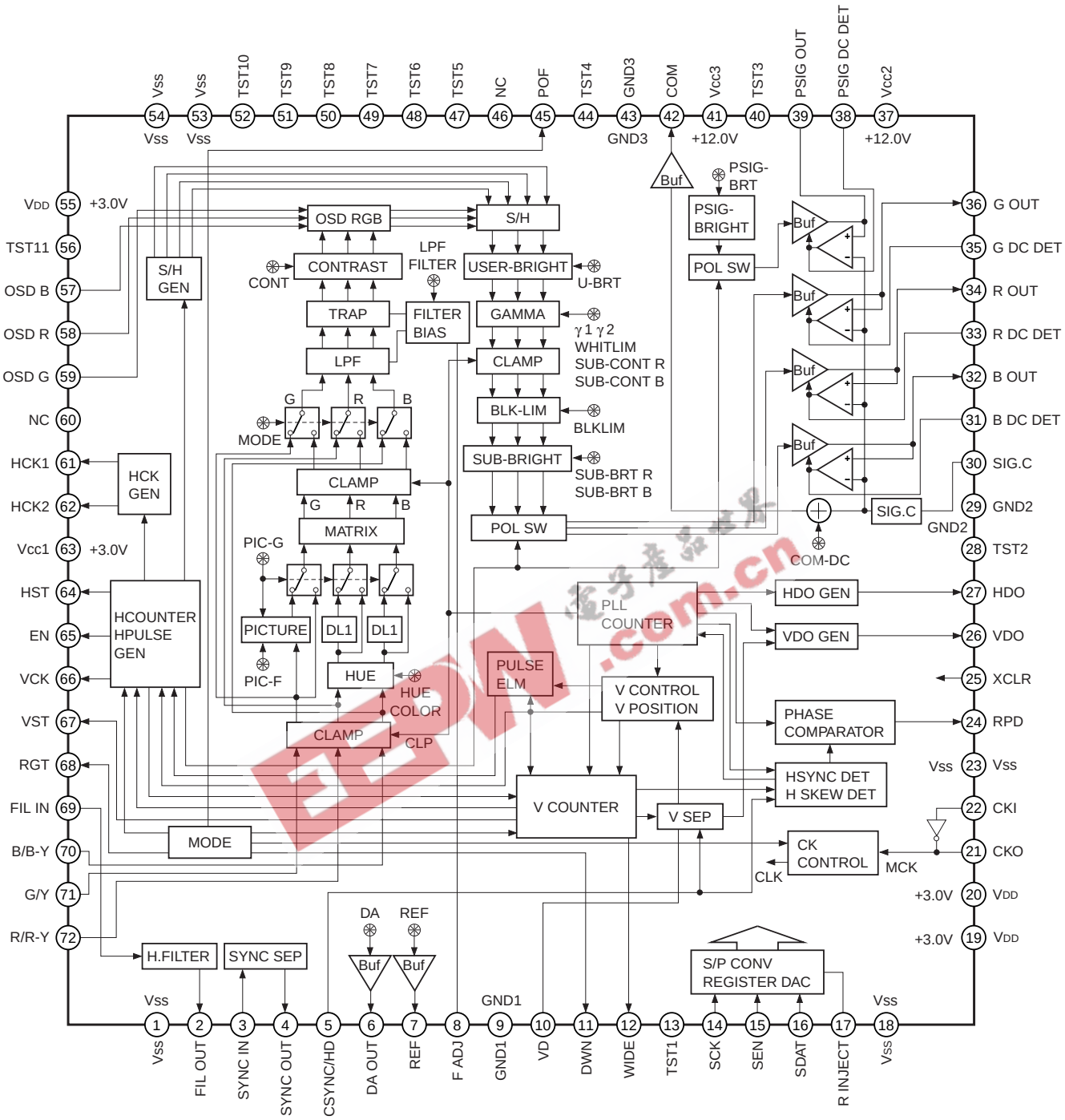
VB-Y	0 to 0.622 (0.311 typ.)	Vp-p

*1 During RGB input

*2 During Y/color difference input

E99529B98-PS

Block Diagram



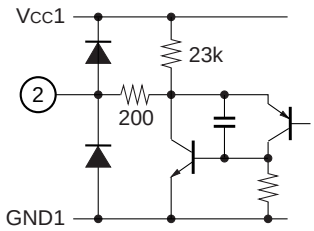
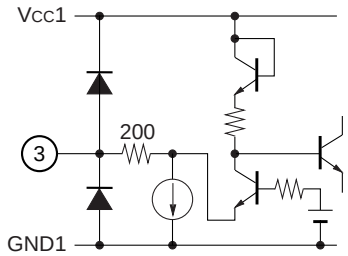
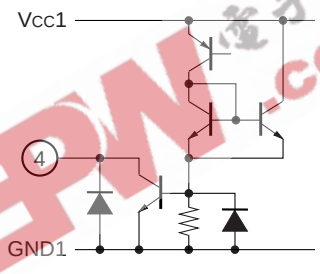
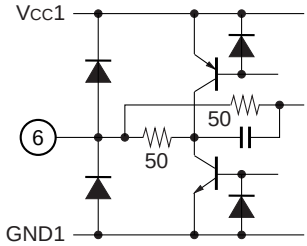
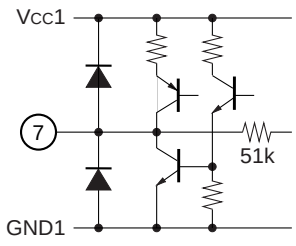
Pin Description

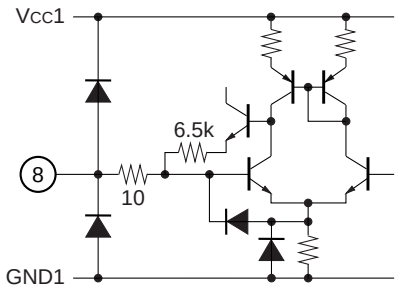
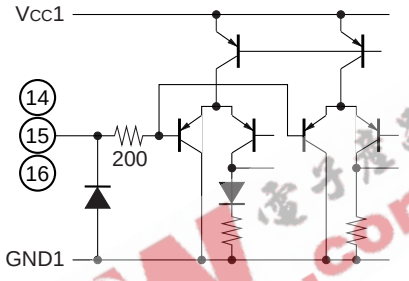
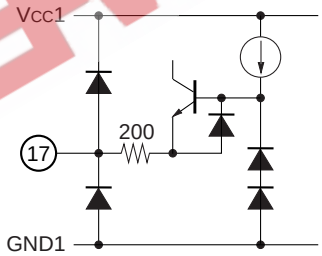
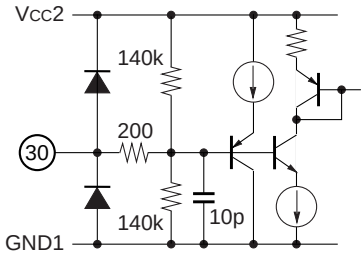
Pin No.	Symbol	I/O	Description	Input pin for open status
1	V_{SS}	—	Digital 3.0V GND	
2	FIL OUT	O	H filter output (for using internal sync separation)	
3	SYNC IN	I	Sync separation circuit input (for using internal sync separation)	
4	SYNC OUT	O	Sync separation circuit output (for using internal sync separation)	
5	CSYNC/HD	I	CSYNC/horizontal sync signal input	
6	DA OUT	O	DAC output	
7	REF	O	Level shifter circuit REF voltage output for LCD panel	
8	F ADJ	O	Trap f0 adjusting resistor connection	
9	GND1	—	Analog 3.0V GND	
10	VD	I	Vertical sync signal input	L
11	DWN	O	Up/down inversion switching signal output	
12	WIDE	O	16:9 wide display switching pulse output	
13	TST1	—	Test (Leave this pin open.)	
14	SCK	I	Serial clock input	
15	SEN	I	Serial load input	
16	SDAT	I	Serial data input	
17	R INJECT	O	Serial block current controlling resistor connection	
18	V_{SS}	—	Digital 3.0V GND	
19	V_{DD}	—	Digital 3.0V power supply	
20	V_{DD}	—	Digital 3.0V power supply	
21	CKO	O	Oscillation cell output	
22	CKI	I	Oscillation cell input	
23	V_{SS}	—	Digital 3.0V GND	
24	RPD	O	Phase comparator output	
25	XCLR	I	Power-on reset capacitor connection (timing generator block)	H
26	VDO	O	VDO pulse output	
27	HDO	O	HDO pulse output	
28	TST2	—	Test (Connect to GND.)	
29	GND2	—	Analog 12.0V GND	
30	SIG.C	I	R, G, B and PSIG output DC voltage adjustment	
31	B DC DET	O	B signal DC voltage feedback circuit capacitor connection	
32	B OUT	O	B signal output	
33	R DC DET	O	R signal DC voltage feedback circuit capacitor connection	
34	R OUT	O	R signal output	
35	G DC DET	O	G signal DC voltage feedback circuit capacitor connection	
36	G OUT	O	G signal output	
37	$V_{CC}2$	—	Analog 12.0V power supply	

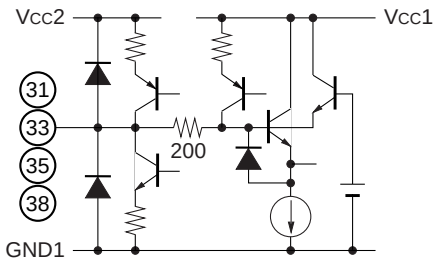
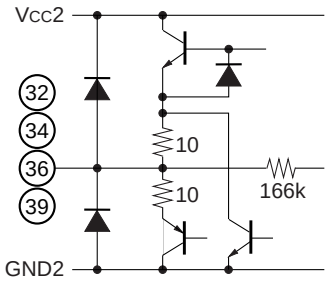
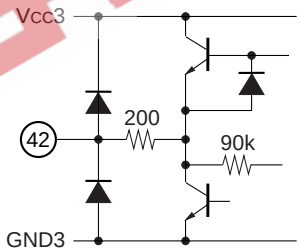
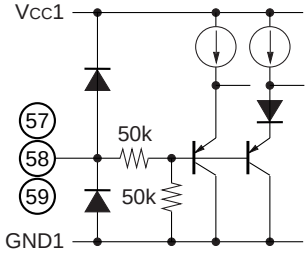
Pin No.	Symbol	I/O	Description	Input pin for open status
38	PSIG DC DET	O	PSIG signal DC voltage feedback circuit capacitor connection	
39	PSIG OUT	O	PSIG output	
40	TST3	—	Test (Leave this pin open.)	
41	Vcc3	—	Analog 12.0V COM (CS) power supply	
42	COM	O	Common pad voltage for LCD panel output (CS)	
43	GND3	—	Analog 12.0V COM (CS) GND	
44	TST4	—	Test (Leave this pin open.)	
45	POF	O	LCD panel power supply on/off (Leave this pin open when not using this function.)	
46	NC			
47	TST5	—	Test (Connect to GND.)	
48	TST6	—	Test (Connect to GND.)	
49	TST7	—	Test (Leave this pin open.)	
50	TST8	—	Test (Leave this pin open.)	
51	TST9	—	Test (Leave this pin open.)	
52	TST10	—	Test (Leave this pin open.)	
53	Vss	—	Digital 3.0V GND	
54	Vss	—	Digital 3.0V GND	
55	VDD	—	Digital 3.0V power supply	
56	TST11	—	Test (Connect to GND.)	
57	OSD B	I	OSD B input	
58	OSD R	I	OSD R input	
59	OSD G	I	OSD G input	
60	NC			
61	HCK1	O	H clock pulse 1 output	
62	HCK2	O	H clock pulse 2 output	
63	Vcc1	—	Analog 3.0V power supply	
64	HST	O	H start pulse output	
65	EN	O	EN pulse output	
66	VCK	O	V clock pulse output	
67	VST	O	V start pulse output	
68	RGT	O	Right/left inversion switching signal output	
69	FIL IN	I	H filter input (for using internal sync separation)	
70	B/B-Y	I	B/B-Y signal input	
71	G/Y	I	G/Y signal input	
72	R/R-Y	I	R/R-Y signal input	

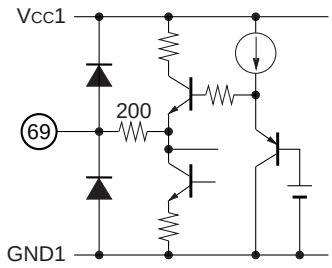
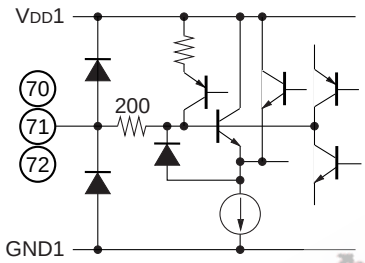
* DWN: DOWN SCAN and UP SCAN, RGT: RIGHT SCAN and LEFT SCAN
H: pull-up processing, L: pull-down processing

Analog Block Pin Description

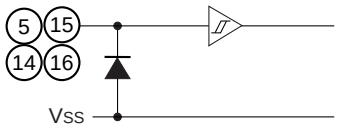
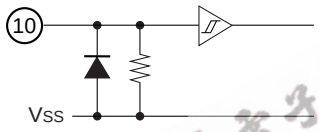
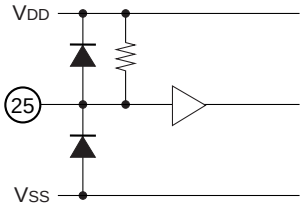
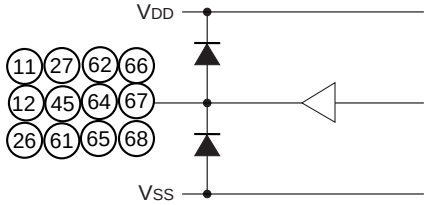
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
2	FIL OUT	2.15V		Amplifies and outputs the sync portion of the video signal input to FIL IN (Pin 69).
3	SYNC IN	1.1V		Sync separation circuit input. Inputs the FIL OUT (Pin 2) output signal via a capacitor.
4	SYNC OUT	—		Sync separation output. Positive polarity output in open collector format.
6	DA OUT	—		DA output. Outputs the serial data converted to DC voltage. The current driving capacity is ±1.0mA (max.).
7	REF	—		REF output. Outputs the serial data converted to DC voltage. The current driving capacity (sink) is ±1.5mA (max.).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
8	F ADJ	1.1V		Connect a resistor between this pin and GND1 to control the internal LPF and trap frequencies. Connect a 33kΩ resistor (tolerance ±2%, temperature characteristics ±200ppm or less). This pin is easily affected by external noise, so make the connection between the pin and external resistor, and between the GND side of the external resistor and the GND1 pin as close as possible.
9	GND1	—		Analog 3.0V GND.
14 15 16	SCK SEN SDAT	—		Serial clock, serial load and serial data inputs for serial communication.
17	R INJECT	0.7V		Connect a resistor for setting the injector current of the IIL logic circuit. Connect a 15kΩ resistor between this pin and GND1. Use a resistor with a deviation of ±2% and temperature characteristics of ±200ppm or less.
29	GND2	—		Analog 12.0V GND. (for the RGB and PSIG output circuits)
30	SIG.C	Preset Vcc2/2 Variable range: 5.0 to 6.5V		R, G, B and PSIG output DC voltage setting. Connect a 0.01µF capacitor between this pin and GND1. When using a SIG.C of other than Vcc2/2, input the SIG.C voltage from an external source.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31 33 35 38	B DC DET R DC DET G DC DET PSIG DC DET	1.8V		Smoothing capacitor connection for the feedback circuit of R, G, B and PSIG output DC level control. Connect a low-leakage capacitor.
32 34 36 39	B OUT R OUT G OUT PSIG OUT	Vcc2/2 (SIG.C = preset)		R, G, B and PSIG signal outputs. The DC level is controlled to match the SIG.C pin voltage. Low output in power saving mode. Vcc2/2V output when preset.
37	Vcc2	12.0V		Analog 12.0V power supply. (for the RGB and PSIG output circuits)
41	Vcc3	12.0V		Analog 12.0V power supply. (for COM (CS) output)
42	COM	—		COMMON voltage output. The output voltage is controlled by serial communication.
43	GND3	—		Analog 12.0V GND. (for COM (CS) output)
57 58 59	OSD B OSD R OSD G	Vth1 = Vcc1 × 1/3 Vth2 = Vcc1 × 2/3		OSD pulse inputs. When one of these input pins exceeds the Vth1 level, all of the outputs go to black limiter level; when an input pin exceeds the Vth2 level, only the corresponding output goes to white limiter level.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
63	$V_{CC}1$	—		Analog 3.0V power supply.
69	FIL IN	1.2V		H filter input. Input the video signal via a capacitor.
70 71 72	B/B-Y G/Y R/R-Y	G/Y 1.8V R/R-Y, B/B-Y, RGB: 1.8V Y/color difference: 2.0V		In Y/color difference input mode, input the Y signal to Pin 71, the B-Y signal to Pin 70, and the R-Y signal to Pin 72. In RGB input mode, input the B signal to Pin 70, the G signal to Pin 71 and the R signal to Pin 72. Pedestal clamp these pins with external coupling capacitors.

Digital Block Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 18 23 53 54	V_{SS}	—		Digital 3.0V GND.
19 20 55	V_{DD}	—		Digital 3.0V power supply.
5 14 15 16	CSYNC/HD SCK SEN SDAT	—		Composite sync/horizontal sync signal input, and serial clock, serial load and serial data inputs for serial communication.
10	VD	—		Vertical sync signal input.
21	CKO	—		Oscillation circuit output.
22	CKI	—		Oscillation circuit input.
24	RPD	—		Phase comparator output.
25	XCLR	—		Digital block system reset.
11 12 26 27 45 61 62 64 65 66 67 68	DWN WIDE VDO HDO POF HCK1 HCK2 HST EN VCK VST RGT	—		Digital block outputs.

Test Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
13 40 44 49 50 51 52	TST1 TST3 TST4 TST7 TST8 TST9 TST10	—		Test. Leave these pins open.
28 47 48 56	TST2 TST5 TST6 TST11	—		Test. Connect to GND.

Setting Conditions for Measuring Electrical Characteristics

Use the Electrical Characteristics Measurement Circuit on page 22 when measuring electrical characteristics. For measurement, the digital block must be initialized and power saving must be canceled by performing Settings 1 and 2 below. In addition, the serial data must be set to the initial settings shown in the table below.

Setting 1. Horizontal AFC adjustment

Input a signal and adjust the VCO using V22 so that WL and WH of the TP24 output waveform are the same.

Setting 2. Canceling power saving mode

The power-on default is power saving mode, so clear (set all "0") serial data PS0, PS1, PS2, PS4 and SYNC GEN.

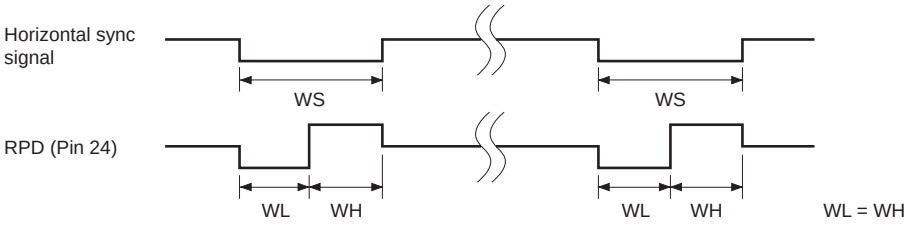


Fig. 1. Horizontal AFC adjustment

Serial data initial settings

MSB ADDRESS LSB								MSB DATA LSB							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	USER-BRIGHT (01000110/LSB)							
0	0	0	0	0	0	0	1	SUB-BRIGHT R (10001010/LSB)							
0	0	0	0	0	0	1	0	SUB-BRIGHT B (10001010/LSB)							
0	0	0	0	0	0	1	1	CONTRAST (00111111/LSB)							
0	0	0	0	0	1	0	0	SUB-CONTRAST R (10011111/LSB)							
0	0	0	0	0	1	0	1	SUB-CONTRAST B (10011111/LSB)							
0	0	0	0	0	1	1	0	γ-2 (11111111/LSB)							
0	0	0	0	0	1	1	1	γ-1 (11111111/LSB)							
0	0	0	0	1	0	0	0	0	PSIG-BRIGHT (1011111/LSB)						
0	0	0	0	1	0	0	1	COM-DC (10000000/LSB)							
0	0	0	0	1	0	1	0	COLOR (00000000/LSB)							
0	0	0	0	1	0	1	1	HUE (10000000/LSB)							
0	0	0	0	1	1	0	0	0	WHITE-LIMITER (00/LSB)	BLACK-LIMITER (11111/LSB)					
0	0	0	0	1	1	0	1	FILTER (00/LSB)		REF (000/LSB)			LPF (000/LSB)		
0	0	0	0	1	1	1	0	PICTURE-GAIN (00000/LSB)					0	PICTURE-F0 (00/LSB)	
0	0	0	0	1	1	1	1	0	0	0	0	MODE (1)	DA (000/LSB)		
0	0	0	1	0	0	0	0	0	0	SYNC GEN (0)	PS 4 (0)	0	PS 2 (0)	PS 1 (0)	PS 0 (0)
0	0	1	0	0	0	0	0	SLSYP (1)	SLEXVD (0)	SLDWN (0)	SLRGT (0)	SLSH2 (1)	SLSH1 (1)	SLWD (0)	SLPL (0)
0	0	1	0	0	0	0	1	0	SLFL (0)	SLFR (0)	SL4096 (0)	SLCLP2 (0)	SLCLP1 (0)	SLVDP (0)	SLHDP (0)
0	0	1	0	0	0	1	0	0	0	SLTST4 (0)	SLTST3 (0)	SLSH0 (1)	SLTST2 (0)	SLTST1 (0)	SLTST0 (0)
0	0	1	0	0	0	1	1	0	0	0	H-POSITION (10000)				
0	0	1	0	0	1	0	0	0	0	0	HD-POSITION (00000)				

Note) If there is the possibility that data may be set at other than the above-noted addresses, set these data to "0".

Electrical Characteristics — DC Characteristics

Analog Block Unless otherwise specified, Ta = 25°C, $V_{CC}1 = V_{DD} = 3.0V$, $V_{CC}2/V_{CC}3 = 12.0V$, SW4 = off for the current consumption measurement, see page 11 for the DAC.

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption 1 (Y/color difference input)	I1	Measure the inflow current to Pin 63.		27.0	37.0	mA
Current consumption 2 (Y/color difference input)	I2	Measure the inflow current to Pin 37.		3.8	5.0	mA
Current consumption 3 (Y/color difference input)	I3	Measure the inflow current to Pin 41.		0.90	1.3	mA
Current consumption 1 (RGB input)	IRGB1	Measure the inflow current to Pin 63.		23.0	30.0	mA
Current consumption 2 (RGB input)	IRGB2	Measure the inflow current to Pin 37.		3.8	5.0	mA
Current consumption 3 (RGB input)	IRGB3	Measure the inflow current to Pin 41.		0.90	1.3	mA
Current consumption 1 (PS0 = 1)	IPS01	Measure the inflow current to Pin 63.		7.5	10.0	mA
Current consumption 2 (PS0 = 1)	IPS02	Measure the inflow current to Pin 37.		0.18	0.35	mA
Current consumption 3 (PS0 = 1)	IPS03	Measure the inflow current to Pin 41.			1.00	µA
Current consumption 1 (PS2 = 1)	IPS21	Measure the inflow current to Pin 63.		26.5	36.5	mA
Current consumption 1 (PS4 = 1)	IPS41	Measure the inflow current to Pin 63.		26.5	36.5	mA
Current consumption 1 (SYNC GEN = 1)	ISG1	Measure the inflow current to Pin 63.		7.0	9.5	mA
Current consumption 2 (SYNC GEN = 1)	ISG2	Measure the inflow current to Pin 37.		0.18	0.35	mA
Current consumption 3 (SYNC GEN = 1)	ISG3	Measure the inflow current to Pin 41.			1.00	µA
FIL OUT pin voltage	V2	During no input	1.8	2.1	2.4	V
SYNC IN pin voltage	V3	During no input	1.8	1.1	1.4	V
SYNC OUT pin voltage	V4	During no input		0.2	0.4	V
F ADJ pin voltage	V8		0.8	1.1	1.4	V
R INJECT pin voltage	V17		0.4	0.7	1.0	V
SIG.C pin voltage	V30		5.8	6.0	6.2	V
B DC DET pin voltage	V31		1.5	1.8	2.1	V
R DC DET pin voltage	V33		1.5	1.8	2.1	V
G DC DET pin voltage	V35		1.5	1.8	2.1	V
PSIG DC DET pin voltage	V38		1.5	1.8	2.1	V
FIL IN pin voltage	V69		0.9	1.2	1.5	V
B/B-Y pin voltage 1	V70	During Y/color difference input	1.7	2.0	2.3	V
B/B-Y pin voltage 2	V70	During RGB input	1.5	1.8	2.1	V
G/Y pin voltage	V71		1.5	1.8	2.1	V
R/R-Y pin voltage 1	V70	During Y/color difference input	1.7	2.0	2.3	V
R/R-Y pin voltage 2	V70	During RGB input	1.5	1.8	2.1	V
REF pin voltage (power saving mode)	V7	I7 = 1.5mA			0.3	V
OSD input resistance	V57 V58 V59		80	100	120	kΩ

Digital Block (including some analog block) (Ta = –15 to +75°C, V_{DD} = V_{CC}1 = 3.7 to 3.6V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Applicable pins
High level input voltage	V_{IH}		$V_{DD} \times 0.7$			V	*1
Low level input voltage	V_{IL}				$V_{DD} \times 0.3$	V	
High level threshold voltage	$V_{T+}1$	Schmitt buffer			2.6	V	*2
Low level threshold voltage	$V_{T-}1$		0.6			V	
Hysteresis voltage	$V_{T+}1 - V_{T-}1$		0.4			V	
High level threshold voltage	$V_{T+}2$				2.6	V	*3
Low level threshold voltage	$V_{T-}2$		0.6			V	
Hysteresis voltage	$V_{T+}2 - V_{T-}2$		0.2			V	
High level input current	$\lvert I_{IH1} \rvert$	$V_I = V_{DD}$			1.0	µA	*4
Low level input current	$\lvert I_{IL1} \rvert$	V_I = 0V			1.0	µA	
High level input current	$\lvert I_{IH2} \rvert$	$V_I = V_{DD}$			3.0	µA	*5
Low level input current	$\lvert I_{IL2} \rvert$	V_I = 0V	10	40	100	µA	
High level input current	$\lvert I_{IH3} \rvert$	$V_I = V_{DD}$	10	40	100	µA	*6
Low level input current	$\lvert I_{IL3} \rvert$	V_I = 0V			3.0	µA	
High level input current	$\lvert I_{IH4} \rvert$	$V_I = V_{DD}$			1.0	µA	*7
Low level input current	$\lvert I_{IL4} \rvert$	V_I = 0V			2.0	µA	
Low level output voltage	V_{OL1}	I_{OL} = 1mA			0.3	V	*8
High level output voltage	V_{OH1}	I_{OH} = –0.25mA	2.6			V	
Low level output voltage	V_{OL2}	I_{OL} = 2mA			0.3	V	*9
High level output voltage	V_{OH2}	I_{OH} = –0.5mA	2.6			V	
Low level output voltage	V_{OL3}	I_{OL} = 4mA			0.3	V	*10
High level output voltage	V_{OH3}	I_{OH} = –1mA	2.6			V	
Low level output voltage	V_{OL4}	I_{OL} = 1.5mA			0.4	V	*11
High level output voltage	V_{OH4}	I_{OH} = –1.25mA	V_{DD} – 0.5			V	
Output leak current	$\lvert I_{OZ} \rvert$	High impedance status			1.0	µA	*12

*1 XCLR (Pin 25), CKI (Pin 22)
*2 CSYNC/HD (Pin 5), VD (Pin 10)
*3 SCK (Pin 14), SEN (Pin 15), SDAT (Pin 16)
*4 CSYNC/HD (Pin 5), CKI (Pin 22)
*5 XCLR (Pin 25)
*6 VD (Pin 10)
*7 SCK (Pin 14), SEN (Pin 15), SDAT (Pin 16)
*8 DWN (Pin 11), WIDE (Pin 12), VCK (Pin 66), VST (Pin 67), RGT (Pin 68)
*9 RPD (Pin 24), VDO (Pin 26), HDO (Pin 27), POF (Pin 45), HST (Pin 64), EN (Pin 65)
*10 HCK1 (Pin 61), HCK2 (Pin 62)
*11 CKO (Pin 21). However, when measuring the output pin (CKO), the input level of the input pin (CKI) should be 0V or V_{DD}.
*12 RPD (Pin 24)

Electrical Characteristics

AC Characteristics

Unless otherwise specified, Settings 1 and 2, the serial data initial settings, and the following setting conditions are required.
Ta = 25°C, $V_{CC}1$ = 3.0V, $V_{CC}2$ = $V_{CC}3$ = 12V, GND1/2/3 = 0V, V_{SS} = 0V, SW2 = ON, SW4 = ON, SW32/34/36 = OFF, no video input, SG1 input to TP5
Note: Serial data values in the table are HEX notation.

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
Maximum gain between input and output Y/color difference	G_{MAX}	CONT FFh	Input SG2 (50mVp-p) to TP71 and measure the output amplitude at TP36.	29	32	34	dB
Maximum gain between input and output RGB	G_{RGBMAX}	CONT FFh MODE 00h	Input SG2 (50mVp-p) to TP71 and measure the output amplitude at TP36.	26	29	31	dB
Amount of contrast attenuation	Gcon	CONT 00h	Assume the output amplitude at TP36 when SG2 (0.5Vp-p) is input to TP71 as GMIN. Δgcon = G_{MAX} – G_{MIN}	25	30		dB
Inverted and non-inverted gain difference	ΔG_{INV}	CONT 2Fh	Assume the inverted output amplitude at TP36 when SG2 (0.35Vp-p) is input to TP71 as Vinv, and the non-inverted output amplitude as Vninv. Δginv = 20 log (Vninv/Vinv)			±0.3	dB
Gain difference between R, G and B	$\Delta G_{RGB}1$	CONT 2Fh	Input SG2 (0.35Vp-p) to TP71 (TP70, TP72), measure the non-inverted output amplitude at TP32, TP34 and TP36, and obtain the maximum and minimum difference between these values.			0.6	dB
	$\Delta G_{RGB}2$	MODE 00h CONT 2Fh				0.6	
Sub-contrast variable amount	$\Delta G_{SC}1$	SUB-CONT 00h	Set CONT = 26h, input SG2 (0.35Vp-p) to TP71, and assume the non-inverted output amplitude at TP32 and TP34 when SUB-CONT R/B = 9Ah, 00h and FFh as V1, V2 and V3, respectively. ΔGsc1 = 20 log (V3/V1) ΔGsc2 = 20 log (V2/V1)		–5.5	–4.5	dB
	$\Delta G_{SC}2$	SUB-CONT FFh		2.0	2.7		
Sub-bright variable amount	$\Delta V_{SB}1$	SUB-BRT R, B 00h	Set U-BRT = 1Ah and measure the non-inverted level at TP32 and TP34 relative to the non-inverted black level at TP36 when SUB-BRT R/B = FFh and 00h.		–1.5	–1.0	V
	$\Delta V_{SB}2$	SUB-BRT R, B FFh		0.8	1.2		
Black limiter variable amount	$V_{BL}1$	BLK-LIM 00h	Set U-BRT = FFh, measure the inverted and non-inverted black limit level at TP36 when BLK-LIM = 00h and 1Fh, and assume the difference from the output DC voltage as $V_{BL}1$ and $V_{BL}2$, respectively.	±1.6	±2.1	±2.7	V
	$V_{BL}2$	BLK-LIM 1Fh		±4.7	±5.1	±5.4	

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
White limiter variable amount	$V_{WL}1$	WHITE-LIM 00h	Set CONT = FFh, input SG2 (0.35Vp-p) to TP71, measure the inverted and non-inverted white limit level when WHITE-LIM = 00h and 03h, and assume the difference from the output DC voltage as $V_{WL}1$ and $V_{WL}2$, respectively.	±1.2	±0.6	±0	V
	$V_{WL}2$	WHITE-LIM 03h		±0.6	±1.2	±1.8	
Black level difference between R, G and B	ΔV_B		Measure the non-inverted black level at TP32, TP34 and TP36, and obtain the maximum and minimum difference between these values.			300	mV
RGB and PSIG output DC voltage	Vc		Measure the output DC level (average voltage) at TP32, TP34, TP36 and TP39.	5.8	6.0	6.2	V
DC voltage difference between RGB and PSIG	ΔVc		Measure the output average voltage difference at TP32, TP34 and TP39 relative to the output average voltage at TP36.			±200	mV
PSIG-BRT variable amount	VPB1	PSIG-BRT 01h	Measure the inverted and non-inverted black level when PSIG-BRT = 01h and 7Fh and assume the difference from the average DC voltage Vc as VPB1 and VPB2, respectively.			±0.7	V
	VPB2	PSIG-BRT 7Fh		±4.2			
USER-BRT variable amount	ΔUB1	U-BRT 00h	Measure the inverted and non-inverted black level at TP36 when U-BRT = 00h and 7Ah and assume the difference from the average voltage as ΔUB1 and ΔUB2, respectively.		±0.8	±1.5	V
	ΔUB2	U-BRT 7Ah		±4.5	±4.9		
Level difference between PSIG-BLK and BLK-LIM	ΔVBB	SLWD 1	Set BLK-LIM = 00h and measure the difference between the inverted and non-inverted black level at TP36 and TP39.			350	mV
Hue variable amount	θ1	HUE 00h	Set U-BRT = 23h, CONT = 80h, COLOR = 40h, and assume the amplitude at TP32 when SG4 (56mVp-p) is input to TP72 as V1. Similarly, assume the amplitude at TP34 when SG4 (100mVp-p) is input to TP70 as V2. θ = tan – 1 (V1/V2). Assume the θ when HUE = 00h, 80h and FFh as θa, θb and θc, respectively. θ1 = θa – θb, θ2 = θc – θb	–20	–25		deg
	θ2	HUE FFh		20	25		deg
Picture variable amount	GP1	PIC-G 01h	Set CONT = 2Fh, input SG3 to TP71, and measure the TP36 amplitude at f0 relative to the TP36 amplitude at 100kHz when PIC-G = 01h and 1Fh. f0 at PIC-f0 = 00h, 01h, 02h and 03h is 2MHz, 2.2MHz, 2.6MHz and 2.9MHz, respectively.	–1.5	0	1.5	dB
	GP2	PIC-G 1Fh		10	12		
Color variable amount	GC1	COLOR 00h	Input SG4 (50mVp-p) to TP70 and TP72, and assume the output amplitude at TP32 and TP34 when COLOR = 00h, 80h and FFh as V1, V2 and V3, respectively. GC1 = 20 log (V1/V2) GC2 = 20 log (V3/V2)		–30	–20	dB
	GC2	COLOR FFh		5.0	6.0		

Item	Symbol	Serial data setting (HEX)	Measurement conditions		Min.	Typ.	Max.	Unit
Matrix amplitude ratio	B-Y/R-Y	CONT 63h COLOR 6Fh	Assume the TP34 output when SG4 (0.1Vp-p) is input to TP72 as RR, the TP32 amplitude when SG4 (0.1Vp-p) is input to TP70 as BB, the TP34 amplitude when SG5 (0.1Vp-p) is input to TP72 as RG, and the TP32 amplitude when SG5 (0.1Vp-p) is input to TP70 as BG. B-Y/R-Y = RR/BB, G-Y/R-Y = RG/RR, G-Y/B-Y = BG/BB		0.85	1.00	1.15	
	G-Y/R-Y				0.41	0.51	0.61	
	G-Y/B-Y				0.15	0.19	0.23	
LPF characteristics	fc1	LPF 01h MODE 00h	Input SG3 to TP71 and measure the frequency which results in –3dB relative to the TP36 amplitude at 100kHz when LPF = 01h and 07h.			2.0	2.5	MHz
	fc2	LPF 07h MODE 00h			5.0	6.4		
Trap characteristics	fo1	MODE 00h	Set U-BRT = 30h, CONT = DFh, input SG7 (13.5MHz) to TP70, TP71 and TP72, and measure the amount by which the output is attenuated when FILTER = 01h relative to FILTER = 00h. Similarly, input SG7 (14.5MHz) to TP70, TP71 and TP72, and measure the amount by which the output is attenuated when FILTER = 02h relative to FILTER = 00h.		–20	–27		dB
	fo2	MODE 00h			–20	–27		
Frequency response	f RGB	MODE 00h	Set SW32, SW34 and SW36 = ON, input SG3 to TP70, TP71 and TP72, and measure the frequency which results in –3dB relative to the TP32, TP34 and TP36 amplitude at 100kHz.		5.5			MHz
REF adjustment range	VREF1	REF 00h	Measure the REF pin output voltage when REF = 00h and 07h.	Output current 1.5mA, sink only	1.20	1.35	1.50	V
	VREF2	REF 07h			1.90	2.05	2.20	
DA adjustment range	VDA1	DA 00h	Measure the DA output voltage when DA = 00h and 07h.	Output current 1.0mA			0.3	V
	VDA2	DA 07h		Output current –1.0mA	2.7			
Internal DAC differential non-linearity error	SDL		Measure under the measurement conditions for each adjustment range.		–1.5		1.5	LSB
Internal DAC non-linearity error	SL		Measure under the measurement conditions for each adjustment range.		–2.0		2.0	LSB
Gamma characteristics	$\Delta\gamma1$	CONT 41h	Input SG2 (0.35mVp-p) to TP71 and measure the amplitude at TP32, TP34 and TP36. Assume the output amplitude when GAMMA1 = FFh as V1, when GAMMA1 = 3Fh as V2, and when GAMMA1 = GAMMA2 = 3Fh as V3. $\Delta\gamma1$ = 20 log (V1/V2) $\Delta\gamma2$ = 20 log (V3/V2)		12	14	16	dB
	$\Delta\gamma2$				12	14	16	
H FIL gain	Ghfil		Input SG6 to TP69 and measure the output amplitude at TP2.		15.0	17.0		dB

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
COMMON control range	COM_{DC}		Measure the COM output DC voltage when COM-DC = 00h and FFh, and measure the difference from the COM output DC voltage when COM-DC = 80h.	±1.0	±1.3		V
SYNC IN sensitivity current	I SYNC		Gradually increase the SYNC IN outflow current and measure the current at which SYNC OUT switches to high.	20	31		µA
SYNC OUT on voltage	VOsync		Measure the SYNC OUT pin voltage during SYNC IN no input.		0.2	0.4	V
OSD threshold value	Vth1 OSD		Input SG4 to TP57, TP58 and TP59, gradually raise the high level from 0V, and assume the high level voltage at which the output level goes to BLK-LIM level as Vth1OSD, and the high level voltage at which the output level goes to WHITE-LIM level as Vth2OSD.	0.8	1.0	1.2	V
	Vth2 OSD			1.8	2.0	2.2	
Propagation delay time between input and output Y/color difference 1	tLH1		Set SW32, SW34 and SW36 = ON, input SG4 (0.35Vp-p) to TP71, and measure the propagation delay time of the non-inverted output rise and fall at TP32, TP34 and TP36 from TP71.	70	120	170	ns
	tHL1			80	130	180	
Propagation delay time between input and output RGB input	tLH2	MODE 00h	Set SW32, SW34 and SW36 = ON, input SG4 (0.35Vp-p) to TP70, TP71 and TP72, and measure the propagation delay time of the non-inverted output rise and fall at TP32, TP34 and TP36 from TP70, TP71 and TP72.	70	110	160	ns
	tHL2			60	110	160	
Propagation delay time between input and output Y/color difference 2	tLH3	PIC-G 01h	Set SW32, SW34 and SW36 = ON, input SG4 (0.35Vp-p) to TP71, and measure the propagation delay time of the non-inverted output rise and fall at TP32, TP34 and TP36 from TP71.	270	330	390	ns
	tHL3			270	330	390	
Propagation delay time between OSD input and output	tLH4		Set SW32, SW34 and SW36 = ON, input SG4 (3Vp-p) to TP57, TP58 and TP59, and measure the propagation delay time of the non-inverted rise and fall at TP70, TP71 and TP72 from TP57, TP58 and TP59.	90	130	170	ns
	tHL4			170	210	250	
Propagation delay time between H FIL and FIL OUT	tLH7		Input SG6 to TP69 and measure the propagation delay time of the rise and fall at TP2 from TP69.	500	700	900	ns
	tHL7			100	300	500	
Propagation delay time between SYNC IN and SYNC OUT	tLH8		Set SW2 = OFF, input SG8 to TP3, and measure the propagation delay time of the rise and fall at TP4 from TP3.	140	200	260	ns
	tHL8			40	100	160	

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
Data setup time	ts0		SEN setup time, activated by the rising edge of SCK. (See Fig. 4.)	150			ns
	ts1		SDAT setup time, activated by the rising edge of SCK. (See Fig. 4.)	150			
Data hold time	th0		SEN hold time, activated by the rising edge of SCK. (See Fig. 4.)	150			ns
	th1		SDAT hold time, activated by the rising edge of SCK. (See Fig. 4.)	150			
Minimum pulse width	tw1L		SCK pulse width. (See Fig. 4.)	210			ns
	tw1H		SCK pulse width. (See Fig. 4.)	210			ns
	tw2		SEN pulse width. (See Fig. 4.)	1			µs
Output transition time	tTLH		Measure the transition time of each output. 30pF load: RPD, VDO, HDO and POF output pins 40pF load: EN and HST output pins 120pF load: HCK1 and HCK2 output pins (See Fig. 2.)			30	ns
	tTHL					30	
	tTLH		Measure the transition time of each output. 40pF load: DWN, WIDE, VCK, VST and RGT output pins (See Fig. 2.)			50	ns
	tTHL					50	
Cross-point time difference	ΔT		Measure HCK1/HCK2. 120pF load (See Fig. 3.)			10	ns
HCK duty	DTYHC		Measure the HCK1/HCK2 duty. 120pF load	47	50	53	%

Electrical Characteristic Measurement Method Diagrams

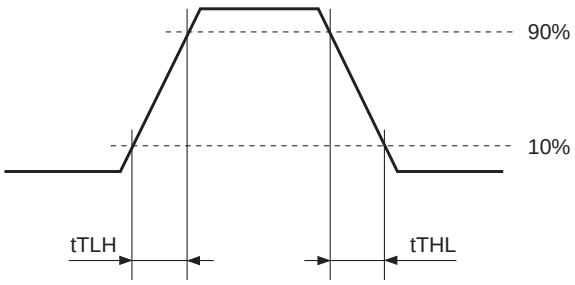


Fig. 2. Output transition time measurement conditions

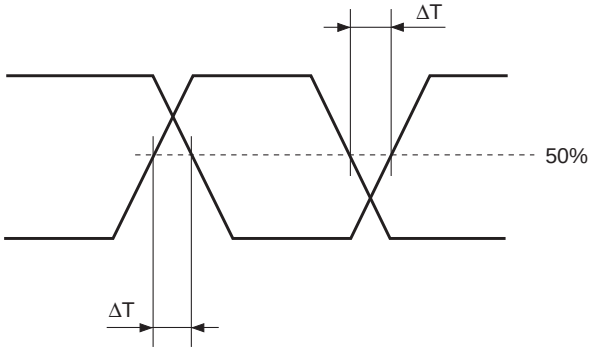


Fig. 3. Cross-point time difference measurement conditions

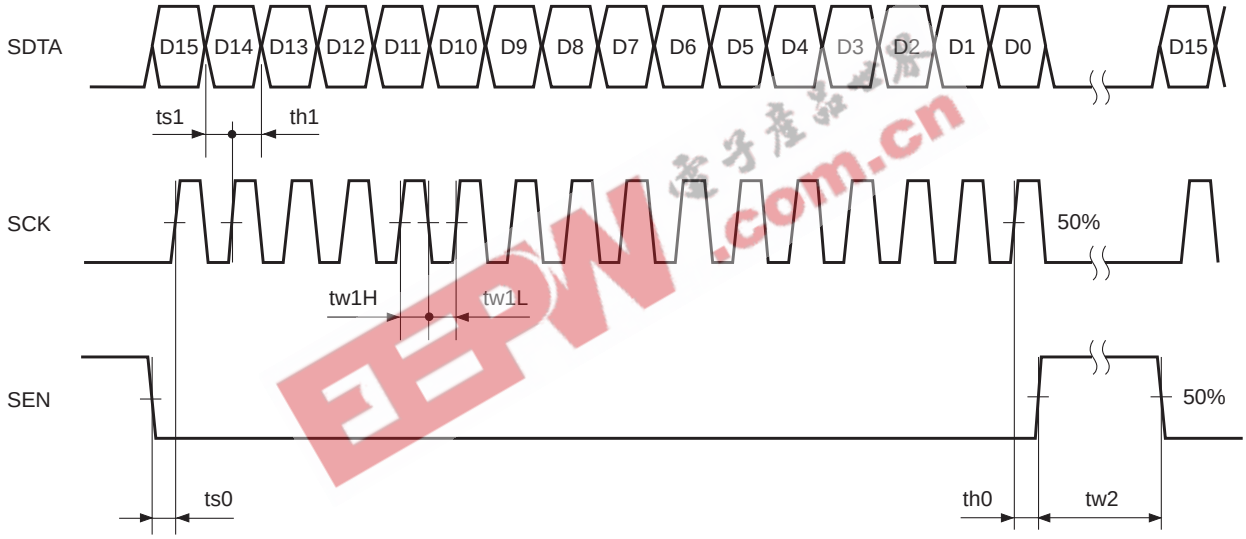
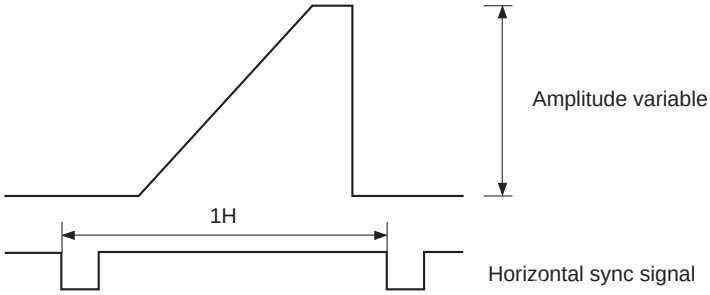
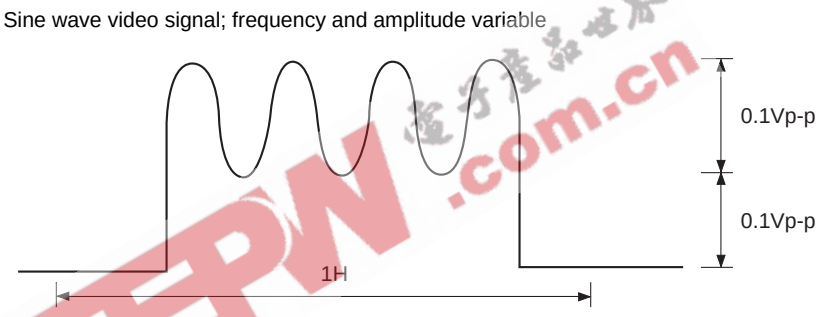
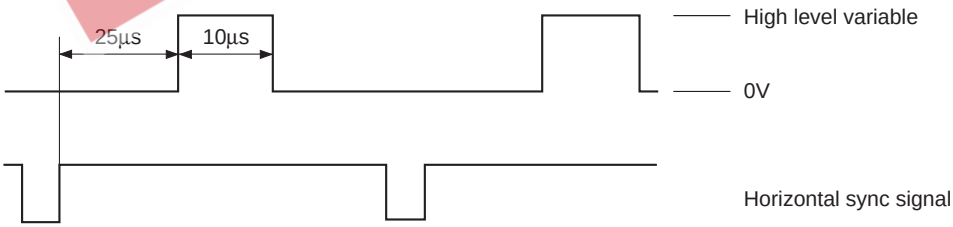
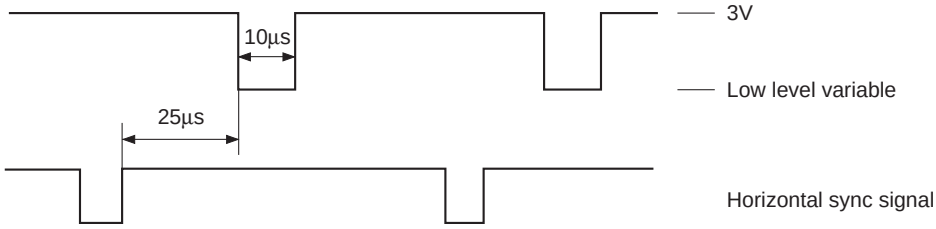
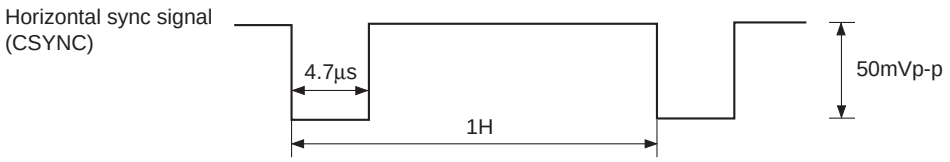
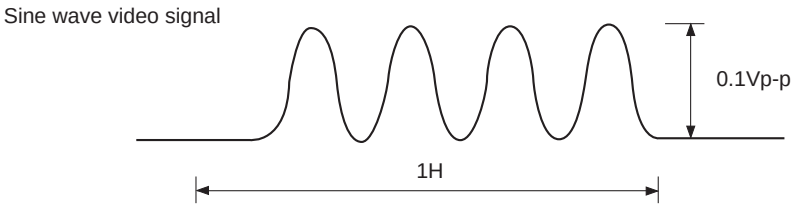
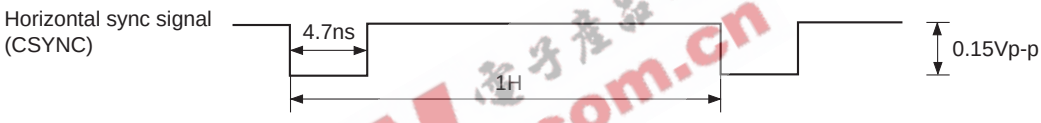
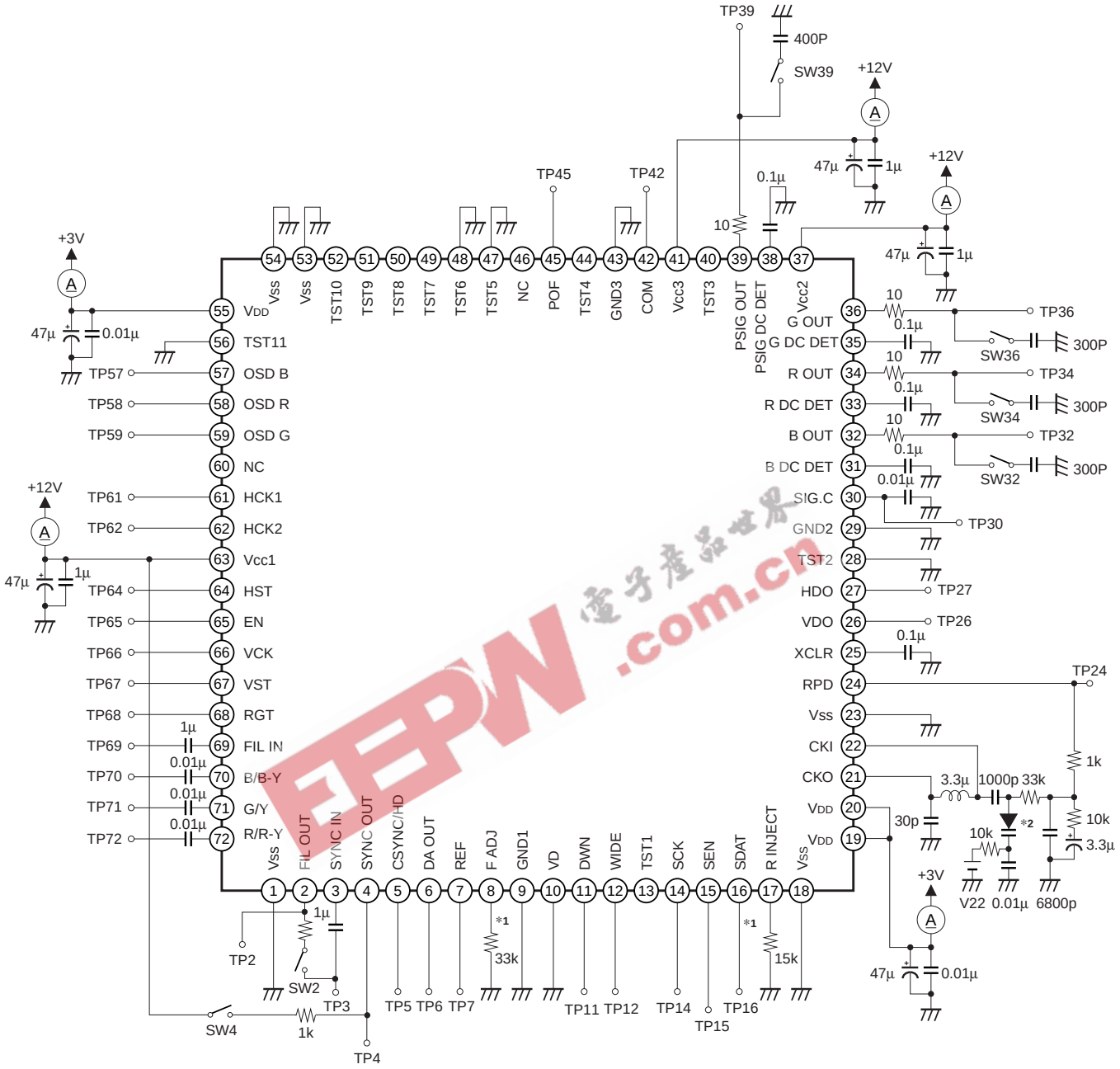


Fig. 4. Serial transfer block measurement conditions

SG No.	Waveform
SG1	
SG2	
SG3	
SG4	
SG5	

SG No.	Waveform
SG6	
SG7	
SG8	

Electrical Characteristics Measurement Circuit



*1 Resistance value tolerance: ±2%, temperature coefficient: ±200ppm or less
Locate this resistor as close to the IC pin as possible to reduce the effects of external signals.
*2 Varicap diode: 1T369 (SONY)

Description of Operation

1) RGB and Y/color difference signal processing block

Signal processing is comprised of picture, hue, matrix, LPF/trap, contrast, OSD, sample-and-hold, γ correction, bright, sub-bright, sub-contrast and output circuits

• Input signal mode switching

The input mode (RGB input, Y/color difference input) can be switched by the serial communication settings.

(During internal sync separation signal input)

During RGB input: The G signal is input to Pins 71 and 69, the B signal to Pin 70, and the R-Y signal to Pin 72.

During Y/color difference input: The Y signal is input to Pins 71 and 69, the B-Y signal to Pin 70, and the R-Y signal to Pin 72.

(During external sync signal input)

During RGB input: The G signal is input to Pin 71, the B signal to Pin 70, the R signal to Pin 72, CSYNC/HD to Pin 5, and VD to Pin 10.

During Y/color difference input: The Y signal is input to Pin 71, the B-Y signal to Pin 70, the R-Y signal to Pin 72, CSYNC/HD to Pin 5, and VD to Pin 10.

• NTSC/PAL switching

The input system (NTSC/PAL) can be switched by the serial communication settings.

• Picture circuit

This performs aperture correction for the Y signal. The center frequency to be corrected and the correction amount are controlled by serial communication. In addition, when not using the picture circuit, it can be turned off by serial communication.

• Hue circuit

This is the hue adjustment circuit for the color difference signal. It is controlled by serial communication.

• Matrix circuit

This circuit converts Y, R-Y and B-Y signals into RGB signals.

• LPF circuit

This is the band limitation filter for the RGB signal. It is used to eliminate the noise component generated at the front end of this IC. The cut-off frequency can be controlled by serial communication. In addition, when not using the LPF, it can be turned off by serial communication.

• Trap circuit

This is used to eliminate the DSP clock and RGB decoder carrier leak generated at the front end of this IC. The center frequency can be switched between 13.5MHz and 14.3MHz by serial communication. In addition, when not using the trap, it can be turned off by serial communication.

• Contrast adjustment circuit

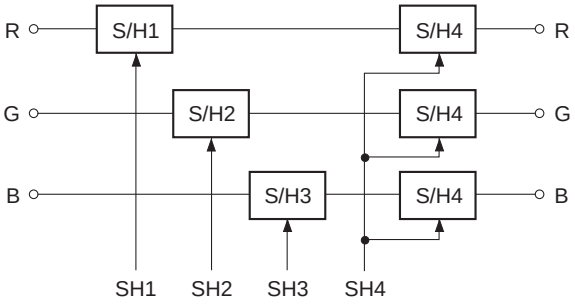
This adjusts the white-black amplitude to set the input RGB signal to the appropriate output level.

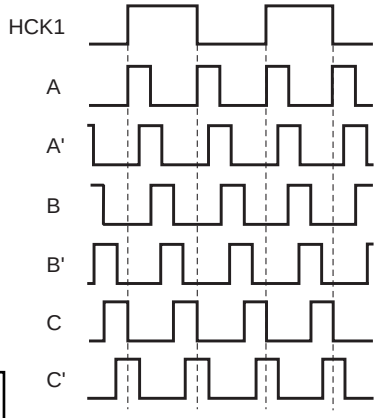
• OSD

This inputs the OSD pulses. There are two input threshold values: Vth1 ($V_{CC}1 \times 1/3$) and Vth2 ($V_{CC}1 \times 2/3$). When an input exceeds Vth1, the corresponding output falls to the level specified by BLACK-LIMITE. When an input exceeds Vth2, the corresponding output rises to the level specified by WHITE-LIMITER. Also, when one of the RGB inputs exceeds Vth1, any signal outputs not exceeding Vth1 also fall to the level specified by BLACK-LIMITER.

• Sample-and-hold circuit

This circuit performs time axis correction for the RGB output signals in order to support the RGB simultaneous sampling systems of LCD panels.





SH1: R signal SH pulse
SH2: G signal SH pulse
SH3: B signal SH pulse
SH4: RGB signal SH pulse

SHS1,2,3,4,5,6: Serial data settings

RGT = H (normal)

	SHS1	SHS2	SHS3	SHS4	SHS5	SHS6
SH1	B	A'	A	C'	C	B'
SH2	Through	Through	Through	Through	Through	Through
SH3	A	C'	C	B'	B	A'
SH4	C	B'	B	A'	A	C'

RGT = L (right/left inversion)

	SHS1	SHS2	SHS3	SHS4	SHS5	SHS6
SH1	B	A'	A	C'	C	B'
SH2	A	C'	C	B'	B	A'
SH3	Through	Through	Through	Through	Through	Through
SH4	C	B'	B	A'	A	C'

The sample-and-hold circuit performs sample-and-hold by receiving the SH1 to SH4 pulses from the TG block. Since LCD panels perform color coding using an RGB delta arrangement, each horizontal line must be compensated by 1.5 dots. This relationship is reversed during right/left inversion. This compensation and other timing is also generated by the digital block. The sample-and-hold timing changes according to the phase relationship with the HCK pulse, so the timing should be set to the SHS1, 2 or 6 position in accordance with the actual board.

• γ correction

In order to support the characteristics of LCD panels, the I/O characteristics are as shown in Fig. 1. The γ1 gain transition point A voltage changes as shown in Fig. 2 by adjusting the serial bus register γ1, and the γ2 gain transition point B voltage changes as shown in Fig. 3 by adjusting γ2.

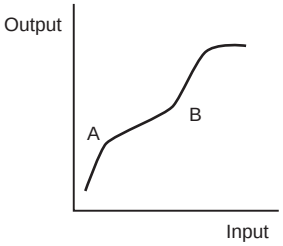


Fig. 1

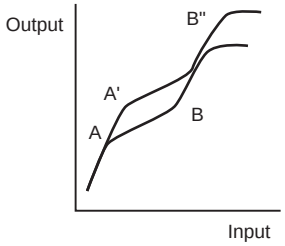


Fig. 2

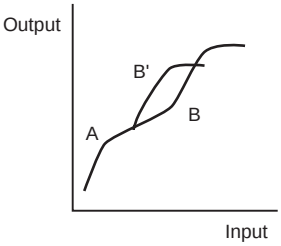
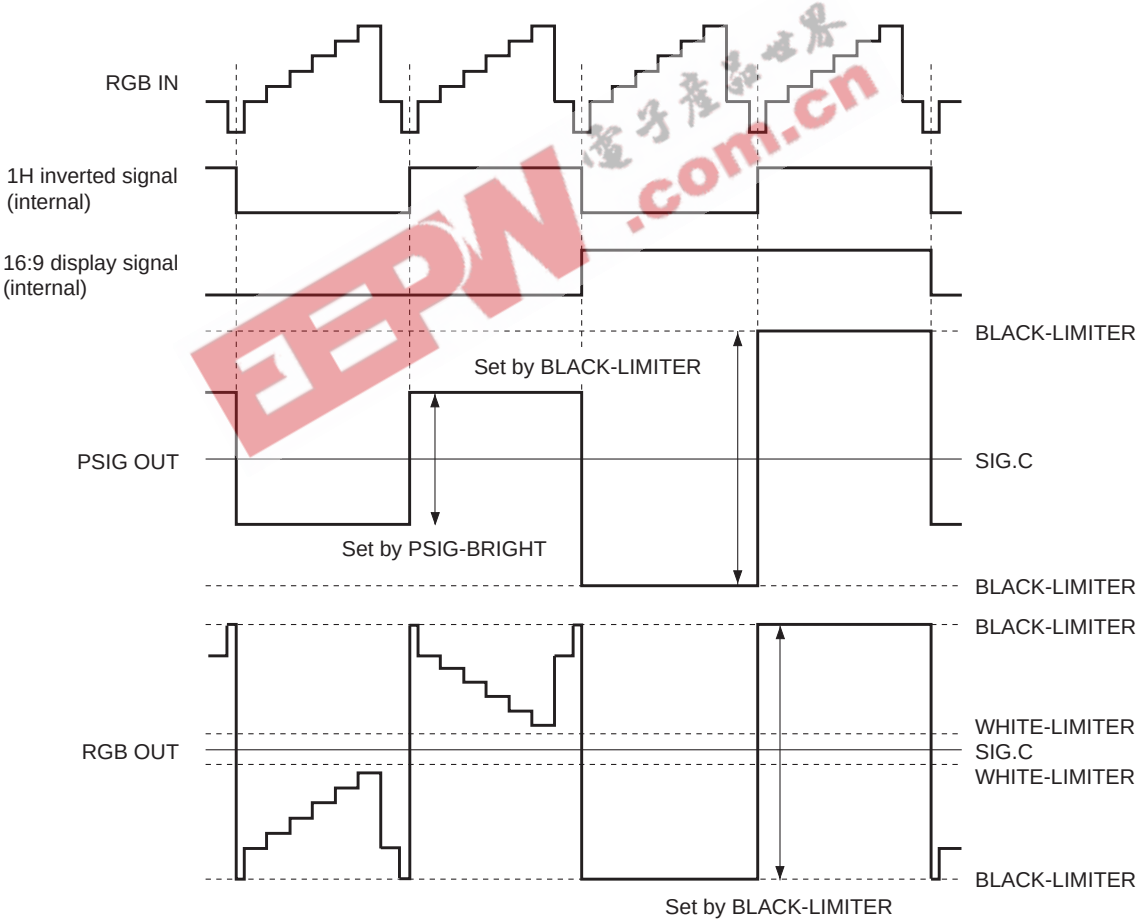


Fig. 3

• Bright circuit
This is used to adjust the black-black amplitude of polarity-inverted RGB output signals. It is not interlinked with the γ transition points.

• White balance adjustment circuit
This is used to adjust the white balance. The black level is adjusted by SUB-BRIGHT, and the black-white amplitude is adjusted by SUB-CONTRAST.

• Output circuit
RGB output (Pins 70, 71, and 72) signals are inverted each horizontal line by the FRP pulse (internal pulse) supplied from the TG block as shown in the figure below. Feedback is applied so that the center voltage (SIG.C) of the output signal matches the reference voltage ($V_{CC}2$ + GND2)/2 (or the voltage input to SIG.C (Pin 30)). In addition, the white level output is clipped at the limiter operation point that is set by the serial communication WHITE-LIMITER, and the black level output is clipped at the limiter operation point that is set by the serial communication BLACK-LIMITER.
The output PSIG signal level is normally adjusted by PSIG-BRIGHT, but during 16:9 display the level is specified by BLACK-LIMITER during V blanking. In addition, the RGB output also simultaneously goes to BLACK-LIMITER level output.



2) Common voltage generation circuit block

The common voltage circuit generates and supplies the common pad voltage to the LCD panel. The voltage is offset by serial communication using the SIG.C voltage as the reference and then output.

3) DAC output circuit

There are two DAC output circuit systems. The DA OUT output circuit outputs DC 3.0V at equal divisions. The REF output circuit generates and supplies the REF voltage for the panel level shifter circuit to the LCD panel. Both circuits are controlled by serial communication.

4) Sync system

• H FIL

This amplifies the sync signal of the input video signal and eliminates the noise with an internal LPF. The sync signal is clamped at the input, so be sure to input via a capacitor.

• SYNC SEP

This inputs the FIL OUT (Pin 2) output and performs sync separation. The signal is output from SYNC OUT (Pin 4) as a positive polarity pulse.

5) Power saving circuit (PS circuit)

A power saving system can be realized together with the LCD panel by independently controlling (serial communication) the operation of each output block. This system is also effective for improving picture quality during power-on/off.

The serial data PS0, PS1, PS2, PS4 and SYNC GEN must be set in order to use this IC. For details of the setting methods, see the "Description of Serial Control Operation" and "Power Supply and Power Saving Sequence" items.

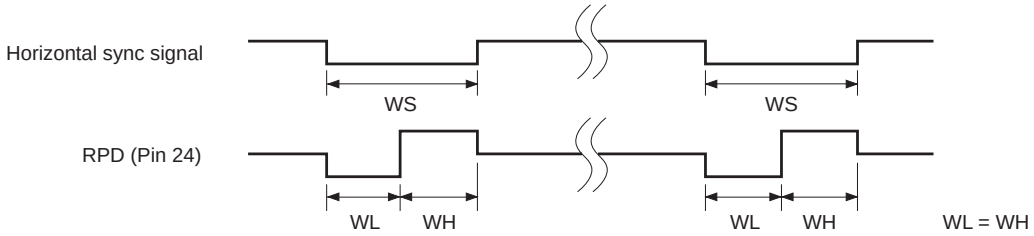
6) TG block

• PLL and AFC circuits

A PLL circuit can be comprised by connecting a PLL circuit phase comparator and frequency division counter and external VCO and LPF circuits.

The PLL error detection signal is generated using the phase comparison output of the entire bottom of the horizontal sync signal and the internal frequency division counter as the RPD output. RPD output is converted to DC error voltage with the lag-lead filter, and then it changes the capacitance of the varicap diode to stabilize the oscillation frequency.

The PLL of this system is adjusted by setting the reverse bias voltage of the varicap diode so that the point at which RPD changes is at the center of the horizontal sync signal window as shown in the figure below.



• H-Position

This adjusts the horizontal display position. Set this function so that the picture center matches the center of the LCD panel.

• Right/left (RGT) and/or up/down inversion (DWN)

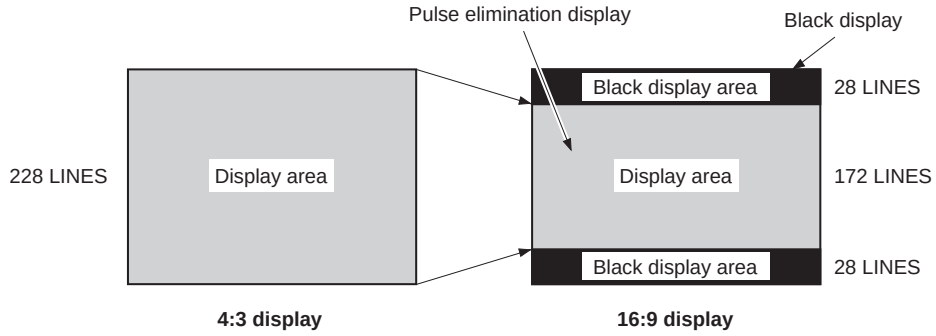
The video display direction can be switched. The horizontal direction can be switched between right scan and left scan, and the vertical direction between down scan and up scan. Set the display direction in accordance with the LCD panel mounting position.

• Wide mode

16:9 quasi-WIDE display can be achieved by converting the aspect ratio through pulse elimination processing.

During wide mode, vertical pulse elimination scanning is performed for both NTSC and PAL display and the video signal is compressed to achieve a 16:9 aspect ratio. In addition, in areas outside the display area, the black level set by BLACK-LIMITER (serial communication data) is wide-masked as the black signal within the limited vertical blanking period.

This function achieves a quasi-display by simply pulse eliminating the video signal, so some video information is lost.



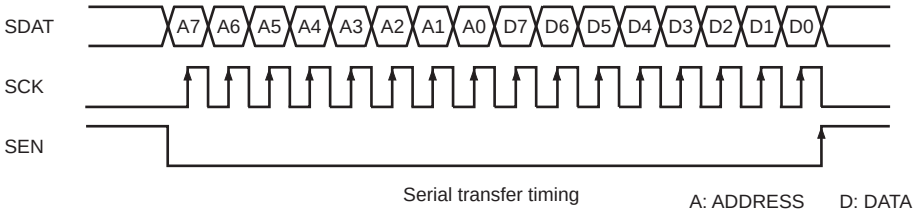
• AC driving of LCD panels during no signal

The output signal runs freely so that the LCD panel is AC driven even when there is no sync signal from the FIL IN (Pin 69) pin or from the CSYNC/HD (Pin 5) and VD (Pin 10) pins. During this time, the sync separation circuit stops and the auxiliary counter is used to generate the free running output pulses after detecting that there is no vertical sync signal for approximately 3 fields (no signal state).

Description of Serial Control Operation

1) Control method

Control data consists of 16 bits of data which is loaded one bit at a time at the rising edge of SCK. This loading operation starts from the falling edge of SEN and is completed at the next rising edge.
Digital block control data is established by the vertical sync signal, so if data is transferred multiple times for the same item, the data immediately before the vertical sync signal is valid. Analog (electronic attenuator) block control data becomes valid each time the SEN signal is input.
In addition, if 16 bits of more of SCK are not input while SEN is low, the transferred data is not loaded to the inside of the IC and is ignored. If 16 bits or more of SCK are input, the 16 bits of data before the rising edge of the SEN pulse are valid data.



2) Serial data map

The serial data map is as follows. Values inside parentheses are the default values.

MSB ADDRESS LSB								MSB DATA LSB							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	USER-BRIGHT (10000000/LSB)							
0	0	0	0	0	0	0	1	SUB-BRIGHT R (10000000/LSB)							
0	0	0	0	0	0	1	0	SUB-BRIGHT B (10000000/LSB)							
0	0	0	0	0	0	1	1	CONTRAST (10000000/LSB)							
0	0	0	0	0	1	0	0	SUB-CONTRAST R (10000000/LSB)							
0	0	0	0	0	1	0	1	SUB-CONTRAST B (10000000/LSB)							
0	0	0	0	0	1	1	0	γ-2 (00000000/LSB)							
0	0	0	0	0	1	1	1	γ-1 (00000000/LSB)							
0	0	0	0	1	0	0	0	(0)	PSIG-BRIGHT (1000000/LSB)						
0	0	0	0	1	0	0	1	COM-DC (10000000/LSB)							
0	0	0	0	1	0	1	0	COLOR (10000000/LSB)							
0	0	0	0	1	0	1	1	HUE (10000000/LSB)							
0	0	0	0	1	1	0	0	(0)	WHITE-LIMITER (00/LSB)	BLACK-LIMITER (10000/LSB)					
0	0	0	0	1	1	0	1	FILTER (00/LSB)		REF (011/LSB)			LPF (000/LSB)		
0	0	0	0	1	1	1	0	PICTURE-GAIN (00000/LSB)					(0)	PICTURE-F0 (00/LSB)	
0	0	0	0	1	1	1	1	(0)	(0)	(0)	(0)	MODE (0)	DA (000/LSB)		
0	0	0	1	0	0	0	0	(0)	(0)	SYNC GEN (1)	PS 4 (1)	(0)	PS 2 (1)	PS 1 (1)	PS 0 (1)
0	0	1	0	0	0	0	0	SLSYP (0)	SLEXVD (0)	SLDWN (0)	SLRGT (0)	SLSH2 (0)	SLSH1 (0)	SLWD (0)	SLPL (0)
0	0	1	0	0	0	0	1	(0)	SLFL (0)	SLFR (0)	SL4096 (0)	SLCLP2 (0)	SLCLP1 (0)	SLVDP (0)	SLHDP (0)
0	0	1	0	0	0	1	0	(0)	(0)	SLTST4 (0)	SLTST3 (0)	SLSH0 (0)	SLTST2 (0)	SLTST1 (0)	SLTST0 (0)
0	0	1	0	0	0	1	1	(0)	(0)	(0)	H-POSITION (10000/LSB)				
0	0	1	0	0	1	0	0	(0)	(0)	(0)	HD-POSITION (00000/LSB)				

Note) If there is the possibility that data may be set at other than the above-noted addresses, set these data to "0".

3) Description of control data

• USER-BRIGHT
This adjusts the brightness of the RGB output signals. Adjustment from LSB → MSB increases the amplitude (black-black).

• SUB-BRIGHT R/B
This adjusts the brightness of the R and B output signals using the G output signal as the reference. Adjustment from LSB → MSB increases the amplitude (black-black).

• CONTRAST
This adjusts the contrast of the RGB output signals. Adjustment from LSB → MSB increases the amplitude (black-white).

• SUB-CONTRAST R/B
This adjusts the contrast of the R and B output signals using the G output signal as the reference. Adjustment from LSB → MSB increases the amplitude (black-black).

• γ-2
This sets the white side γ point level of the RGB output signals. Adjustment from MSB → LSB lowers the γ point. When not adjusting γ-2, set γ-2: 11111111 (LSB). Set the γ-2 point to the white side of the γ-1 point.

• γ-1
This sets the black side γ point level of the RGB output signals. Adjustment from MSB → LSB lowers the γ point. When not adjusting γ-1, set γ-1: 11111111 (LSB). Set the γ-1 point to the black side of the γ-2 point.

• PSIG-BRIGHT
This adjusts the bright level of the PSIG output signal. Adjustment from LSB → MSB increases the amplitude (peak to peak).
Note: Do not set PSIG-BRIGHT: 0000000 (LSB), as this setting turns off the internal PSIG circuit.

• COM-DC
This adjusts the COMMON output voltage. Adjustment from LSB → MSB increases the output voltage.

• COLOR
This adjusts the color gain during Y/color difference input. Adjustment from LSB → MSB increases the gain.

• HUE
This adjusts the phase during Y/color difference input. Adjustment from LSB → MSB advances the phase.

• WHITE-LIMITER
This adjusts the white side limiter level of the RGB output signals. See the AC Characteristics for the output level.

• BLACK-LIMITER
This adjusts the black side limiter level of the RGB output signals. Adjustment from LSB → MSB lowers the limiter level.

• LPF

This switches the frequency response of the low-pass filter. Set the fc/–3dB frequency relative to the amplitude 100kHz reference. See the AC Characteristics for the output level.

D2	D1	D0	fc (RGB input/no load/typ.)
0	0	0	LPF OFF
0	0	1	2.0MHz
0	1	0	2.7MHz
0	1	1	3.4MHz
1	0	0	3.9MHz
1	0	1	4.9MHz
1	1	0	5.7MHz
1	1	1	6.4MHz

• REF

This adjusts the REF output voltage. Adjustment from LSB → MSB raises the output voltage level. See the AC Characteristics for the output level.

• FILTER

This sets the trap (f0) center frequency. See the AC Characteristics for the output level.

D7	D6	Center frequency (f0)
0	0	TRAP OFF
0	1	13.5MHz
1	0	14.3MHz
1	1	—

• PICTURE-F0

This sets the picture center frequency (f0) during Y/color difference input. See the AC Characteristics for the output level.

D1	D0	Center frequency (f0)
0	0	2.0MHz (typ.)
0	1	2.2MHz (typ.)
1	0	2.6MHz (typ.)
1	1	2.9MHz (typ.)

• PICTURE-VOLUME

This adjusts the picture gain during Y/color difference input. Adjustment from LSB → MSB raises the gain. When not using the picture function (OFF), set PICTURE-VOLUME: 00000 (LSB).

• DA

This adjusts the DA output voltage. See the AC Characteristics for the output level.

• MODE

This switches the input signal.

D3	Input signal
0	RGB input
1	Y/color difference input

• SYNC GEN

This sync generator mode stops all output pulses other than the HDO and VDO output pulses. The PS0, PS1, PS2 and PS4 settings have priority over the SYNC GEN setting. Normally set to "0".

D5	Mode (SYNC GEN)
0	Normal operation
1	All output pulses and corresponding output blocks other than the HDO and VDO output pulses are stopped.

• PS0, PS1, PS2, PS4

These perform the power saving settings for each input and output block. Be sure to use these settings as described in "Power Supply and Power Saving Sequence". The power-on default for this IC is power saving mode, so the settings should be canceled by serial communication after power-on.

D0, 1, 2, 4	Mode (PS0, PS1, PS2, PS4)
0	Normal operation
1	The respective outputs and corresponding output blocks are stopped.

Power Supply and Power Saving Sequence

When using this IC, the power supply sequences described below must be followed during power-on/off to ensure reliability as a LCD driving system. Thoroughly study the function specifications of each control method (1), (2) and (3) before use.

Control timing (1)
Use this timing when not using the power saving (PS) function regardless of picture quality during power-on/off.

Control timing (2)
Use this timing when using the power saving (PS) function regardless of picture quality during power-on/off. Note that in this case an external switch is necessary.

Control timing (3)
Use this timing when using the power saving (PS) function and placing priority on picture quality during power-on/off. Note that in this case an external switch is necessary.

Control timing (1)

(1) IC power-on (3V, 12V), LCD power-on (HV_{DD}, VV_{DD})
(2) A settings: after the IC and LCD power supplies have risen
(3) IC power-off (3V, 12V), LCD power-off (HV_{DD}, VV_{DD}): optional

The LCD power supply (HV_{DD}, VV_{DD}) rise timing should adequately satisfy the panel specifications.
Serial data settings other than PS should be made during the control period from the rise of the IC 3V power supply to (2).

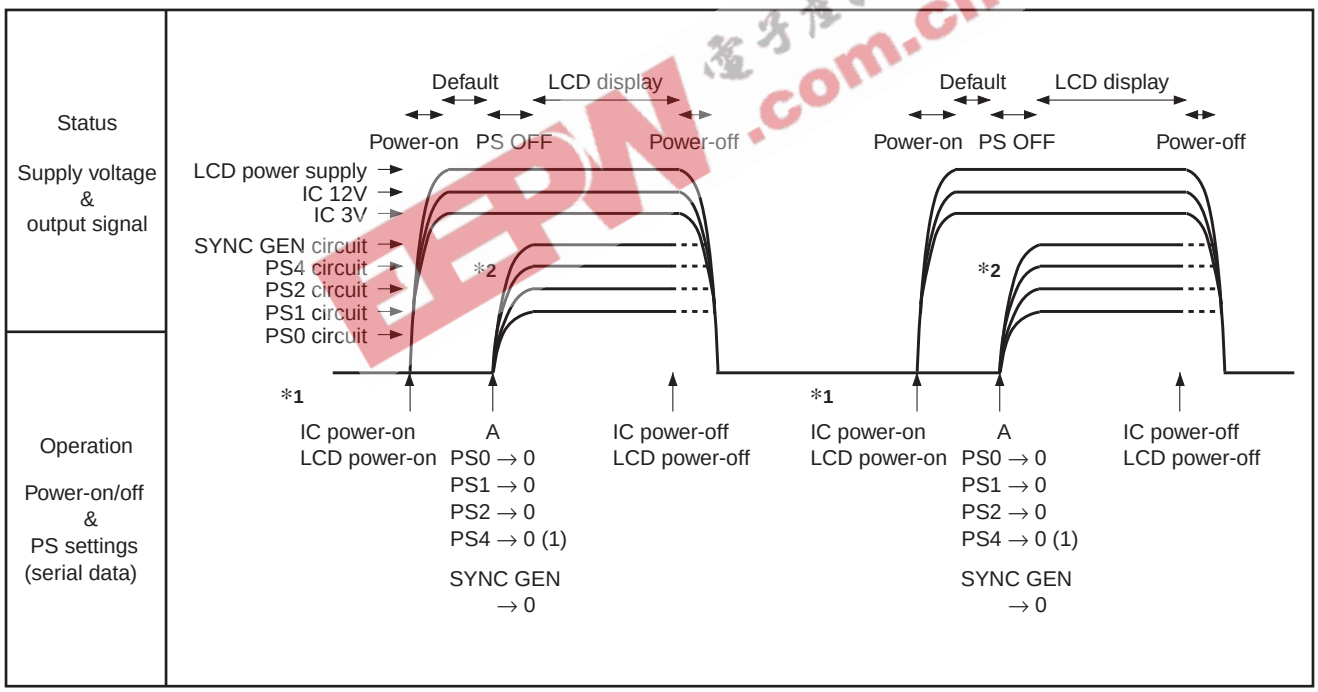


Fig. 1

*1 During IC power-on (default status), the PS mode is activated (the PS0, PS1, PS2, PS4 and SYNC GEN data are all set to "1"). Therefore, the PS settings should be canceled via serial communication in accordance with the sequence specifications.

*2 When inputting the sync signal from an external source, set serial data PS4 = 1.

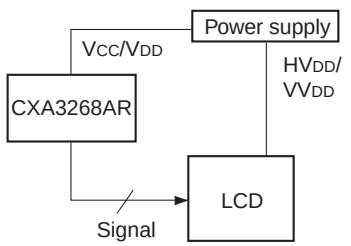


Fig. 2. System block diagram

Control timing (2)

(1) IC power-on (3V, 12V), LCD power-on (HV_{DD}, VV_{DD})
(2) A settings: after the IC and LCD power supplies have risen
(3) B settings: optional
(4) IC power-off (3V, 12V), LCD power-off (HV_{DD}, VV_{DD}): optional
It is possible to skip from step (2) to step (4) without making the B settings (dotted lines in the figure).

The LCD power supply (HV_{DD}, VV_{DD}) rise timing should adequately satisfy the panel specifications. Serial data settings other than PS should be made during the control period from the rise of the IC 3V power supply to (2).

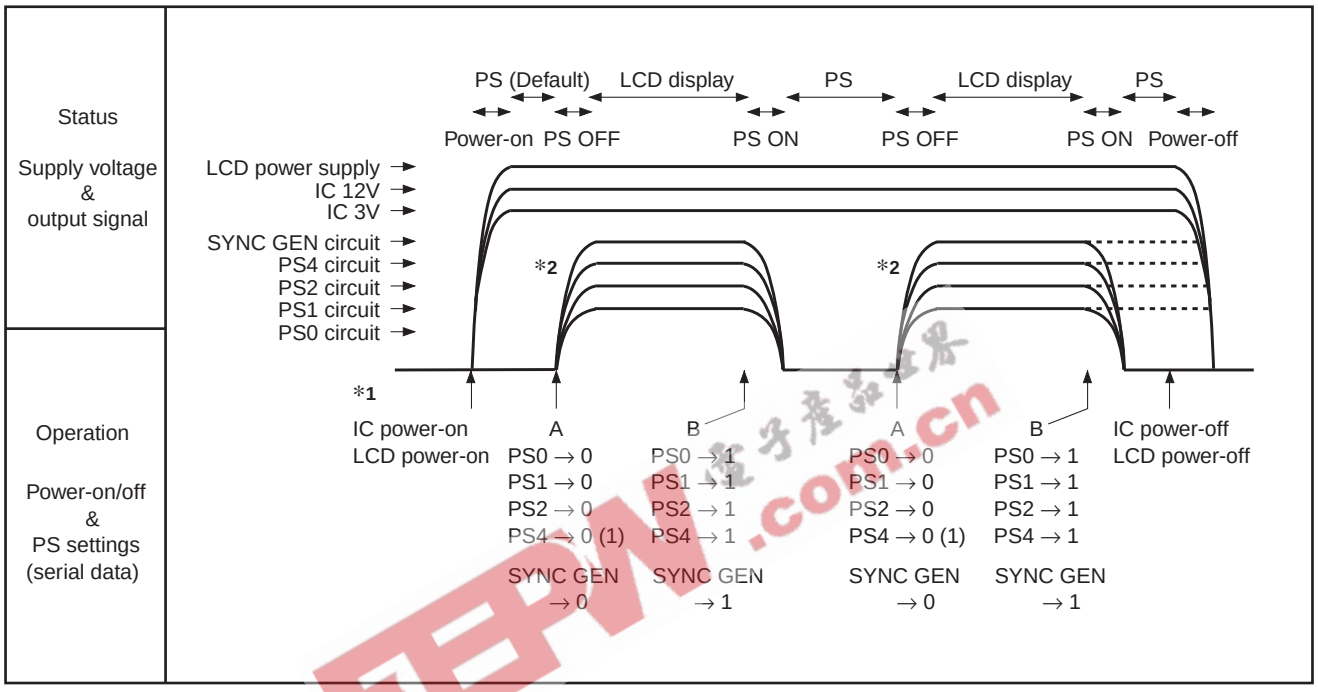


Fig. 1

*1 During IC power-on (default status), the PS mode is activated (the PS0, PS1, PS2, PS4 and SYNC GEN data are all set to "1"). Therefore, the PS settings should be canceled via serial communication in accordance with the sequence specifications.
*2 When inputting the sync signal from an external source, set serial data PS4 = 1.

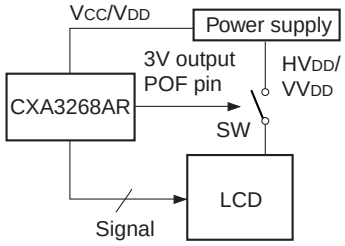


Fig. 2. System block diagram

Control timing (3)

(1) IC power-on (3V)
(2) IC power-on (12V), LCD power-on (HV_{DD}, VV_{DD}): after the IC power supply (3V) has completely risen
(3) A settings: after the IC (12V) and LCD power supplies have risen
(4) B settings: after the PLL has stabilized (stable RPD waveform) and the panel I/O power supply conditions have been satisfied.
(5) C settings: optional
(6) D settings: after COM/CS, RGB and PSIG have fallen
(7) E settings: 100ms or more after the D settings
(8) IC power-off (12V), LCD power-off (HV_{DD}, VV_{DD}): after the HV_{DD} and VV_{DD} pin voltages have fallen
(9) IC power-off (3V): after the IC power supply (12V) has completely fallen

Serial data settings other than PS should be made during the control period from the rise of the IC 3V power supply to (3).
The LCD power supply (HV_{DD}, VV_{DD}) rise timing should adequately satisfy the panel specifications.

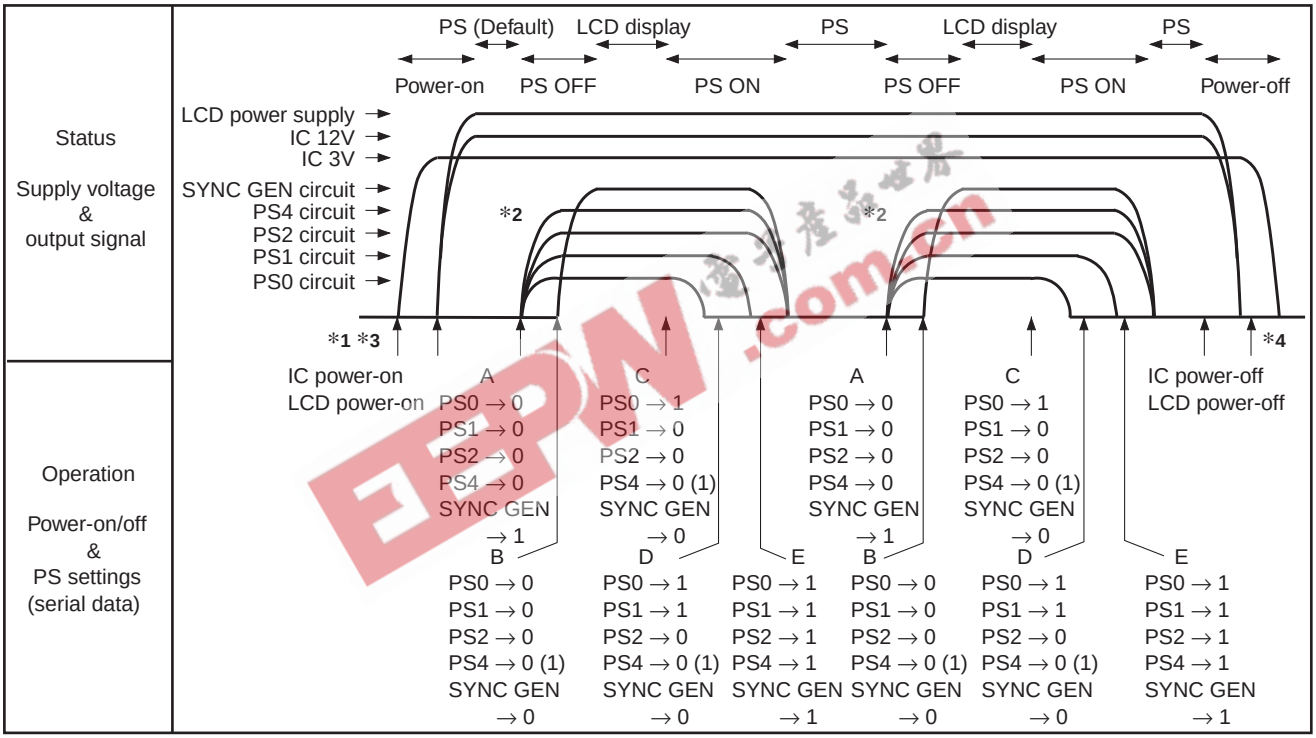


Fig. 1

*1 During IC power-on (default status), the PS mode is activated (the PS0, PS1, PS2, PS4 and SYNC GEN data are all set to "1"). Therefore, the PS settings should be canceled via serial communication in accordance with the sequence specifications.
*2 When inputting the sync signal from an external source, set serial data PS4 = 1.
*3 When raising the power supplies, first raise the IC 3V power supply, then raise the IC 12V and LCD power supplies.
*4 When lowering the power supplies, first lower the LCD and IC 12V power supplies, then lower the IC 3V power supply.

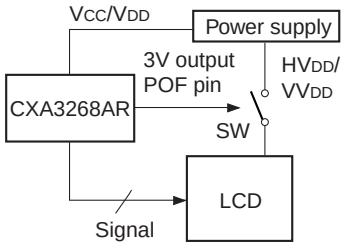


Fig. 2. System block diagram

• SLPL

This switches the display system.

D0	Display system
0	NTSC
1	PAL

• SLWD

This switches the display aspect.

D1	Supported aspect
0	4:3 display
1	16:9 display

• SLSH0, SLSH1, SLSH2

These switch the sample-and-hold timing.

SLSH2 D3	SLSH1 D2	SLSH0 D3	Sample-and-hold position
0	0	0	SHS1
0	0	1	SHS2
0	1	0	SHS3
0	1	1	SHS4
1	0	0	SHS5
1	0	1	SHS6
1	1	0	Through (sample-and-hold off)
1	1	1	Through (sample-and-hold off)

• SLRGT

This is the right/left inversion function. This switches the horizontal scan direction of the LCD panel.

D4	Scan mode
0	Normal display (right scan)
1	Right/left inverted display (left scan)

• SLDWN

This is the up/down inversion function. This switches the vertical scan direction of the LCD panel.

D5	Scan mode
0	Normal display (down scan)
1	Up/down inverted display (up scan)

• SLEXVD

This switches the external vertical sync signal (VD/Pin 10) input. This is used when not performing sync separation with the internal sync separation circuit during external separate sync (VD, HD/Pins 10 and 5) input. Set to "0" during external CSYNC/Pin 5 input.

D6	Mode
0	Other than during external vertical sync signal input
1	External vertical sync signal input

• SLSYP

This switches the input sync polarity. When using the Pin 4 (SYNC OUT) output as the sync signal (when using the internal sync separation signals), set this to "0".

D7	Input polarity
0	Positive polarity
1	Negative polarity

• SLHDP, SLVDP

These switch the HDO output and VDO output polarity.

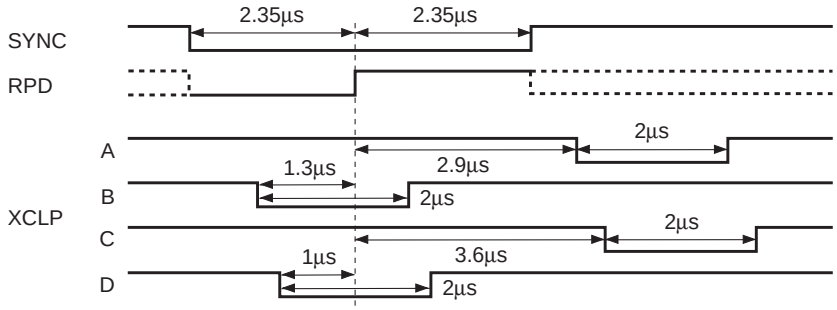
D0	Output polarity (HDO)
0	Positive polarity
1	Negative polarity

D1	Output polarity (VDO)
0	Positive polarity
1	Negative polarity

• SLCP1, SLCP2

These switch the clamp position.

D3	D2	Clamp position
0	0	A (Back porch position/when using the internal sync separation signals)
0	1	B (Sync position/when using the internal sync separation signals)
1	0	C (Back porch position/during external sync signal input)
1	1	D (Sync position/during external sync signal input)



Note) When clamp is performed at back porch and sync position, set back porch and sync period of Pins 69, 70, 71 and 72 input signals at pedestal level.

• SL4096

This function inverts the output signal polarity every 4096 fields. This further inverts the polarity of the RGB output that is inverted every 1H for 4096 fields. Normally set to 1H inversion.

D4	Mode
0	1H inversion
1	1H inversion + 4096 field inversion

• SLFR

This function inverts the output signal polarity every field. Normally set to 1H inversion.

D5	Mode
0	1H inversion
1	1 field inversion

• SLFL

This function is used to stop output signal polarity inversion. Normally set to polarity inversion.

D6	Mode
0	Polarity inversion
1	Polarity inversion stopped

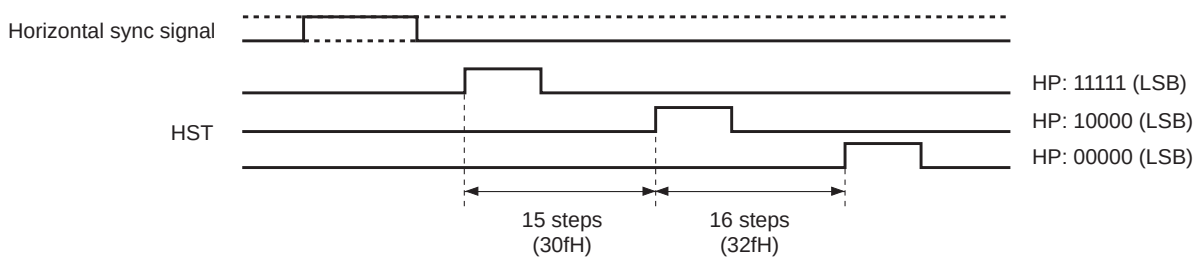
• SLTST0, 1, 2, 3, 4

These are the test functions. Set to normal mode.

D0, 1, 2, 3, 4	Mode
0	Normal mode
1	Test mode

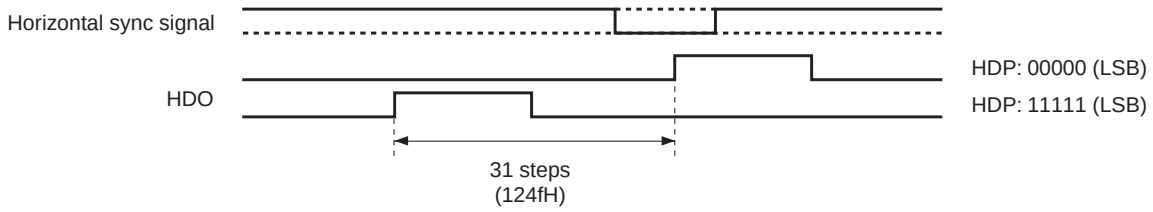
• HP1, 2, 3, 4, 5

These set the H position. The horizontal display position is switched by adjusting the HST pulse position using the input horizontal sync signal as the reference. Adjustment is possible in 1 bit = 2fH increments. (1fH = 1 dot)

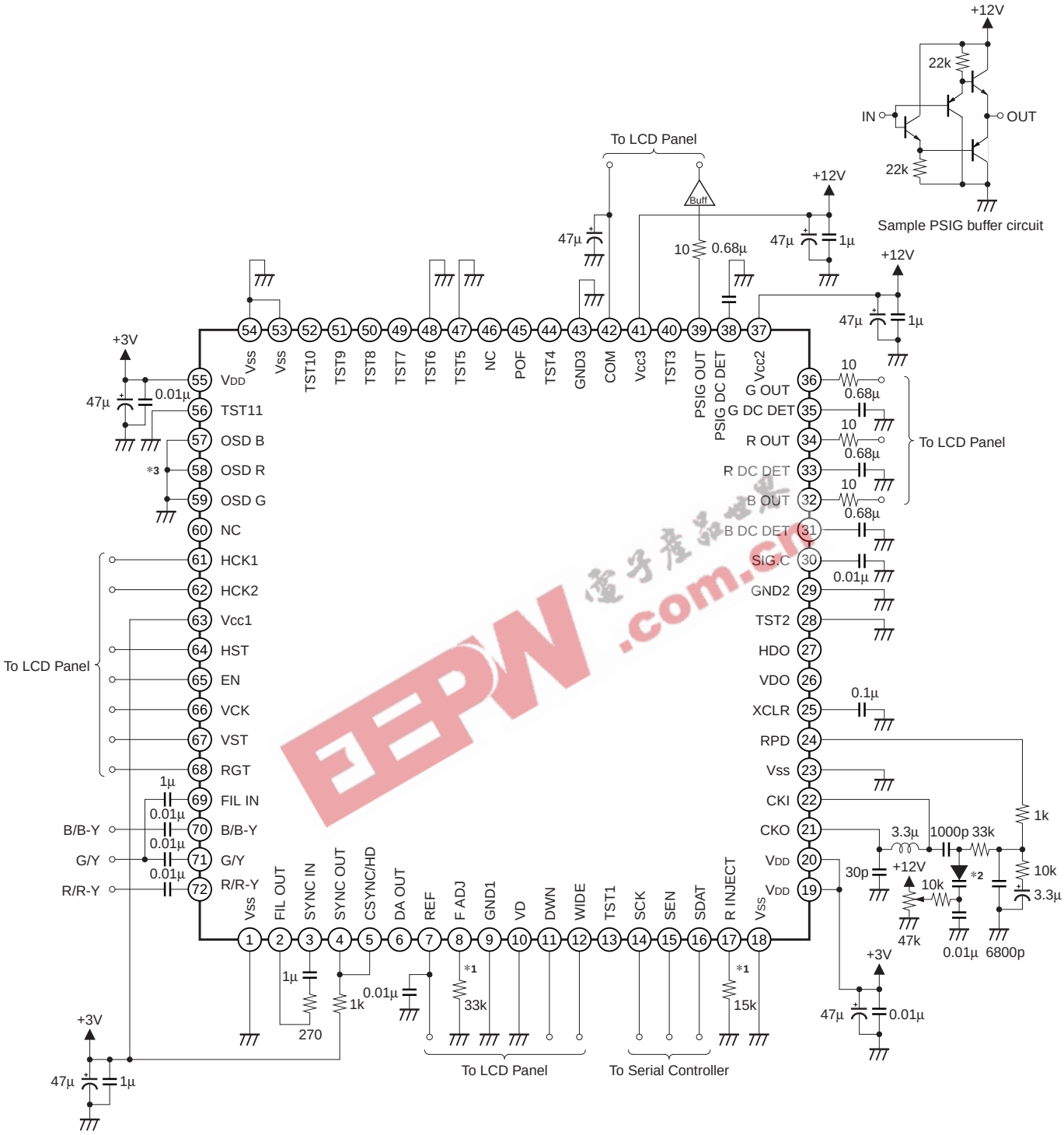


• HDP1, 2, 3, 4, 5

These set the HDO output pulse position. The HDO pulse output position is switched using the input horizontal sync signal as the reference. Adjustment is possible in 1 bit = 4fH increments. (1fH = 1 dot)



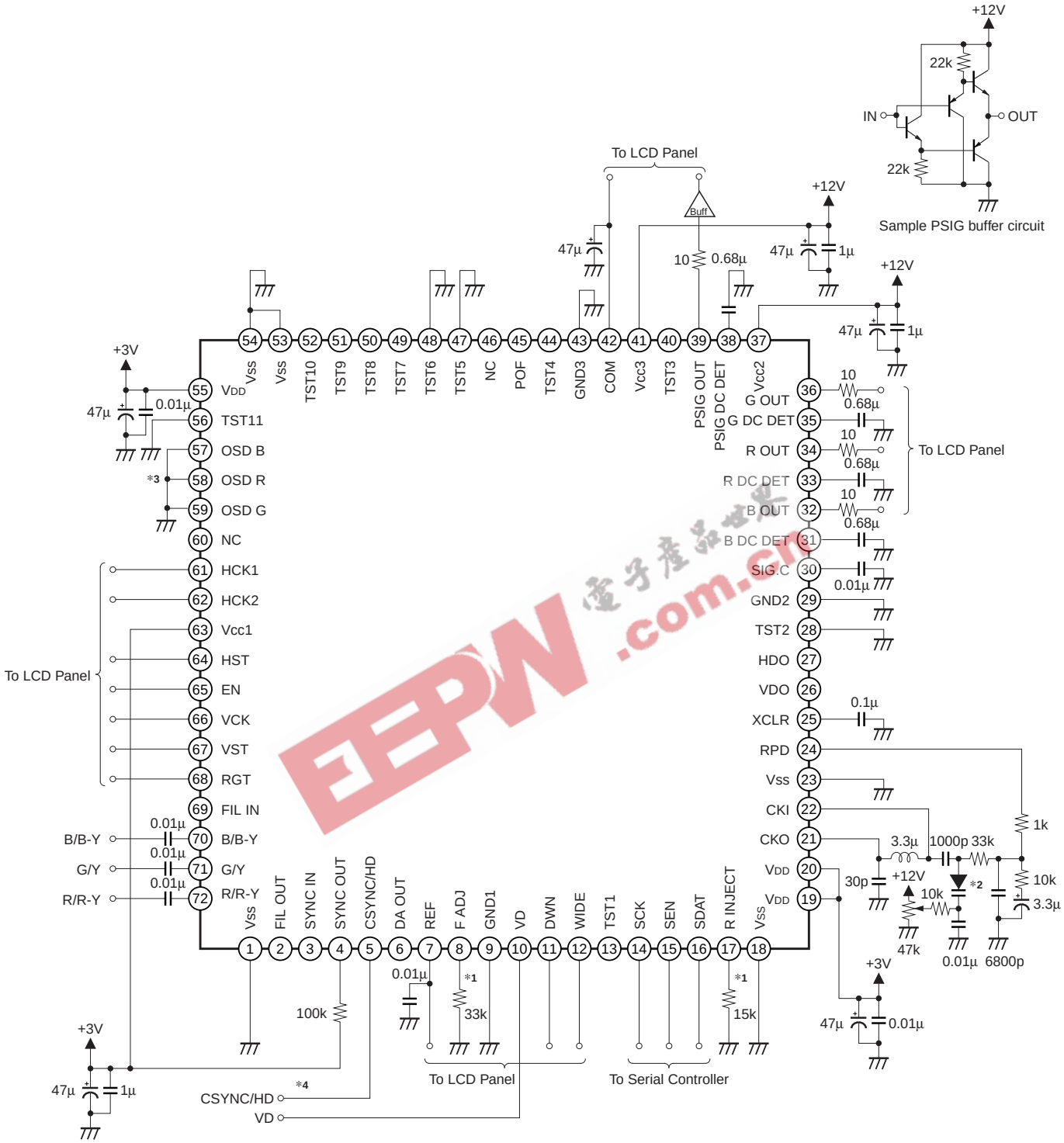
Application Circuit (RGB input/Y/color difference input, during internal sync separation signal input)



*1 Resistance value tolerance: ±2%, temperature coefficient: ±200ppm or less
Locate this resistor as close to the IC pin as possible to reduce the effects of external signals.
*2 Varicap diode: 1T369 (SONY)
*3 Connect to GND when not using OSD input.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (RGB input/Y/color difference input, during external sync signal input)



*1 Resistance value tolerance: ±2%, temperature coefficient: ±200ppm or less
Locate this resistor as close to the IC pin as possible to reduce the effects of external signals.
*2 Varicap diode: 1T369 (SONY)
*3 Connect to GND when not using OSD input.
*4 During CSYNC input, input to Pin 5 only (leave Pin 10 open). During separate sync (HD, VD) input, input to Pins 5 and 10.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

(1) This IC contains digital circuits, so the set board pattern must be designed in consideration of undesired radiation, interference to analog circuits, etc. Care should also be taken for the following items when designing the pattern.

- The digital and analog IC power supplies should be separated, but the GND and V_{SS} should not be separated and should use a plain GND (V_{SS}) pattern in order to reduce impedance as much as possible. The power supplies should also use a plain pattern.
- Use ceramic capacitors for the by-pass capacitors between the power supplies and GND, and connect these capacitors as close to the pins as possible.
- The resistor connected to Pin 8 should be connected as close to the pin as possible, and the wiring from the pin to GND should be as short as possible. Also, do not pass other signal lines close to this pin or the connected resistor.
- The resistor connected to Pin 17 should be located as close to the pin as possible. Also, do not pass other signal lines close to this pin.
- The capacitors connected to Pins 7 and 42 should be located as close to the LCD panel as possible.
- The PLL block (LPF/VCO) should be compact and located near the IC.

(2) The R/R-Y (Pin 72), G/Y (Pin 71), B/B-Y (Pin 70) and FIL IN (Pin 69) pin input signals are clamped at the inputs using the capacitors connected to each pin, so these signals should be input at sufficiently low impedance.
(Input at an impedance of 1kΩ (max.) or less.)

(3) The smoothing capacitor of the DC level control feedback circuit in the capacitor block connected to the RGB output pins should have a leak current with a small absolute value and variance. Also, when using the pulse elimination (PAL display, WIDE display) function, the picture quality should be thoroughly evaluated before deciding the capacitance value of the capacitor.

(4) A thorough study of whether the capacitor connected to the COM output pin satisfies the LCD panel specifications should be made before deciding the capacitance value.

(5) If this IC is used in connection with a circuit other than an LCD, it may cause that circuit to malfunction depending on the order in which power is supplied to the circuits. Thoroughly study the consequences of using this IC with other circuits before deciding on its use.

(6) Since this IC utilizes a C-MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, or due to interface with the power supply of another circuit, or due to the order in which power is supplied to circuits. Be sure to take measures against the possibility of latch up.

(7) Be sure to observe the power supply and power saving sequence specifications specified for this IC.

(8) Do not apply a voltage higher than V_{DD} or lower than V_{SS} to I/O pins.

(9) Do not use this IC under operating conditions other than those given.

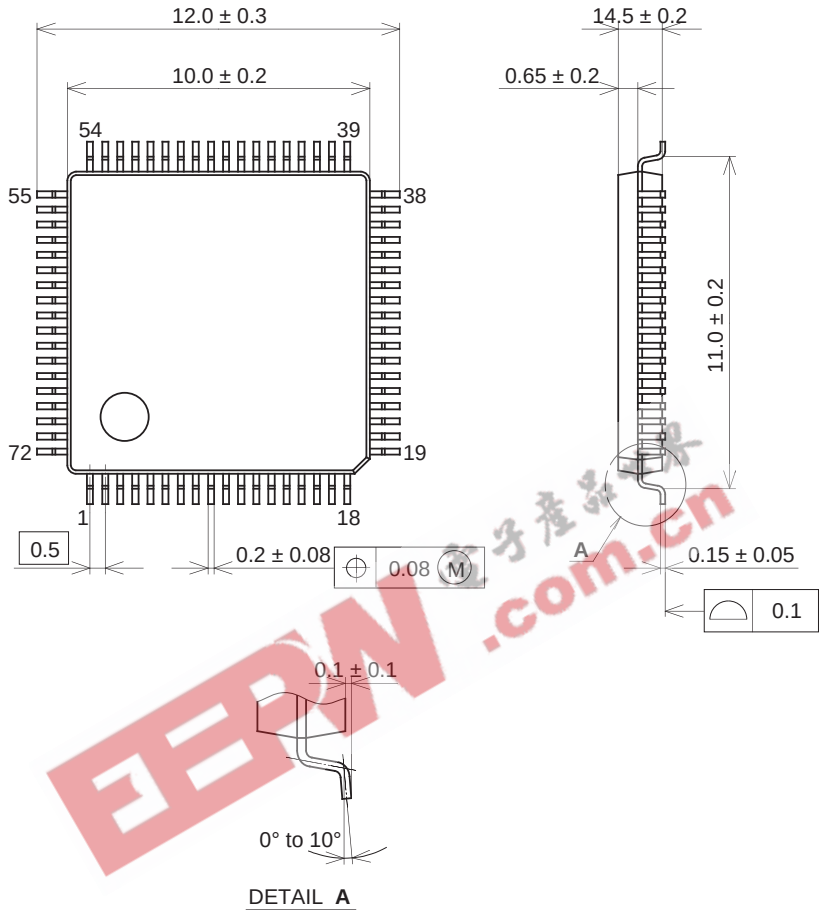
(10) Absolute maximum rating values should not be exceeded even momentarily. Exceeding ratings may damage the device, leading to eventual breakdown.

(11) This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.

(12) Always connect the V_{SS}, GND1 and GND2/3 pins to the lowest potential applied to this IC; do not leave these pins open. The voltages applied to the power supply pins should be as follows.
V_{SS} = GND1 = GND2/3 ≤ V_{DD} = $V_{CC}1$ ≤ $V_{CC}2$ = $V_{CC}3$.

Package Outline Unit: mm

72PIN LQFP (PLASTIC)



SONY CODE	LQFP-72P-L111
EIAJ CODE	P-LQFP72-10X10-0.5
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.3g