SONY

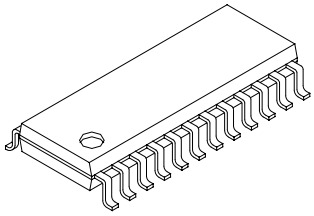
CXA2039M

Base Band Hue/Color Control

Description

The CXA2039M is a bipolar color difference signal processing IC for color TVs. This chip enables base band hue and color control for color difference signals.

24 pin SOP (Plastic)



Features

- 2 UV inputs, 1 UV output
- 3 Y inputs, 2 Y outputs
  (1 of the 2 outputs outputs either of 2 inputs.)
- Built-in color difference signal delay line circuit

Absolute Maximum Ratings

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	780	mW

Operating Conditions

Supply voltage	V_{CC}	9 ± 0.5	V

Applications

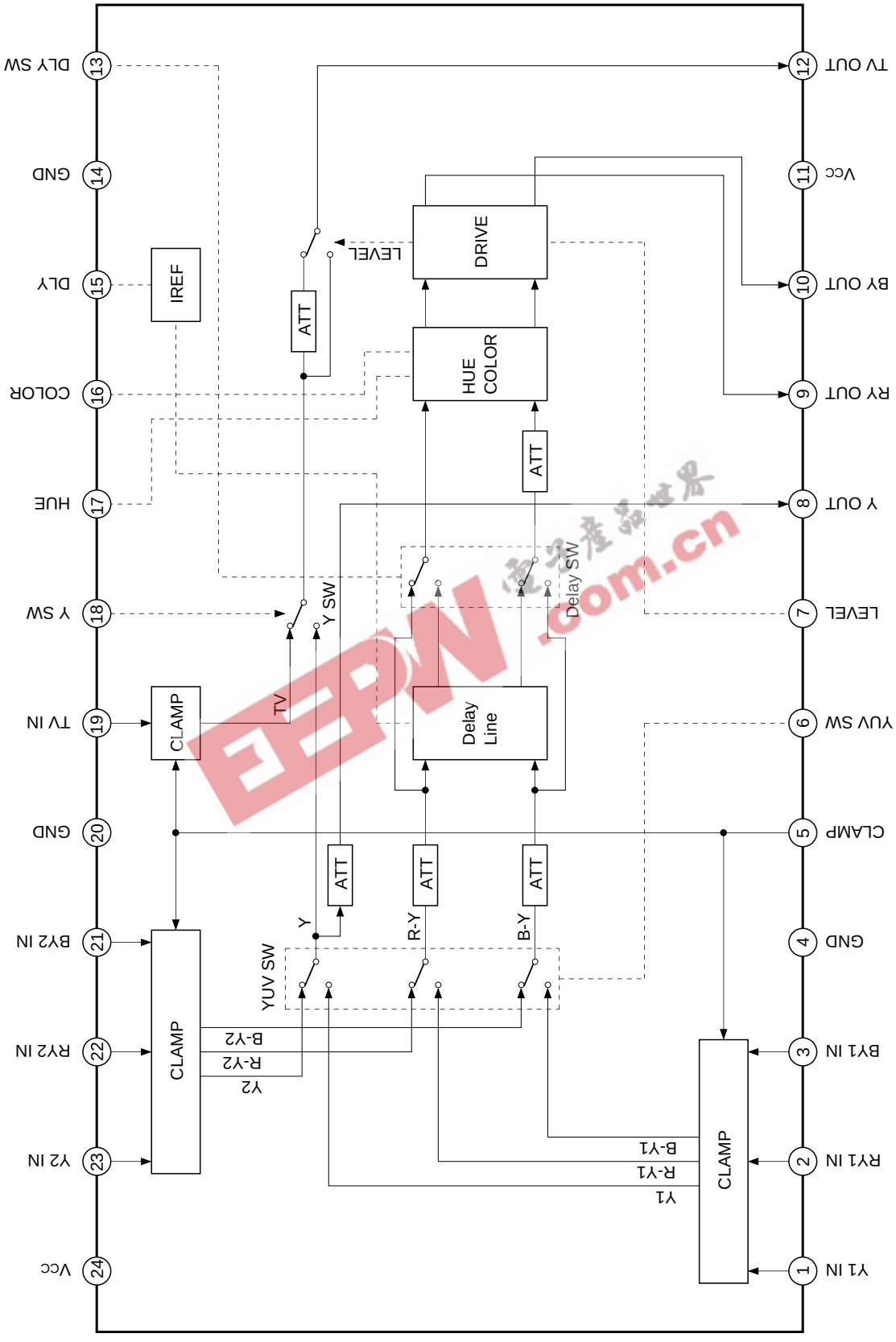
Color TVs

Structure

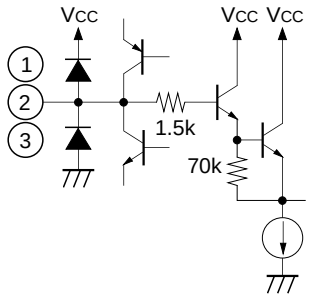
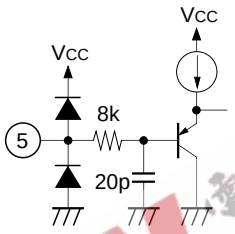
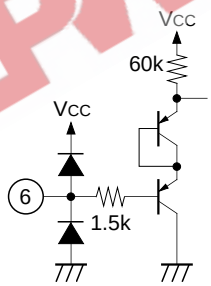
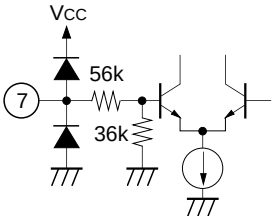
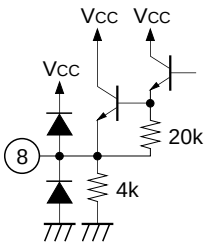
Bipolar silicon monolithic IC

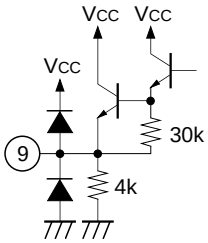
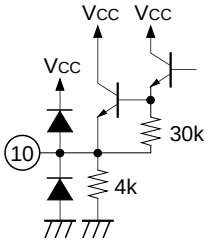
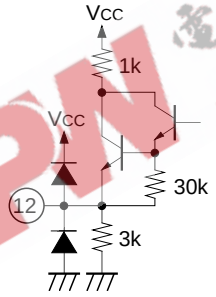
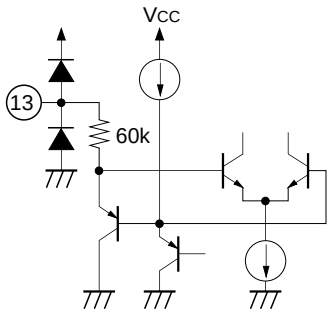
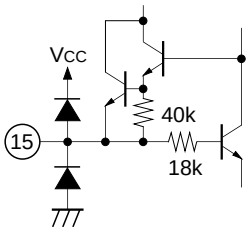
E96X26C1Y-PS

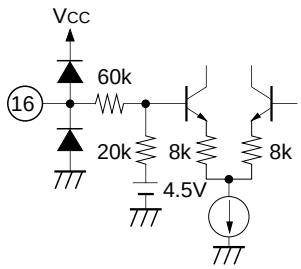
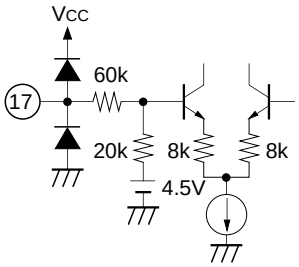
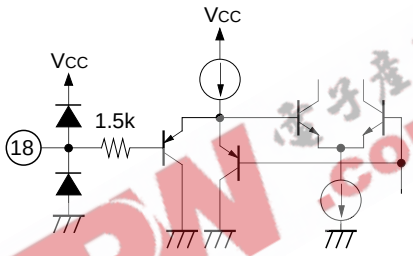
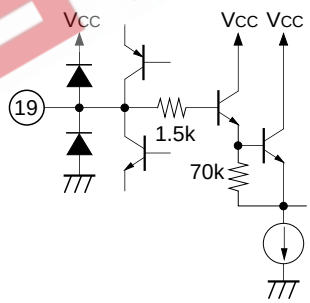
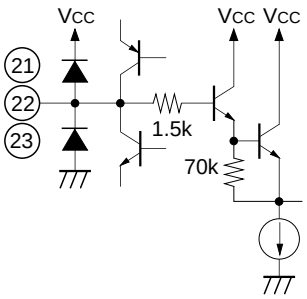
Block Diagram



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 2 3	Y1 IN RY1 IN BY1 IN			Y1, R-Y1 and B-Y1 signal inputs. Input the signals via capacitors.
4 14 20	GND			GND.
5	CLAMP			Clamp pulse (positive polarity) input. VILMAX = 2.5V VIHMIN = 3.5V
6	YUV SW			YUV SW control. YUV SW ≤ 0.4V → Y2 IN, RY2 IN, and BY2 IN signals selected. YUV SW ≥ 1.0V → Y1 IN, RY1 IN, and BY1 IN signals selected.
7	LEVEL			RY OUT, BY OUT and TV OUT output level control. VILMAX = 6.0V VIHMIN = 6.8V
8	Y OUT			Y signal output. Outputs the signals input to Pins 1 and 23 attenuated by –6dB.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	RY OUT			R-Y signal output.
10	BY OUT			B-Y signal output.
11 24	Vcc	9V		Power supply.
12	TV OUT			Y signal output.
13	DLY SW			Delay on/off switching signal input. DLY SW ≤ 1.4V → Delay off DLY SW ≥ 2.2V → Delay on
15	DLY			Delay line reference current setting. Connect to GND via a resistor. When 10kΩ is connected, the delay time is 600ns. Increasing the resistance value increases the delay time and vice versa.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	COLOR			Color control. Control is performed by applying a voltage of 0 to 9V.
17	HUE			Hue control. Control is performed by applying a voltage of 0 to 9V.
18	Y SW			Y SW control. DLY SW ≤ 1.4V → TV IN signal selected. DLY SW ≥ 2.2V → Y1 IN or Y2 IN signal selected (selected by YUV SW).
19	TV IN			Y signal input. Input the signal via a capacitor.
21 22 23	BY2 IN RY2 IN Y2 IN			Y2, R-Y2 and B-Y2 signal inputs. Input the signals via capacitors.

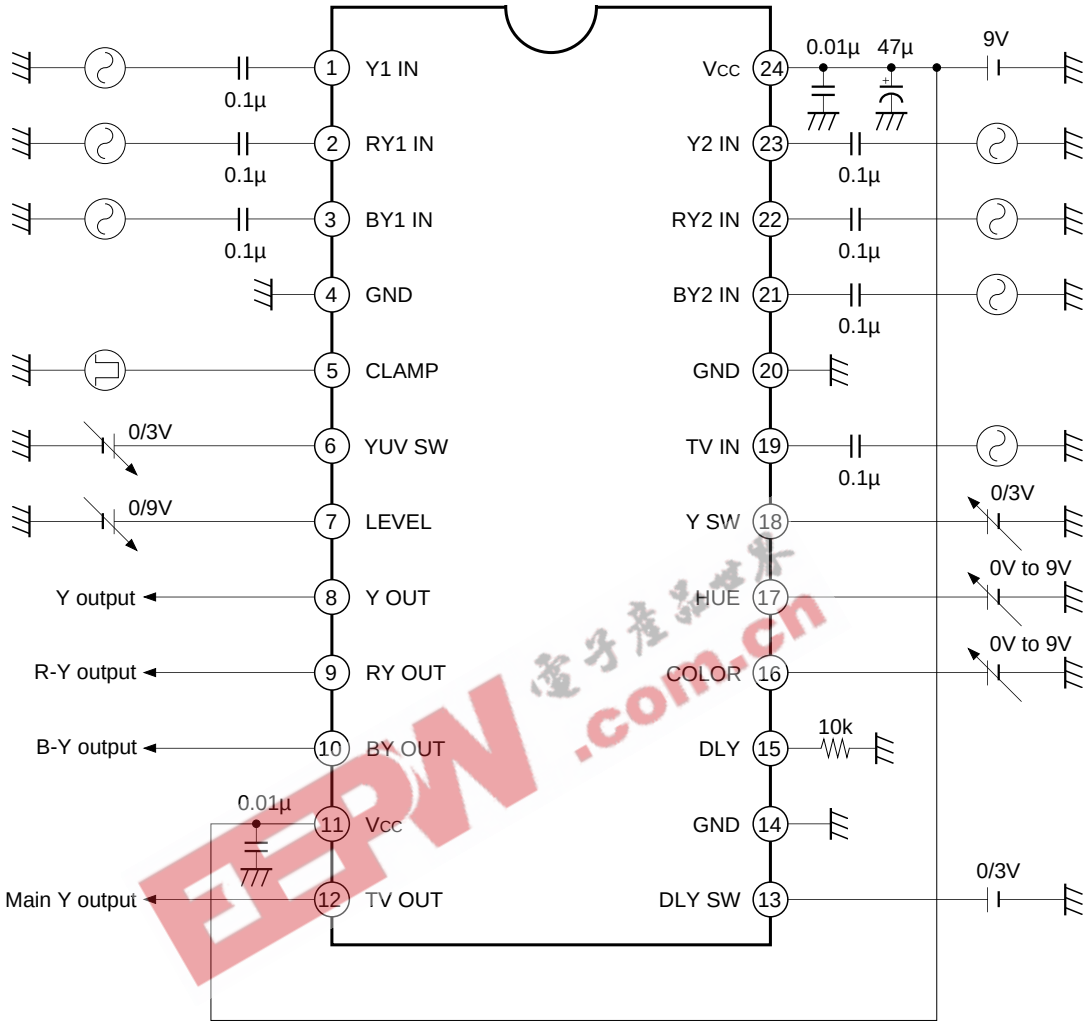
Electrical Characteristics

Setting conditions

- Ta = 25°C V_{CC} = 9V
- Set initially to: YUV SW = 0V, LEVEL = 0V, DLY SW = 0V, COLOR = 4.5V, HUE = 4.5V, Y SW = 0V. (when inputting the signals from Y2 IN, RY2 IN and BY2 IN)

No.	Item	Symbol	Measurement pin	Input signal	Measurement conditions and contents		Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}	11 24		Vcc pin inflow current		14	19	24	mA
2	TV OUT output gain	VTV1	12	Y: 1.4Vp-p R-Y, B-Y: 0.7Vp-p	I/O gain	Gain SW = Low MODE LEVEL ≤ 6V	–7.0	–6.2	–5.0	dB
3	TV OUT output gain	VTV2	12			Gain SW = High MODE LEVEL ≥ 6.8V	–1.0	0	1.0	dB
4	Y OUT output gain	VY	8		I/O gain		–7.0	–6.2	–5.0	dB
5	RY OUT output gain	VRY1	9		I/O gain	Gain SW = Low MODE LEVEL ≤ 6V	–7.0	–5.3	–4.0	dB
6	RY OUT output gain	VRY2	9			Gain SW = High MODE LEVEL ≥ 6.8V	–6.6	–4.7	–4.0	dB
7	BY OUT output gain	VBY1	10		I/O gain	Gain SW = Low MODE LEVEL ≤ 6V	–4.7	–3.1	–1.7	dB
8	BY OUT output gain	VBY2	10			Gain SW = High MODE LEVEL ≥ 6.8V	–4.3	–2.3	–1.3	dB
9	Color variable range 1	Cmax.	9		Set the output when COLOR = 4.5V to 0dB and measure the output when COLOR = 9V.		5.3	6.1	6.8	dB
10	Color variable range 2	Cmin.	9		Set the output when COLOR = 4.5V to 0dB and measure the output when COLOR = 0 V.			–40	–30	dB
11	Hue variable range 1	Hmax.	10	B-Y = 0.7Vp-p R-Y = 0.5Vp-p	$\tan^{-1} = \frac{\text{Output level during RY signal input only}}{\text{Output level during BY signal input only}}$ when HUE = 9V		40	48		Deg.
12	Hue variable range 2	Hmin.	10		$\tan^{-1} = \frac{\text{Output level during RY signal input only}}{\text{Output level during BY signal input only}}$ when HUE = 0V			–48	–40	Deg.
13	RY OUT Delay	RYDLY	9	0.7Vp-p	DLY SW = 3V. Measure the I/O delay.		530	600	680	ns
14	BY OUT Delay	BYDLY	10		DLY SW = 3V. Measure the I/O delay.		530	600	680	ns
15	Y OUT frequency response	fY	8	Y signal 1.4Vp-p 200kHz, 5MHz	Y SW = 3V. Measure the 200kHz gain with respect to 5MHz.		–1.0	0	1.0	dB
16	RY OUT frequency response	fRY	9				–6.0	–3.5	0	dB
17	BY OUT frequency response	fBY	10	R-Y and B-Y signal 1.4Vp-p 200kHz, 5MHz			–8.0	–5.0	–1.0	dB
18	TV OUT frequency response	fTV	12				–1.0	0	1.0	dB

Electrical Characteristics Measurement Circuit



* When performing measurements with signals input from Y1 IN, RY1 IN and BY1 IN: YUV SW = 3V
When performing measurements with signals input from Y2 IN, RY2 IN and BY2 IN: YUV SW = 0V

Description of Operation

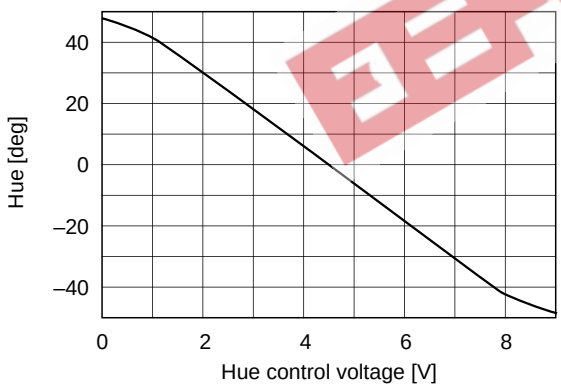
The Y, R-Y and B-Y signals input from Pins 1, 2, 3, 21, 22 and 23 are clamped by the clamp circuit and sent to the YUV SW circuit. The Y signal input from Pin 19 is clamped by the clamp circuit and then sent to the Y SW circuit.

The YUV SW circuit receives the switching signal from Pin 6 and selects either the signals from Pins 1, 2 and 3 or from Pins 21, 22 and 23. The R-Y and B-Y signals output from the YUV SW circuit are attenuated and sent to the delay line and delay switch circuits. The delay time at the delay line circuit can be set as desired in the range of 500 to 700ns according to the resistance value connected between Pin 15 and GND. After passing through the delay line circuit, the signals are sent to the delay switch circuit where the Pin 13 control voltage is received and delay on/off switching is performed. The signals output from the delay switch circuit are input to the base band hue and color control circuits where the Pins 16 and 17 control voltages are received and hue and color control is performed. Then, the signals are amplified by the drive circuit and output from Pins 9 and 10. The drive circuit gain can be switched between two values according to the voltage applied to Pin 7. Two types of Y signals, 0dB and –6dB with respect to the input level, are output from the YUV SW circuit. The 0dB signal is sent as is to the Y SW circuit, and the –6dB signal is output from Pin 8.

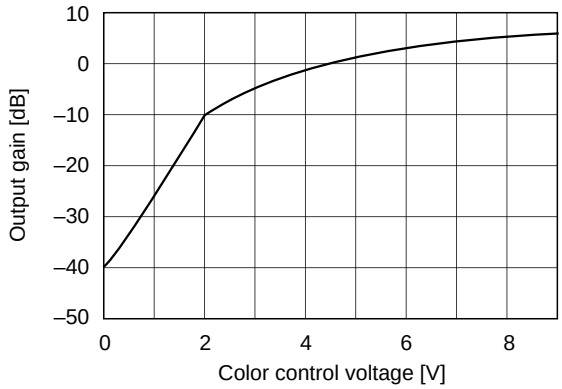
The Y SW circuit receives the switching signal from Pin 18 and selects the Pin 19 signal and either the Pin 1 or Pin 23 signal selected by YUV SW. Two types of Y signals, an unadjusted signal and a signal attenuated by –6dB, are output from the Y SW circuit. These signals are sent to the level switch circuit where one of them is selected according to the voltage applied to Pin 7 and output from Pin 12.

Curve Data

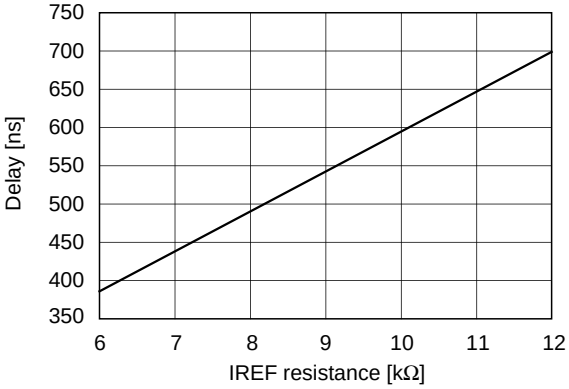
Hue



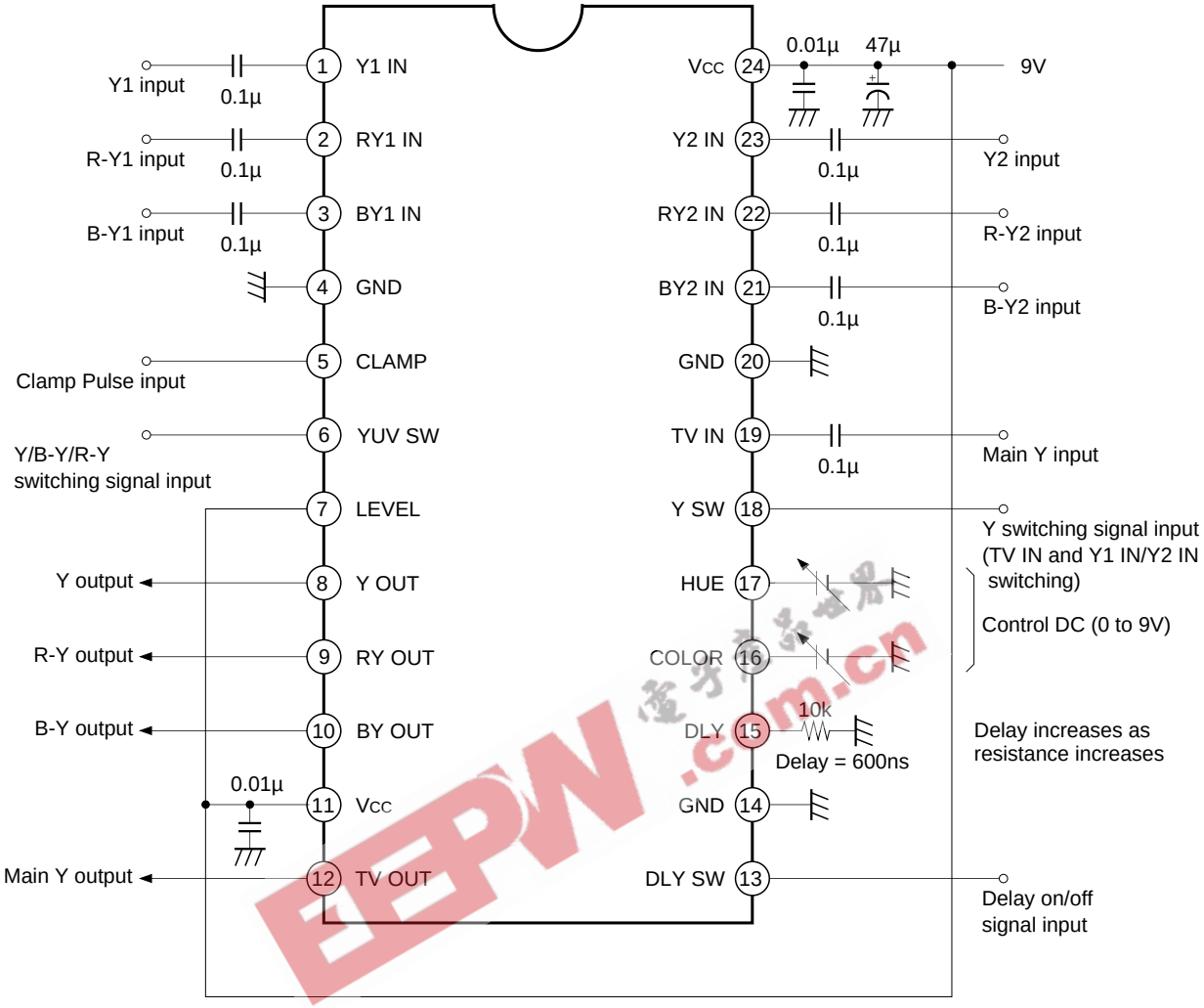
Color



I/O delay



Application Circuit



Pin 7 (Pins 9, 10 and 12 output level switching)

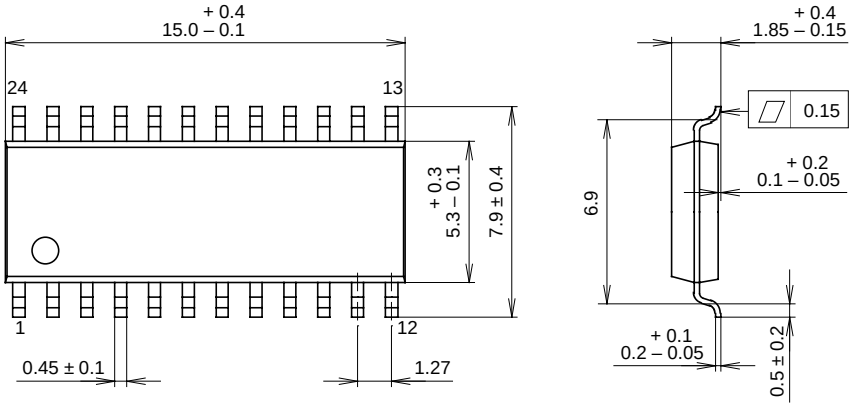
9V = Output High MODE [RYOUT: –2.3dB (Typ.)/BYOUT: –4.7dB (Typ.)]

0V = Output Low MODE [RYOUT: –3.1dB (Typ.)/BYOUT: –5.3dB (Typ.)]

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

24PIN SOP (PLASTIC)



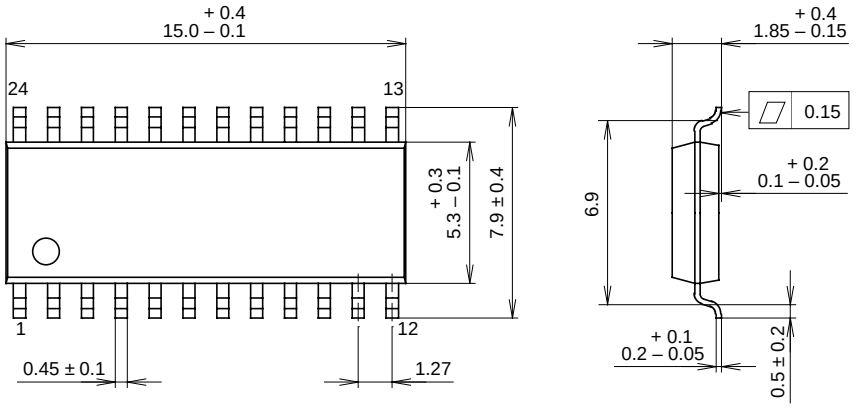
SONY CODE	SOP-24P-L01
EIAJ CODE	*SOP024-P-0300-A
JEDEC CODE	

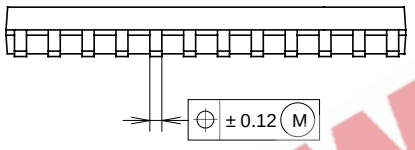
PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g

Package Outline Unit: mm

24PIN SOP (PLASTIC)





SONY CODE	SOP-24P-L01
EIAJ CODE	*SOP024-P-0300-A
JEDEC CODE	

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm