SONY

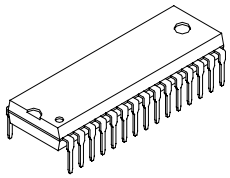
CXA2174S

US Audio Multiplexing Decoder

Description

The CXA2174S is an IC designed as a decoder for the Zenith TV Multi-channel System and also corresponds with I²C BUS. Functions include stereo demodulation, SAP (Separate Audio Program) demodulation, dbx noise reduction and sound processor. Various kinds of filters are built-in this IC. Adjustment, mode control and sound processor control are all executed through I²C BUS.

30 pin SDIP (Plastic)



Features

- Alignment-free VCO and filter
- Audio multiplexing decoder
  dbx noise reduction decoder
  sound processor
  — One external input
  — Volume control
  are all included in a single chip. Almost any sort of signal processing is possible through this IC.
- Input level, separation adjustments and each mode control are possible through I²C bus.

Applications

TV, VCR and other decoding systems for US audio multiplexing TV broadcasting

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

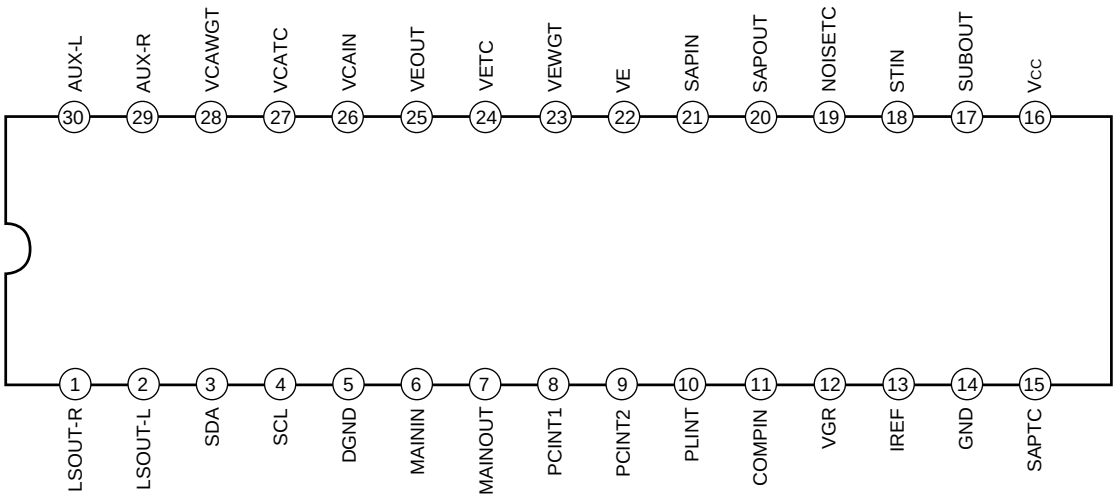
• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.35	W

Range of Operating Supply Voltage

9 ± 0.5 V

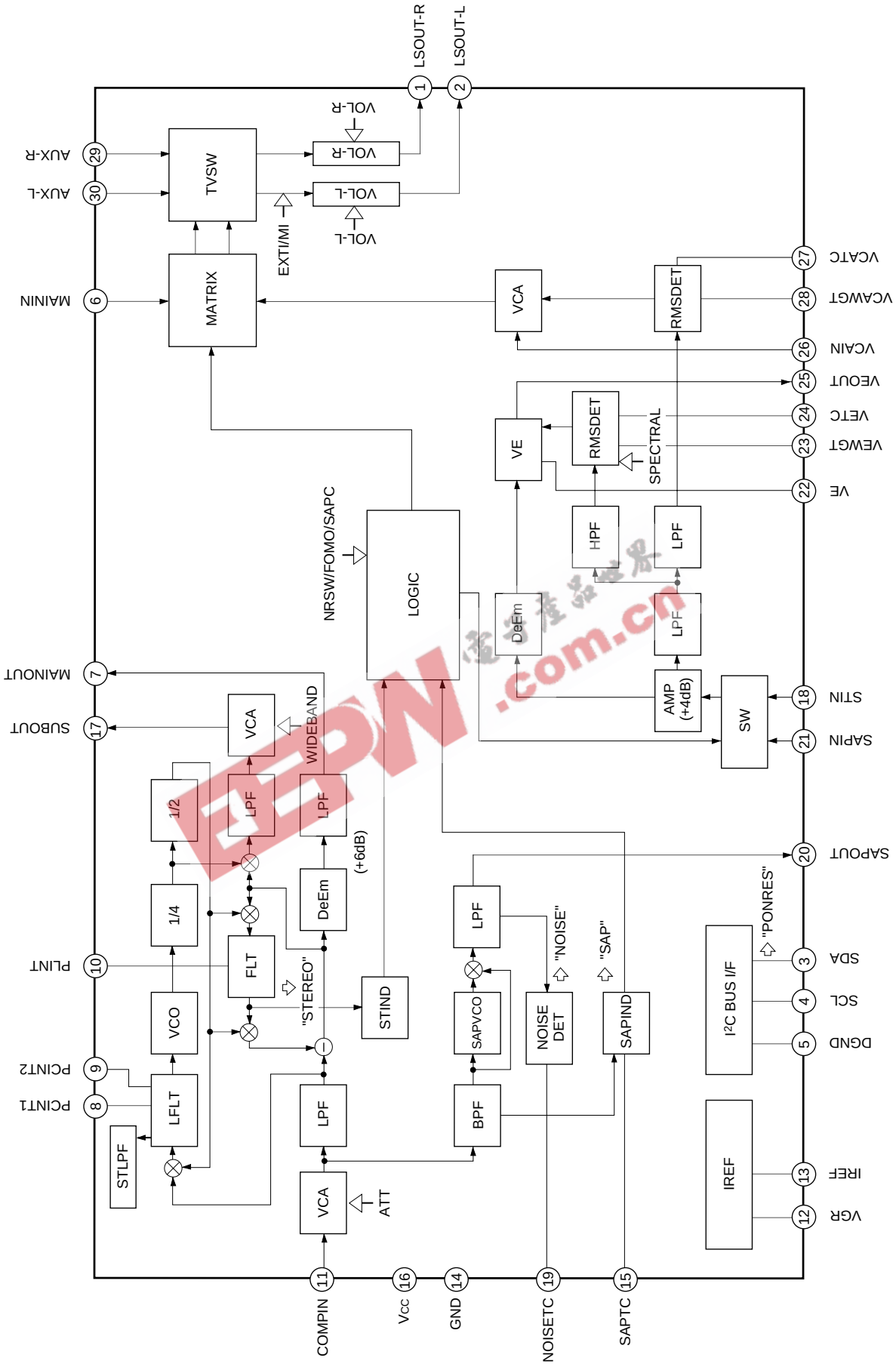
* A license of the dbx-TV noise reduction system is required for the use of this device.

Pin Configuration (Top View)

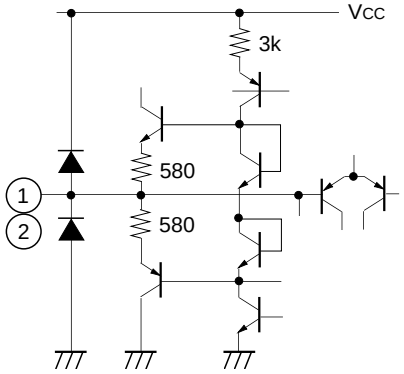
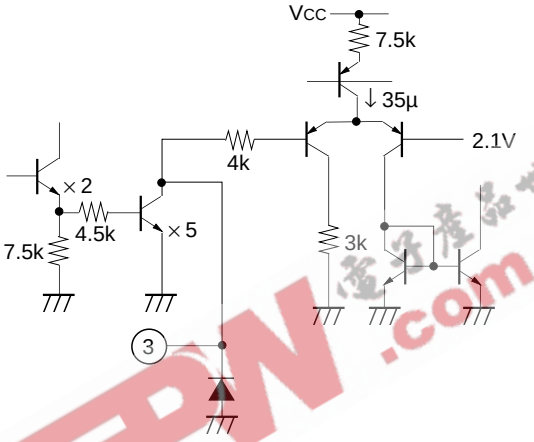
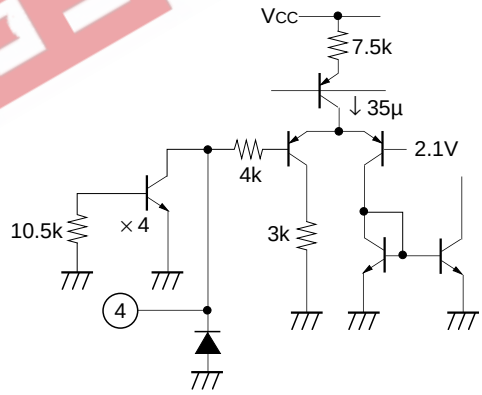
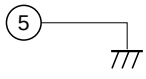


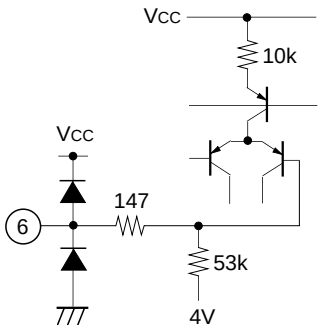
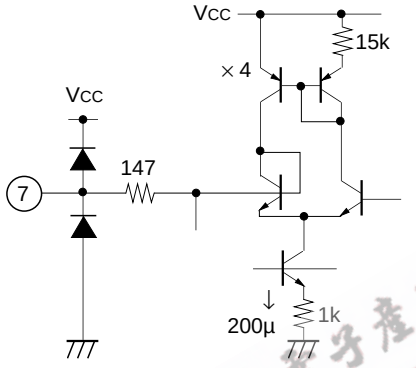
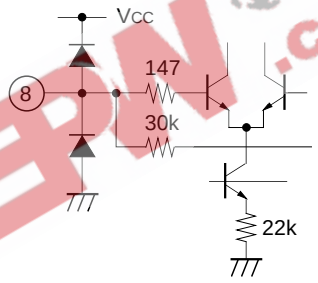
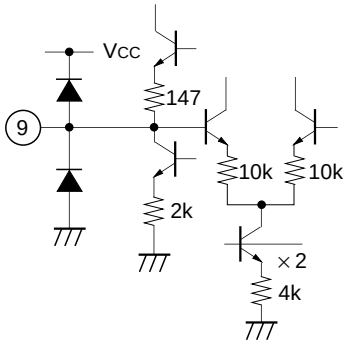
E00815-PS

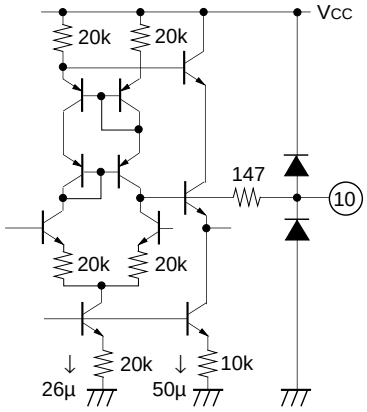
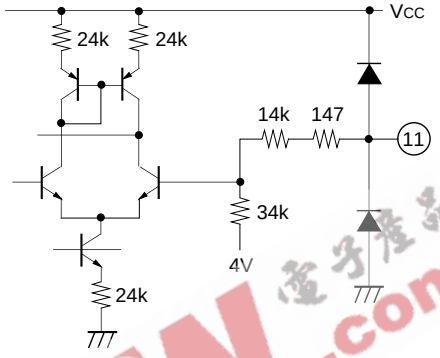
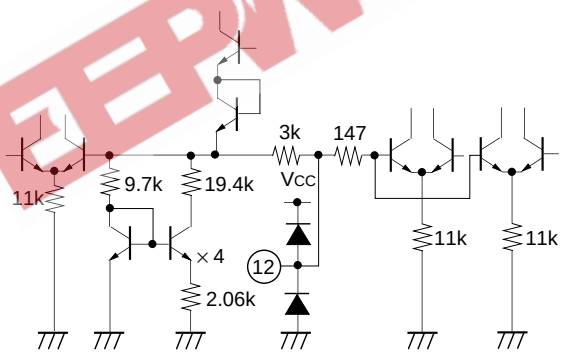
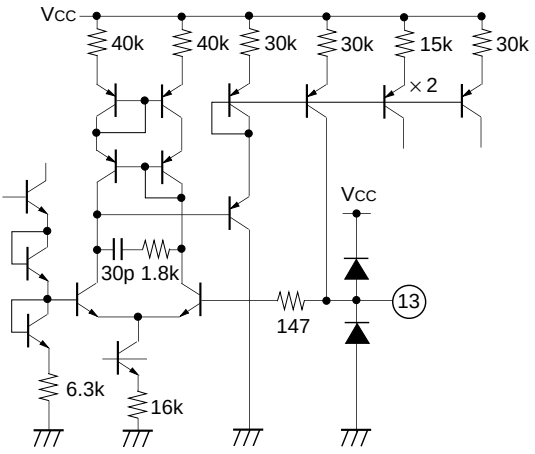
Block Diagram

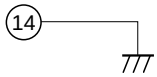
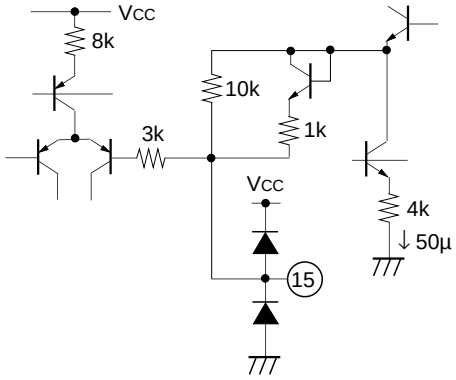
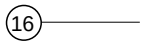
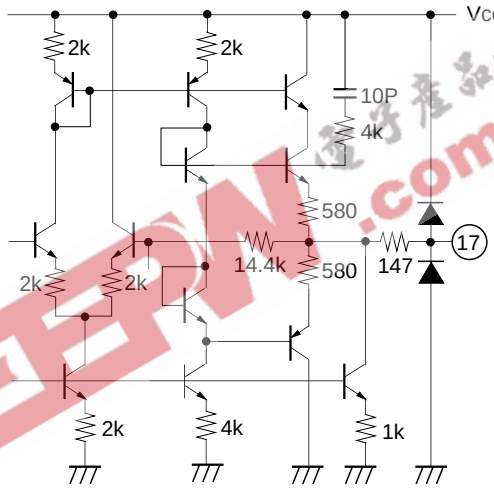
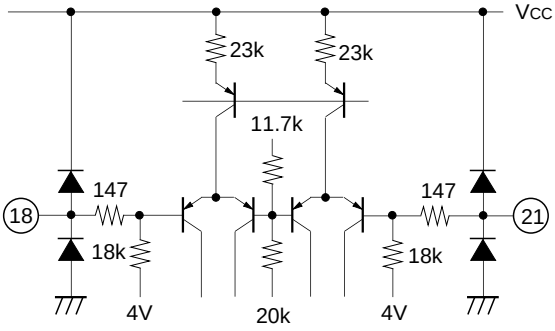


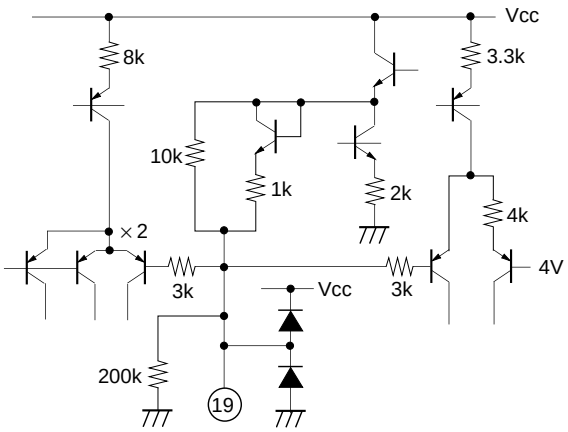
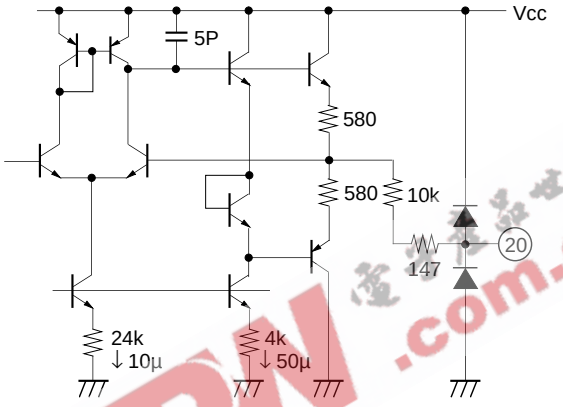
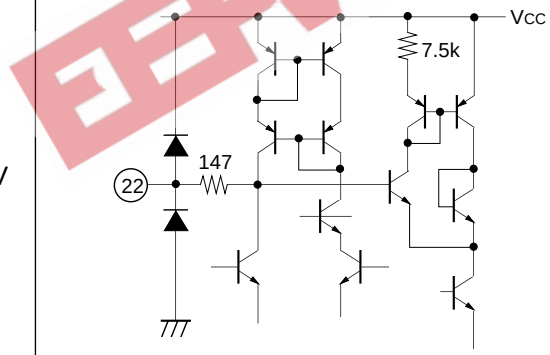
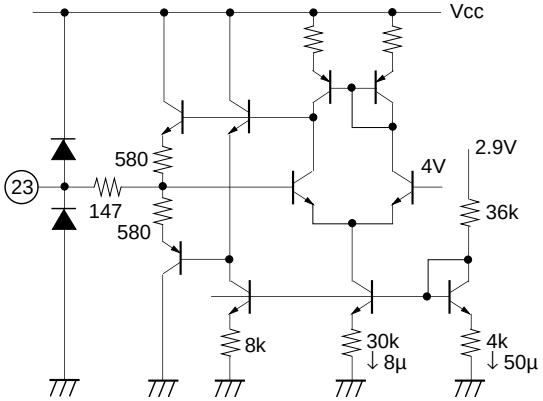
Pin Description (Ta = 25°C, V_{CC} = 9V)

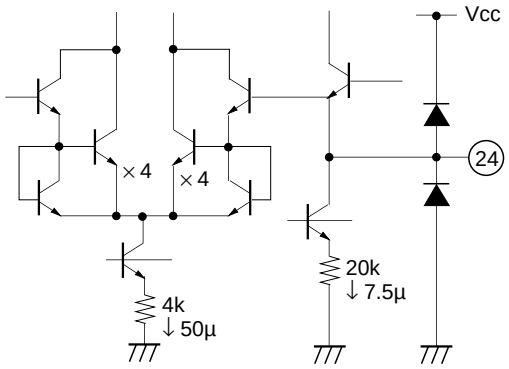
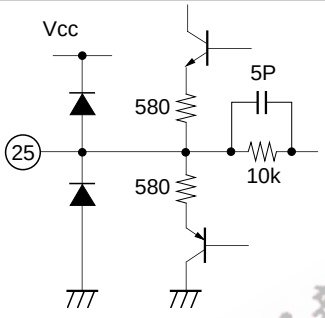
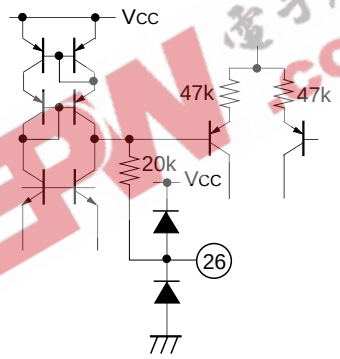
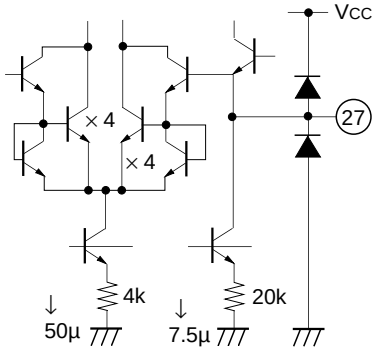
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	LSOUT-R	4.0V		LSOUT right channel output pin.
2	LSOUT-L	4.0V		LSOUT left channel output pin.
3	SDA	—		Serial data I/O pin. V_{IH} > 3.0V V_{IL} < 1.5V
4	SCL	—		Serial clock input pin. V_{IH} > 3.0V V_{IL} < 1.5V
5	DGND	—		Digital block GND.

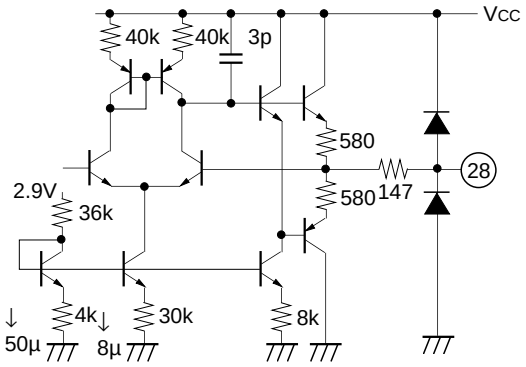
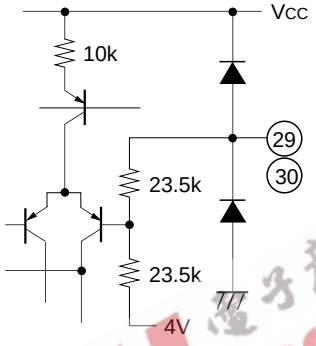
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	MAININ	4.0V		Input the (L + R) signal from MAINOUT (Pin 7).
7	MAINOUT	4.0V		(L + R) signal output pin.
8	PCINT1	4.0V		Stereo block PLL loop filter integrating pin.
9	PCINT2	4.0V		

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
10	PLINT	5.1V		Pilot cancel circuit loop filter integrating pin. (Connect a 1µF capacitor between this pin and GND.)
11	COMPIN	4.0V		Audio multiplexing signal input pin.
12	VGR	1.3V		Band gap reference output pin. (Connect a 10µF capacitor between this pin and GND.)
13	IREF	1.3V		Set the filter and VCO reference current. The reference current is adjusted with the BUS DATA based on the current which flows to this pin. (Connect a 62kΩ (±1%) resistor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	GND	—		Analog block GND.
15	SAPTC	4.5V		Set the time constant for the SAP carrier detection circuit. (Connect a 4.7µF capacitor between this pin and GND.)
16	Vcc	—		Supply voltage pin.
17	SUBOUT	4.0V		(L–R) signal output pin.
18	STIN	4.0V		Input the (L-R) signal from SUBOUT (Pin 17).
21	SAPIN	4.0V		Input the (SAP) signal from SAPOUT (Pin 20).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
19	NOISETC	3.0V		Set the time constant for the noise detection circuit. (Connect a 4.7µF capacitor between this pin and GND.)
20	SAPOUT	4.0V		SAP FM detector output pin.
22	VE	4.0V		Variable de-emphasis integrating pin. (Connect a 2700pF capacitor and a 3.3kΩ resistor in series between this pin and GND.)
23	VEWGT	4.0V		Weight the variable de-emphasis control effective value detection circuit. (Connect a 0.047µF capacitor and a 3kΩ resistor in series between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	VETC	1.7V		Determine the restoration time constant of the variable de-rmphasis control effective value detection circuit. (the specified restoration time constant can be obtained by connecting a 3.3µF capacitor between this pin and GND.)
25	VEOUT	4.0V		Variable de-emphasis output pin. (Connect a 4.7µF non-polar capacitor between Pins 25 and 26.)
26	VCAIN	4.0V		VCA input pin. Input the variable de-emphasis output signal from Pin 25 via a coupling capacitor.
27	VCATC	1.7V		Determine the restoration time constant of the VCA control effective value detection circuit. (the specified restoration time constant can be obtained by connecting a 10µF capacitor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	VCAWGT	4.0V		Weight the VCA control effective value detection circuit. (Connect a 1µF capacitor and a 3.9kΩ resistor in series between this pin and GND.)
29	AUX-R	4.0V		Right channel external input pin.
30	AUX-L	4.0V		Left channel external input pin.

Electrical Characteristics

COMPIN input level (100% modulation level)

Main (L + R) (Pre-Emphasis: OFF) = 245mVrms
SUB (L – R) (dbx-TV: OFF) = 490mVrms
Pilot = 49mVrms
SAP Carrier = 147mVrms
f_H = 15.734kHz

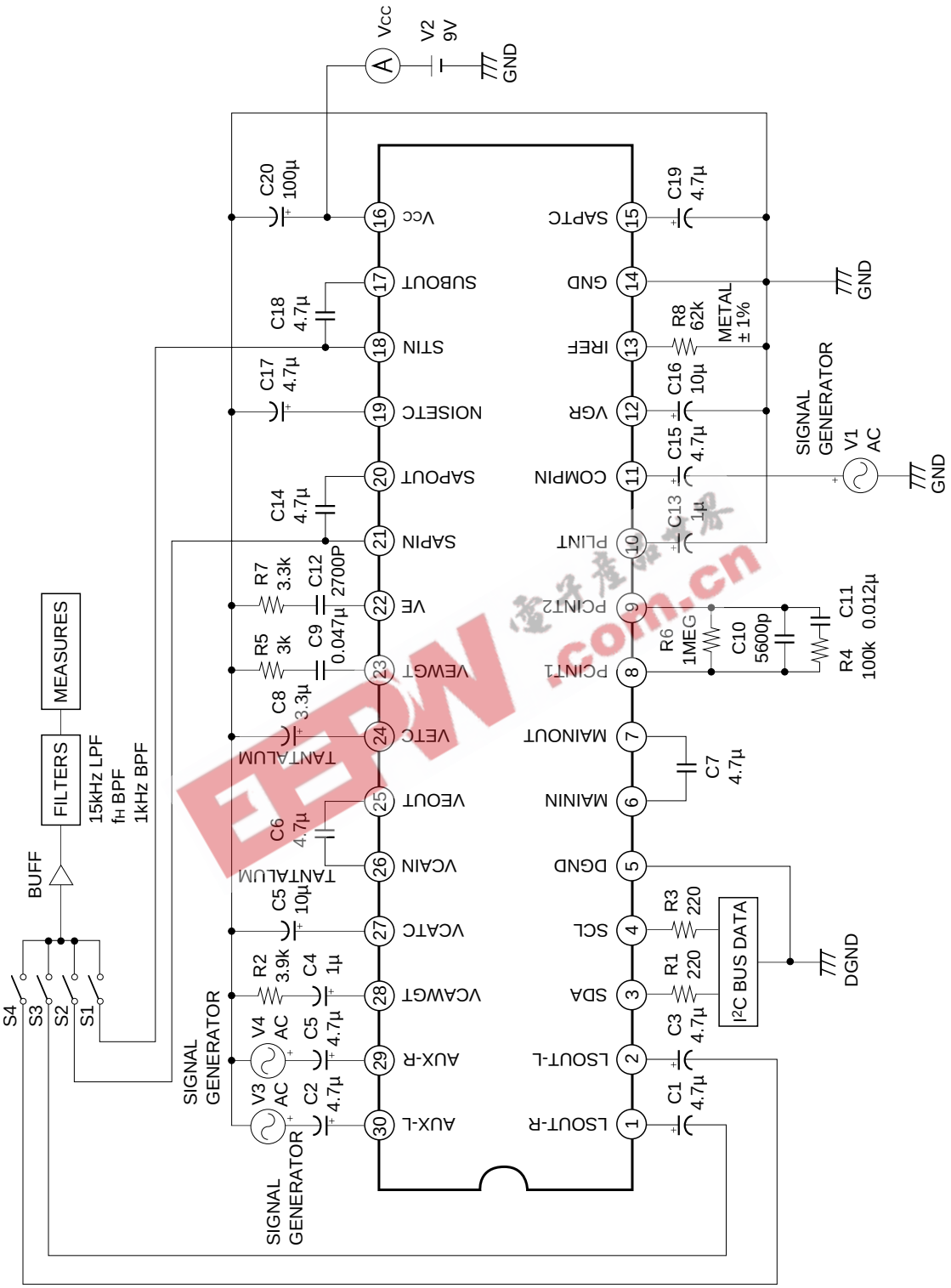
(Ta = 25°C, Vcc = 9V)

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
1	Current consumption	Icc		—	No signal				23	32	43	mA
2	Main output level	Vmain	MONO	11	Mono 1kHz 100% mod. Pre-em. ON			1/2	440	490	540	mVrms
3	Main de-emphasis frequency response	FCdeem	MONO	11	Mono 5kHz 30% mod. Pre-em. ON	20 log ('5k'/'1k')		1/2	–1.2	0	1.0	dB
4	Main LPF frequency response	FCmain	MONO	11	Mono 12kHz 30% mod. Pre-em. ON	20 log ('12k'/'1k')		1/2	–3.0	–1.0	1.0	dB
5	Main distortion	THDm	MONO	11	Mono 1kHz 100% mod. Pre-em. ON		15kLPF	1/2	—	0.1	0.5	%
6	Main overload distortion	THDmmax	MONO	11	Mono 1kHz 200% mod. Pre-em. ON		15kLPF	1/2	—	0.15	0.5	%
7	Main S/N	SNmain	MONO	11	Mono 1kHz, Pre-em. ON	20 log ('100%'/'0%')	15kLPF	1/2	61	69	—	dB
8	Sub output level	Vsub	ST	11	SUB (L-R) 1kHz, 100% mod., NR OFF			17	150	190	230	mVrms
9	Sub LPF frequency response	FCsub	ST	11	SUB (L-R) 12kHz, 30% mod., NR OFF	20 log ('12k'/'1k')		17	–3.0	–0.5	1.0	dB
10	Sub distortion	THDsub	ST	11	SUB (L-R) 1kHz, 100% mod., NR OFF		15kLPF	17	—	0.1	1.0	%
11	Sub overload distortion	THDsmax	ST	11	SUB (L-R) 1kHz, 200% mod., NR OFF		15kLPF	17	—	0.2	2.0	%
12	Sub S/N	SNsub	ST	11	SUB (L-R) 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	17	56	64	—	dB
13	Crosstalk Stereo → SAP	CTst	SAP	11	ST-L (R) 1kHz, 100% mod., NR ON, SAP Carrier (5f_H)	20 log ('NRSW = 0'/ 'NRSW = 1')	1kBPF	2	60	70	—	dB
14	Cross talk SAP → Stereo	CTsap	ST	11	SAP 1kHz 100% mod. NR ON, PILOT (f_H)	20 log ('NRSW = 1'/'NRSW = 0')	1kBPF	2	60	70	—	dB

(Ta = 25°C, Vcc = 9V)

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
15	Stereo ON level	THst	ST	11	Change PILOT (f_H) Level	0dB = 49mVrms		BUS RETURN	–9.0	–6.0	–3.0	dB
16	Stereo ON/OFF hysteresis	HYst				20 log ('on level '/'off level')			2.0	6.0	10.0	dB
17	SAP output level	Vsap	SAP	11	SAP 1kHz 100% mod. NR OFF			20	130	160	190	mVrms
18	SAP LPF frequency response	FCsap	SAP	11	SAP 10kHz 30% mod. NR OFF	20 log ('10k'/'1k')		20	–3.0	0	2.5	dB
19	SAP distortion	THDsap	SAP	11	SAP 1kHz 100% mod. NR OFF		15kLPF	20	—	2.5	6.0	%
20	SAP S/N	SNsap	SAP	11	SAP 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	20	46	55	—	dB
21	SAP ON level	THsap	SAP	11	Change SAP Carrier ($5f_H$) Level	0dB = 147mVrms		BUS RETURN	–12.0	–9.0	–6.5	dB
22	SAP ON/OFF hysteresis	HYsap				20 log ('on level' /'off level')			2.0	4.0	6.0	dB
23	ST separation 1 L → R	STLsep1	ST	11	ST-L 300Hz 30% mod. NR ON		15kLPF	1/2	23	35	—	dB
24	ST separation 1 R → L	STRsep1	ST	11	ST-R 300Hz 30% mod. NR ON		15kLPF	1/2	23	35	—	dB
25	ST separation 2 L → R	STLsep2	ST	11	ST-L 3kHz 30% mod. NR ON		15kLPF	1/2	23	35	—	dB
26	ST separation 2 R → L	STRsep2	ST	11	ST-R 3kHz 30% mod. NR ON		15kLPF	1/2	23	35	—	dB
27	LSOUT output level	Vls	EXT	30/29	Sine wave 1kHz 490mVrms	EXT1 = '1'		1/2	440	490	540	mVrms
28	LSOUT mute attenuation	MUls	EXT	30/29	Sine wave 1kHz 490mVrms	EXT1 = '1' M1 = '0'	1kBPF	1/2	—	–90	–80	dB
29	LSOUT distortion	THDls	EXT	30/29	Sine wave 1kHz 490mVrms	EXT1 = '1'	15kLPF	1/2	—	0.01	0.3	%
30	LSOUT overload distortion	THDlsmax	EXT	30/29	Sine wave 1kHz 2Vrms	EXT1 = '1'	15kLPF	1/2	—	0.03	0.3	%
31	LSOUT S/N	SNls	EXT	30/29	Sine wave 1kHz 490mVrms	EXT1 = '1'	15kLPF	1/2	80	88	—	dB
32	LSOUT volume maximum attenuation	VOLmin	EXT	30/29	Sine wave 1kHz 490mVrms	EXT1 = '1' VOL-L = '0' VOL-R = '0'	1kBPF	1/2	—	–90	–80	dB

Electrical Characteristics Measurement Circuit



Adjustment Method

1. ATT adjustment
   1) TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
   2) Input a 100Hz, 245mVrms sine wave signal to COMPIN and monitor the LSOUT-L output level. Then, adjust the “ATT” data for ATT adjustment so that the LSOUT-L output goes to the standard value (490mVrms).
   3) Adjustment range: ±20%
      Adjustment bits: 4 bits

2. Separation adjustment
   1) TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
   2) Set the unit to stereo mode and input the left channel only signal (modulation factor 30%, frequency 300Hz NR-ON) to COMPIN. At this time, adjust the “WIDEBAND” adjustment data to reduce LSOUT-R output to the minimum.
   3) Next, set the frequency only of the input signal to 3kHz and adjust the “SPECTRAL” adjustment data to reduce LSOUT-R output to the minimum.
   4) The adjustments in 2 and 3 above are performed to optimize the separation.
   5) “WIDEBAND” “SPECTRAL”
      Adjustment range: ±30% Adjustment range: ±15%
      Adjustment bits: 6 bits Adjustment bits: 6 bits

* Adjust this IC through Tuner and IF when this IC is mounted in the set.

Register Specifications

Slave address

SLAVE RECEIVER	SLAVE TRANSMITTER
84H (1000 0100)	85H (1000 0101)

Register table

SUB ADDRESS	DATA							
MSB LSB	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
****0000	*		TEST-DA	TEST1	ATT			
****0001	*		SPECTRAL					
****0010	*		WIDEBAND					
****0011	*		EXT1	*	NRSW	FOMO	SAPC	M1
****0100	*		VOL-L					
****0101	*		VOL-R					

* : don't care

Status Registers

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	—	—	—	—

Note) The micro computer reads both SAP and NOISE status and judges SAP discrimination.

Description of Registers

Control registers

Register	Number of bits	Classification*1	Standard setting	Contents
ATT	4	A	9	Input level adjustment
SPECTRAL	6	A	1F	Adjustment of stereo separation (3kHz)
WIDEBAND	6	A	1F	Adjustment of stereo separation (300Hz)
TEST-DA	1	T	0	DAC test mode
TEST1	1	T	0	Test mode
EXT1	1	U	0	Selection of TV mode or external input mode
NRSW	1	U	0	Selection of the output signal (Stereo mode, SAP mode)
FOMO	1	U	0	Forced MONO (Left channel only is MONO during SAP output.)
M1	1	U	1	Selection of LSOUT mute function ON/OFF (0: mute ON, 1: mute OFF)
SAPC	1	S	0	Selection SAP mode or L + R mode according to the presence of SAP brodecasting
VOL-L	1	U	3F	Left channel volume control
VOL-R	1	U	3F	Right channel volume control

*1 Classification U: User control
A: Adjustment
S: Proper to set
T: Test

Status registers

Register	Number of bits	Contents	
PONRES	1	POWER ON RESET detection;	1: RESET
STEREO	1	Stereo discrimination of the COMPIN input signal;	1: Stereo
SAP	1	SAP discrimination of the COMPIN input signal;	1: SAP
NOISE	1	Noise level discrimination of the SAP signal;	1: Noise

Description of Control Registers

ATT (4): Perform input level adjustment.
0 = Level min.
F = Level max.

SPECTRAL (6): Perform high frequency (fs = 3kHz) separation adjustment.
0 = Level max.
3F = Level min.

WIDEBAND (6): Perform low frequency (fs = 300Hz) separation adjustment.
0 = Level min.
3F = Level max.

TEST-DA (1): Set DAC output test mode.
0 = Normal mode
1 = DAC output test mode
In addition, the following output are present at Pin 2.
LSOUT-L (Pin 2): DA control DC level

TEST1 (1): Monitor SAPBPF and NRBPF output
0 = Normal mode
1 = SAPBPF, NRBPF output
In addition, the following outputs are present at Pins 1 and 2.
LSOUT-L (Pin 2): SAP BPF OUT
LSOUT-R (Pin 1): NR BPF OUT

EXT1 (1): Select TV mode or external input mode
0 = TV mode
1 = External input mode

NRSW (1): Select stereo mode or SAP mode
0 = Stereo mode
1 = SAP mode

FOMO (1): Select forced MONO mode
0 = Normal mode
1 = Forced MONO mode

M1 (1): Mute the LSOUT-L and LSOUT-R output.
0 = Mute ON
1 = Mute OFF

SAPC (1): Select the SAP signal output mode
When there is no SAP signal, the conditions for selecting SAP output are selected by SAPC.
0 = L + R output is selected
1 = SAP output is selected

VOL-L (6): LSOUT-L output signal level control
0 = Volume min.
3F = Volume max.
–1.25dB/STEP

VOL-R (6): LSOUT-R output signal level control
0 = Volume min.
3F = Volume max.
–1.25dB/STEP

Description of Mode Control

Mode control	SAPC = 0	SAPC = 1
NRSW	"Select dbx input and TV decoder output" Conditions: FOMO = 0 NRSW = 0 (MONO or ST output) • During ST input: left channel: L, right channel: R • During other input: left channel: L + R, right channel: L + R NRSW = 1 (SAP output) • When there is "SAP" during SAP discrimination – left channel: SAP, right channel: SAP • When there is "No SAP", output is the same as when NRSW = 0.	"Select dbx input and TV decoder output" Conditions: FOMO = 0 NRSW = 0 (MONO or ST output) As on the left NRSW = 1 (SAP output) • Regardless of the presence of SAP discrimination, dbx input: "SAP" left channel: SAP, right channel: SAP However, when there is no SAP, SAPOUT output is soft muted (–7dB)
FOMO	"Forced MONO" FOMO = 1 • During SAP output: left channel: L + R, right channel: SAP • During ST or MONO output: left channel: L + R, right channel: L + R	
SAPC	Change the selection conditions for "MONO or ST output" and "SAP output". SAPC = 0: Switch to SAP output when there is SAP discrimination. Do not switch to SAP output when there is no SAP discrimination. SAPC = 1: Switch to SAP output regardless of whether there is SAP discrimination.	
M1	"MUTE" M1 = 0: LSOUT output is muted.	

Decoder Output and Mode Control Table 1 (SAPC = 1)

Input signal mode	Mode detection			Mode control			dbx input	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC		Lch	Rch
MONO *1	0	0	0	0	*	1	MUTE	L + R	L + R
	0	0	0	1	0	1	SAP	SAP	SAP
	0	0	0	1	1	1	SAP	L + R	SAP
	0	*	1	0	*	1	MUTE	L + R	L + R
	0	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	*	1	1	1	1	(SAP)	L + R	(SAP)
STEREO *1	1	0	*	0	0	1	L – R	L	R
	1	0	*	0	1	1	MUTE	L + R	L + R
	1	1	1	0	0	1	L – R	L	R
	1	1	1	0	1	1	MUTE	L + R	L + R
	1	0	0	1	0	1	SAP	SAP	SAP
	1	0	0	1	1	1	SAP	L + R	SAP
	1	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	*	1	1	1	1	(SAP)	L + R	(SAP)
MONO & SAP	0	1	*	0	0	1	MUTE	L + R	L + R
	0	1	*	0	1	1	MUTE	L + R	L + R
	0	1	0	1	0	1	SAP	SAP	SAP
	0	1	0	1	1	1	SAP	L + R	SAP
	0	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	1	(SAP)	L + R	(SAP)
STEREO & SAP	1	1	*	0	0	1	L – R	L	R
	1	1	*	0	1	1	MUTE	L + R	L + R
	1	1	0	1	0	1	SAP	SAP	SAP
	1	1	0	1	1	1	SAP	L + R	SAP
	1	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	1	(SAP)	L + R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately –7dB).
The signal is soft muted when NOISE = 1.

* : Don't care.

*1 SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
Then microcomputer reads "NOISE" status from IC and decides whether SAP is outputted.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Decoder Output and Mode Control Table 2 (SAPC = 0)

Input signal mode	Mode detection			Mode control			dbx input	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC		Lch	Rch
MONO *1	0	0	*	*	*	0	MUTE	L + R	L + R
	0	1	1	0	0	0	MUTE	L + R	L + R
	0	1	1	0	1	0	MUTE	L + R	L + R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L + R	(SAP)
STEREO *1	1	0	*	0	0	0	L – R	L	R
	1	0	*	0	1	0	MUTE	L + R	L + R
	1	0	*	1	0	0	L – R	L	R
	1	0	*	1	1	0	MUTE	L + R	L + R
	1	1	1	0	0	0	L – R	L	R
	1	1	1	0	1	0	MUTE	L + R	L + R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L + R	(SAP)
MONO & SAP	0	1	0	0	0	0	MUTE	L + R	L + R
	0	1	0	0	1	0	MUTE	L + R	L + R
	0	1	0	1	0	0	SAP	SAP	SAP
	0	1	0	1	1	0	SAP	L + R	SAP
	0	1	1	0	0	0	MUTE	L + R	L + R
	0	1	1	0	1	0	MUTE	L + R	L + R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L + R	(SAP)
STEREO & SAP	1	1	0	0	0	0	L – R	L	R
	1	1	0	0	1	0	MUTE	L + R	L + R
	1	1	0	1	0	0	SAP	SAP	SAP
	1	1	0	1	1	0	SAP	L + R	SAP
	1	1	1	0	0	0	L – R	L	R
	1	1	1	0	1	0	MUTE	L + R	L + R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L + R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately –7dB).
The signal is soft muted when NOISE = 1.

* : Don't care.

*1 SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
Then microcomputer reads "NOISE" status from IC and decides whether SAP is outputted.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Description of Operation

The US audio multiplexing system possesses the base band spectrum shown in Fig. 1.

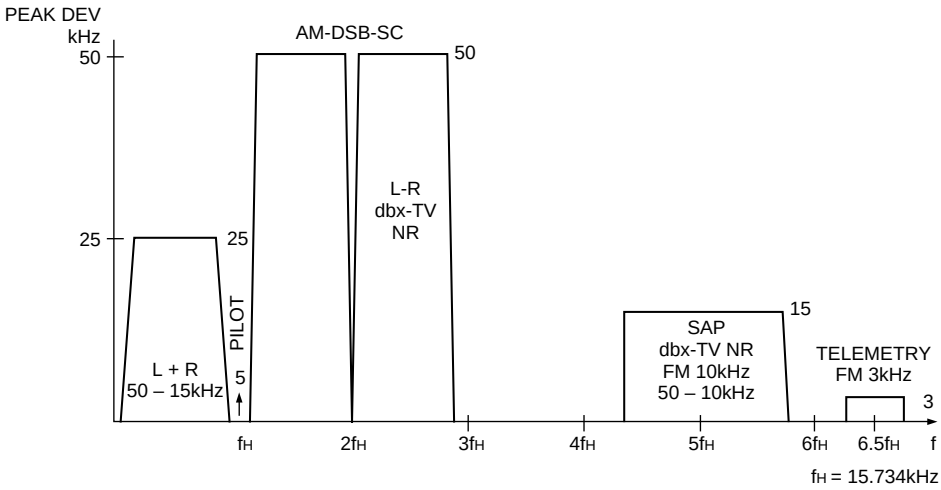


Fig. 1. Base band spectrum

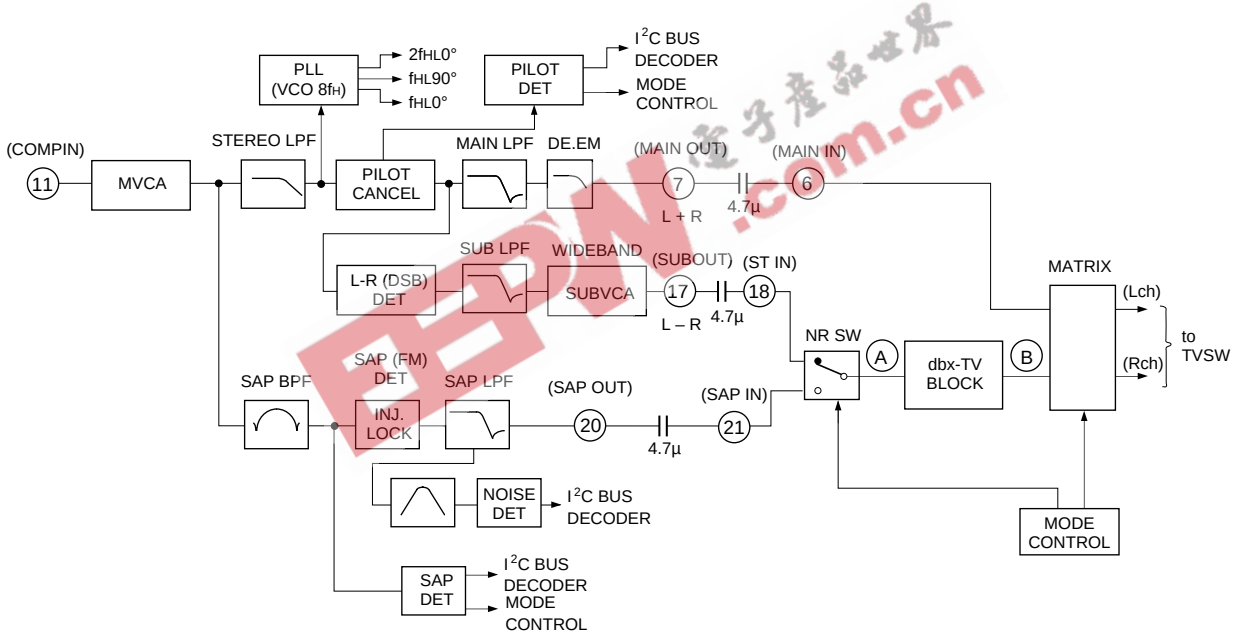


Fig. 2. Overall block diagram (See Fig. 3 for the dbx-TV block)

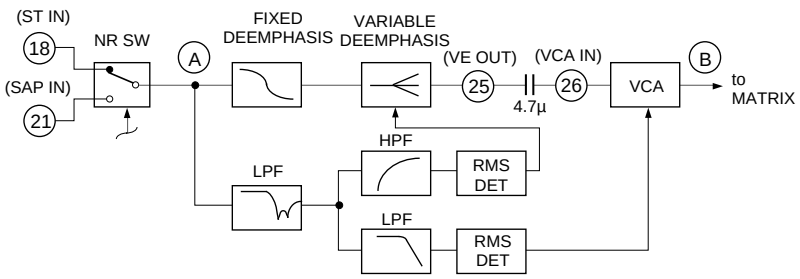


Fig 3. dbx-TV block

(1) L + R (MAIN)

After the audio multiplexing signal input from COMPIN (Pin 11) passes through MVCA, the SAP signal and telemetry signal are suppressed by STEREO LPF. Next, the pilot signals are canceled. Finally, the L – R signal and SAP signal are removed by MAIN LPF, and frequency characteristics are flattened (de-emphasized) and input to the matrix.

(2) L – R (SUB)

The L – R signal follows the same course as L + R before the pilot signal is canceled. L – R has no carrier signal, as it is a suppressed-carrier double-sideband amplitude modulated signal (DSB-AM modulated). For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for the demodulation of the L – R signal. In the last stage, the residual high frequency components are removed by SUB LPF and the L – R signal is input to the dbx-TV block via the NRSW circuit after passing through SUBVCA.

(3) SAP

SAP is an FM signal using $5f_H$ as a carrier as shown in the Fig. 1. First, the SAP signal only is extracted using SAP BPF. Then, this is subjected to FM detection. Finally, residual high frequency components are removed and frequency characteristics flattened using SAP LPF, and the SAP signal is input to the dbx-TV block via the NRSW circuit. When there is no SAP signal, the Pin 20 output is soft muted.

(4) Mode discrimination

Stereo discrimination is performed by detecting the pilot signal amplitude. SAP discrimination is performed by detecting the $5f_H$ carrier amplitude. NOISE discrimination is performed by detecting the noise near 25kHz after FM detection of SAP signal.

(5) dbx-TV block

Either the L – R signal or SAP signal input respectively from ST IN (Pin 18) or SAP IN (Pin 21) is selected by the mode control and input to the dbx-TV block.

The input signal then passes through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The signal output from the variable de-emphasis circuit passes through an external capacitor and is applied to VCA (voltage control amplifier). Finally, the VCA output is converted from a current to a voltage using an operational amplifier and then input to the matrix.

The variable de-emphasis circuit transmittance and VCA gain are respectively controlled by Each of effective value detection circuits. Each of the effective value detection circuits passes the input signal through a predetermined filter for weighting before the effective value of the weighted signal is detected to provide the control signal.

(6) Matrix, TVSW

The signals (L + R, L – R, SAP) input to “MATRIX” become the outputs for the ST-L, ST-R, MONO and SAP signals according to the mode control and whether there is ST / SAP discrimination.

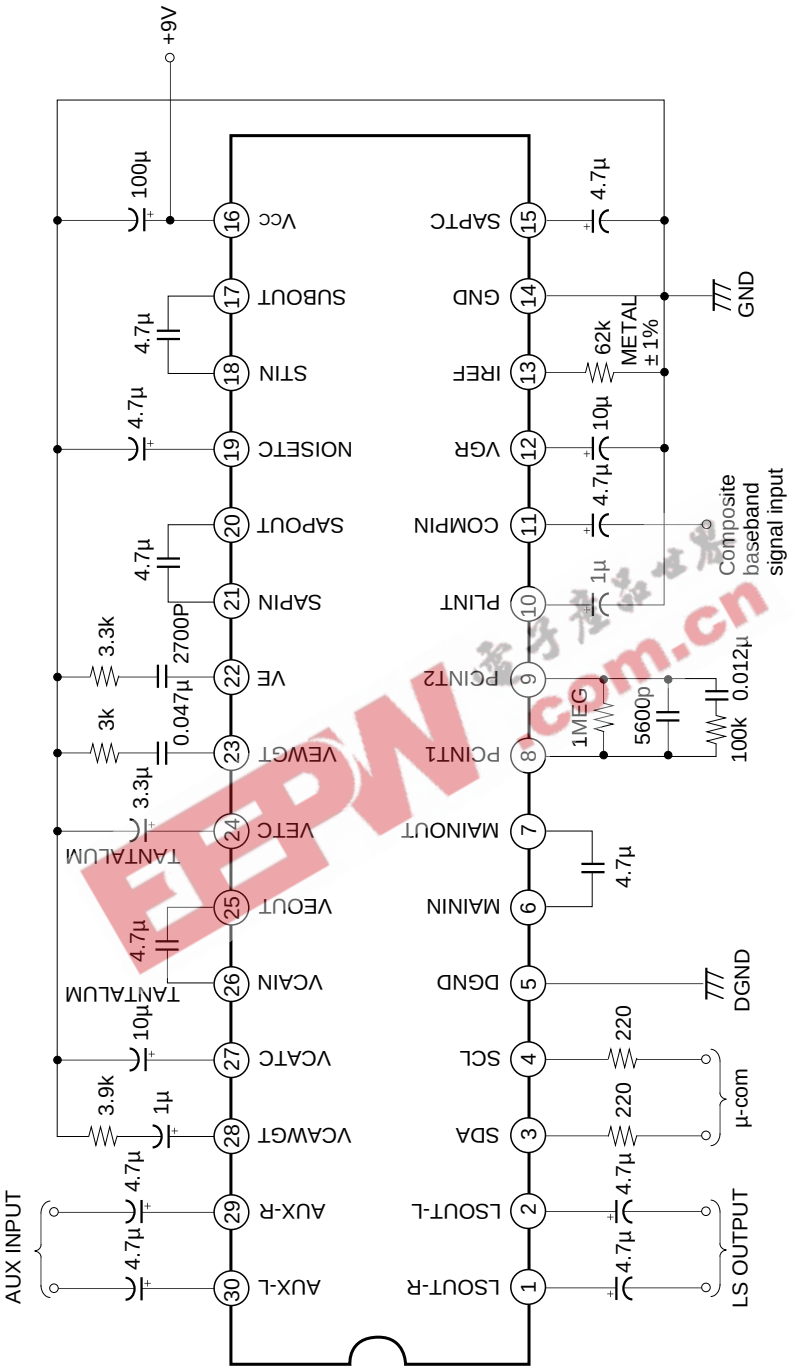
“TVSW” switches the “MATRIX” output signal and external input signal.

(7) Others

“MVCA” is a VCA which adjusts the input signal level to the standard level of this IC.

“Bias” supplies the reference voltage and reference current to the other blocks. The current flowing to the resistor connecting IREF (Pin 13) with GND become the reference current.

Application Circuit



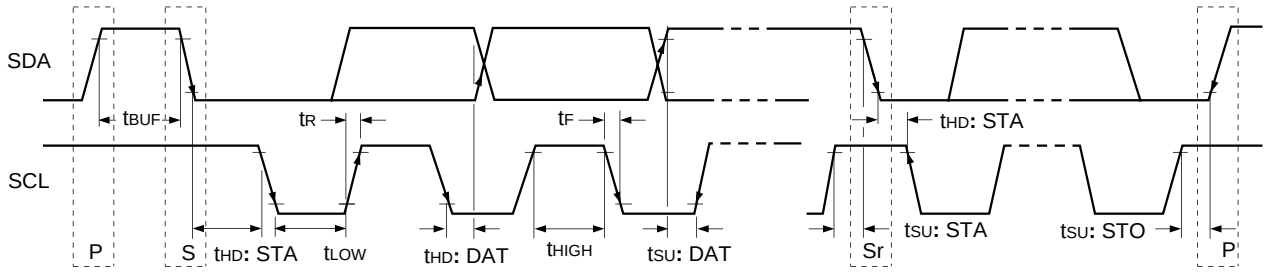
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

I²C BUS block items (SDA, SCL)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	
3	High level input current	I_{IH}	—	—	10	µA
4	Low level input current	I_{IL}	—	—	10	
5	Low level output voltage SDA (Pin 3) during 3mA inflow	V_{OL}	0	—	0.4	V
6	Maximum inflow current	I_{OL}	3	—	—	mA
7	Input capacitance	C_I	—	—	10	pF
8	Maximum clock frequency	f_{SCL}	0	—	100	kHz
9	Minimum waiting time for data change	t_{BUF}	4.7	—	—	µs
10	Minimum waiting time for start of data transfer	t_{HD}: STA	4.0	—	—	
11	Low level clock pulse width	t_{LOW}	4.7	—	—	
12	High level clock pulse width	t_{HIGH}	4.0	—	—	
13	Minimum waiting time for start preparation	t_{SU}: STA	4.7	—	—	
14	Minimum data hold time	t_{HD}: DAT	0	—	—	
15	Minimum data preparation time	t_{SU}: DAT	250	—	—	ns
16	Rise time	t_R	—	—	1	µs
17	Fall time	t_F	—	—	300	ns
18	Minimum waiting time for stop preparation	t_{SU}: STO	4.7	—	—	µs

I²C BUS load conditions: Pull-up resistor 4kΩ (Connect to +5V)
Load capacity 200pF (Connect to GND)

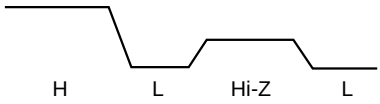
I²C BUS Control Signal



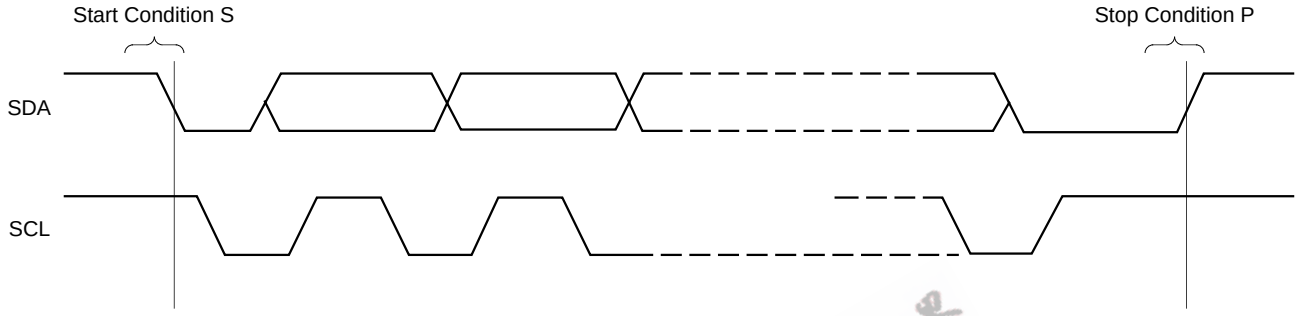
I²C BUS Signal

There are two I²C signals, SDA (Serial DATA) and SCL (Serial CLOCK) signals. SDA is a bidirectional signal.

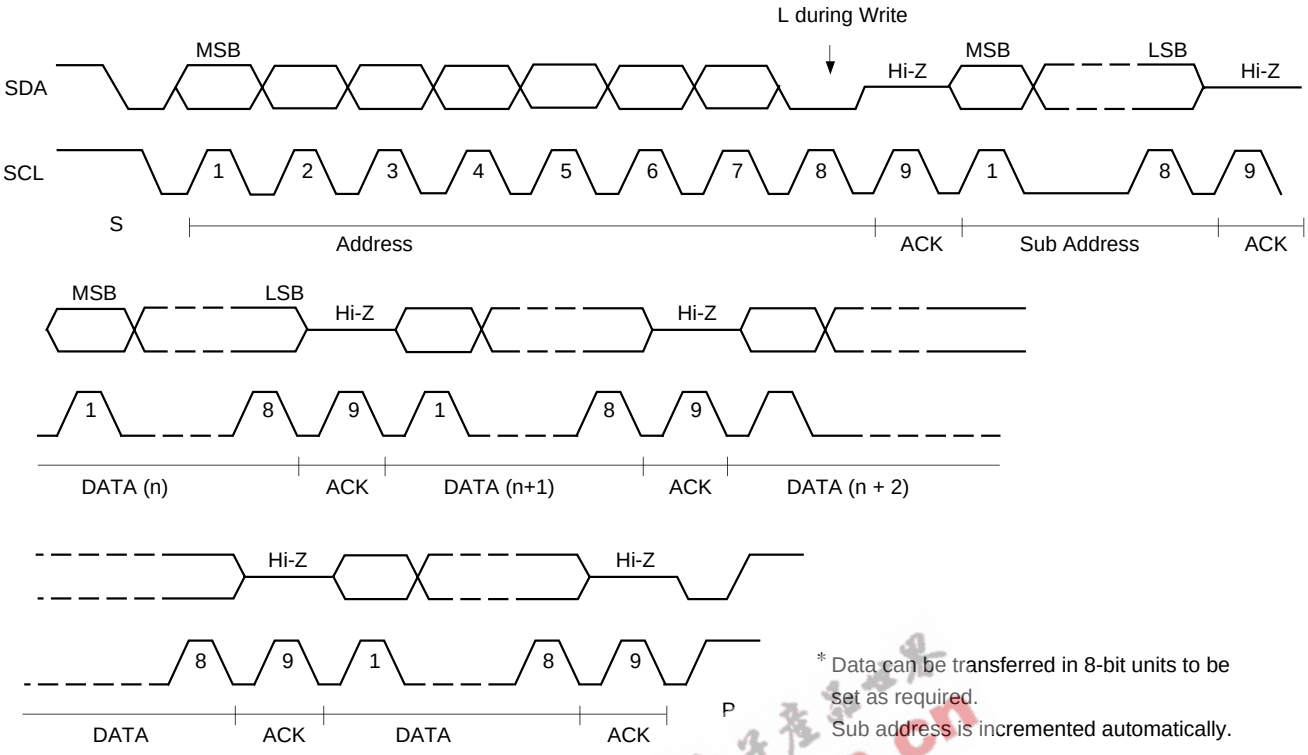
• Accordingly there are 3 values outputs, H, L and Hi-Z.



• I²C transfer begins with Start Condition and ends with Stop Condition.

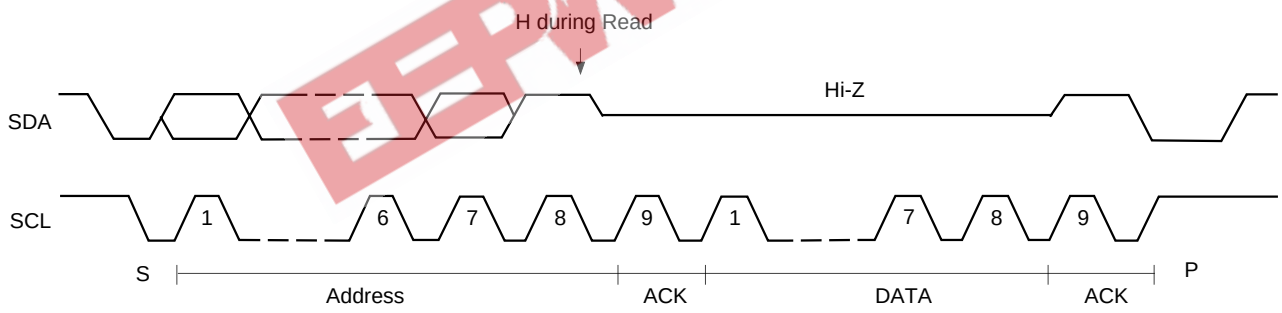


• **I²C data Write (Write from I²C controller to the IC)**

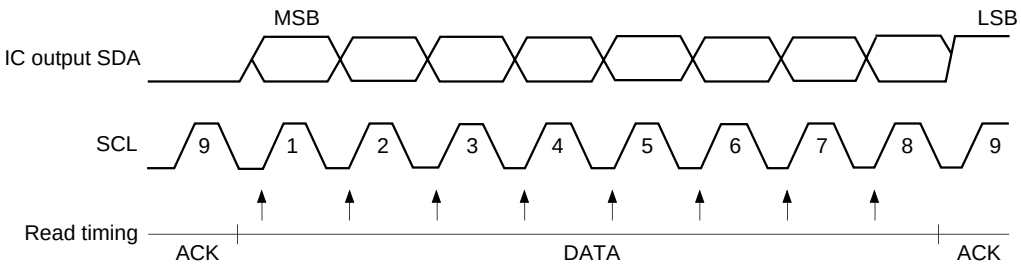


* Data can be transferred in 8-bit units to be set as required.
Sub address is incremented automatically.

• **I²C data Read (Read from the IC to I²C controller)**

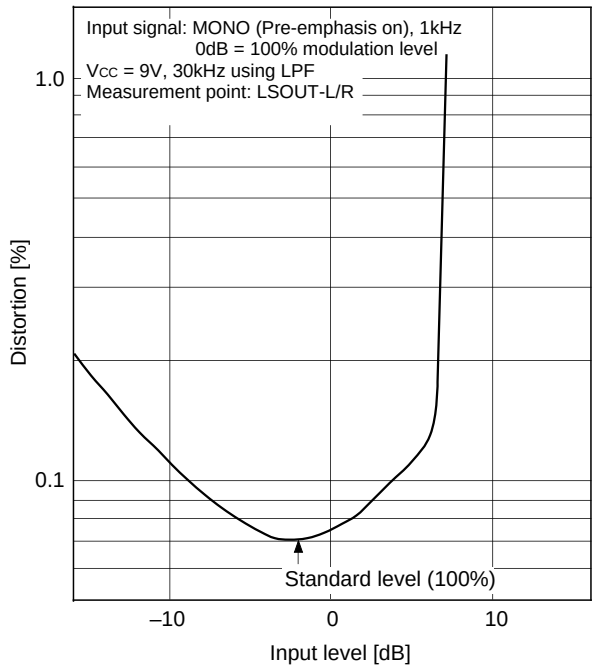


• **Read timing**

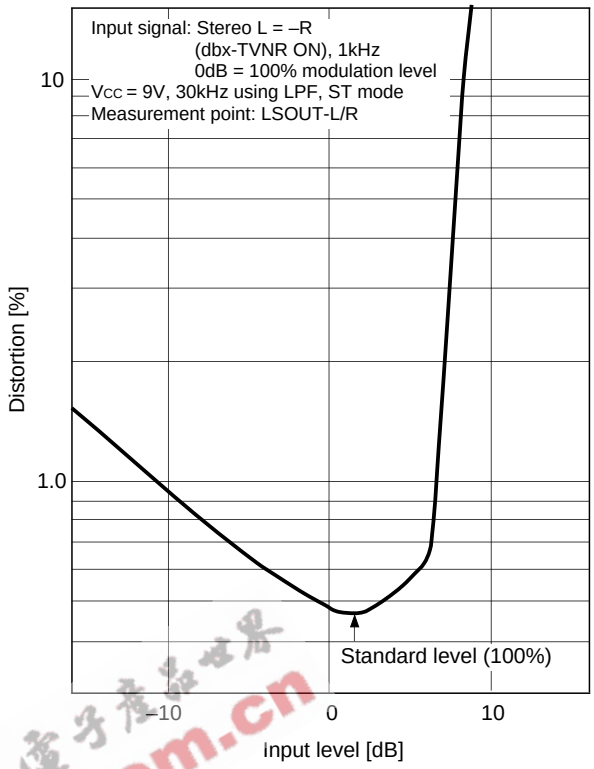


* Data Read is performed during SCL rise.

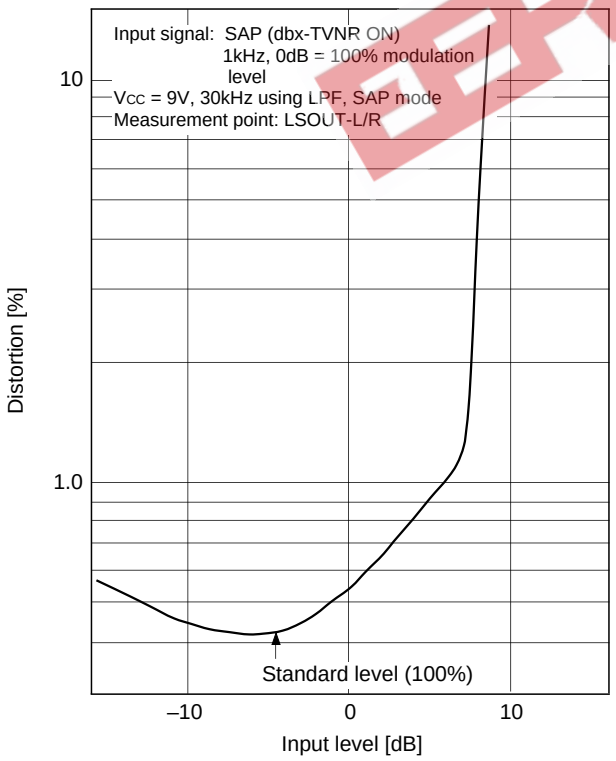
Input level vs. Distortion characteristics 1 (MONO)



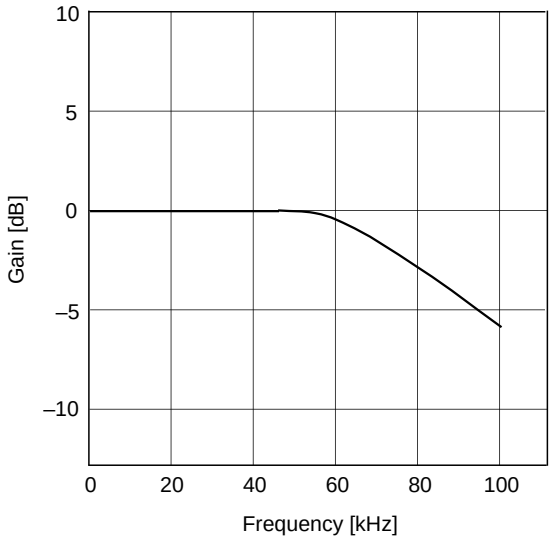
Input level vs. Distortion characteristics 2 (Stereo)



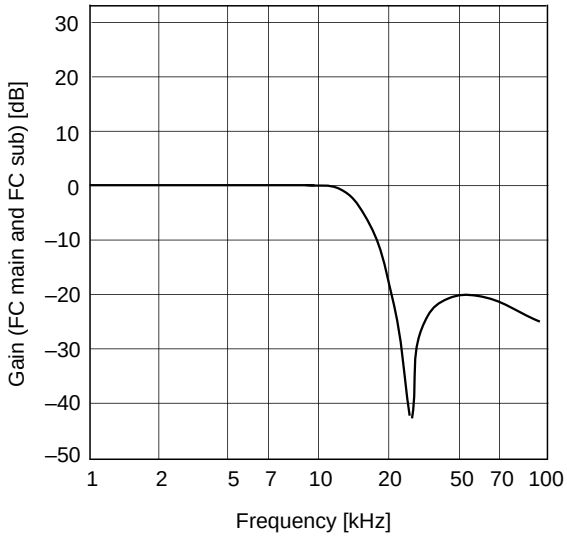
Input level vs. Distortion characteristics 3 (SAP)



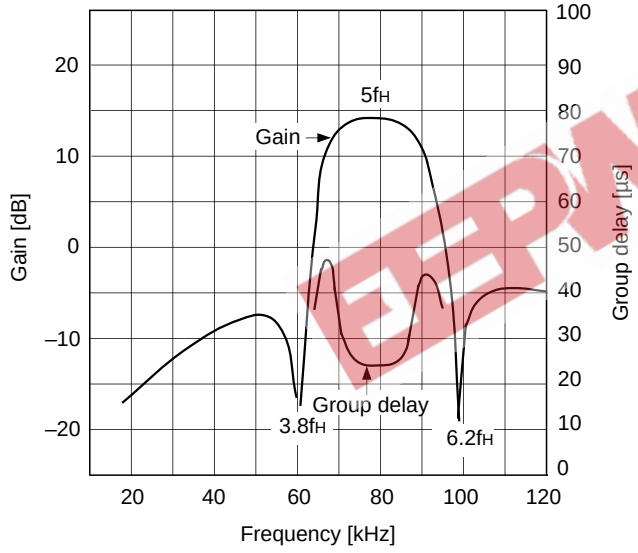
Stereo LPF frequency characteristics



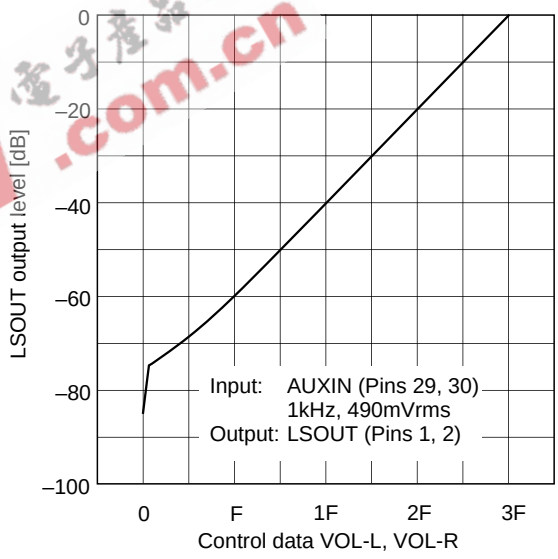
Main LPF and Sub LPF frequency characteristics



SAP frequency characteristics and group delay

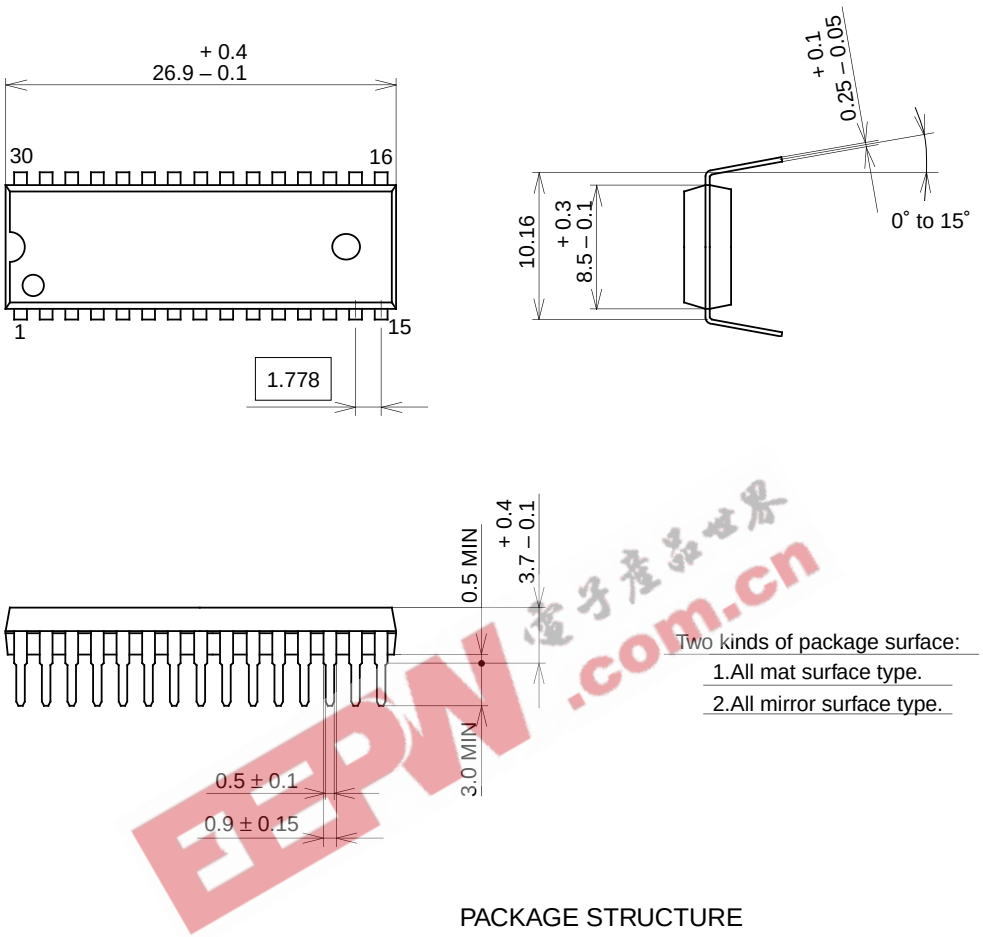


Volume charactiristics



Package Outline Unit: mm

30PIN SDIP (PLASTIC)



SONY CODE	SDIP-30P-01
EIAJ CODE	P-SDIP30-8.5x26.9-1.778
JEDEC CODE	————

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g