

## All Band TV Tuner IC with On-chip PLL

### Description

The CXA3252N is a monolithic TV tuner IC which integrates local oscillator and mixer circuits for VHF band, local oscillator and mixer circuits for UHF band, an IF amplifier and a tuning PLL onto a single chip, enabling further miniaturization of the tuner.

### Features

- Superior cross modulation
- Supports both IF double-tuned filter and adjacent channel trap.
- Balanced UHF oscillator (4 pins) with excellent oscillation stability
- Supports both I<sup>2</sup>C and 3-wire bus modes
- Automatic identification of 18, 19 or 27-bit control (during 3-wire bus mode)
- On-chip high voltage drive transistor for charge pump
- Reference frequency selectable from 31.25, 50 or 62.5 kHz (when using a 4 MHz crystal)
- Low-phase noise synthesizer
- On-chip 4-output band switch (supports output voltages from 5 to 9 V)
- 32 pin SSOP

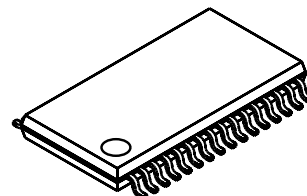
### Applications

- TV tuners
- VCR tuners
- CATV tuners

### Structure

Bipolar silicon monolithic IC

32 pin SSOP (Plastic)



### Absolute Maximum Ratings (Ta=25 °C)

- Supply voltage  $V_{cc1}, V_{cc2}$  -0.3 to + 5.5 V  
 $V_{cc3}$  -0.3 to +10.0 V
- Storage temperature  $T_{stg}$  -55 to + 150 °C
- Allowable power dissipation

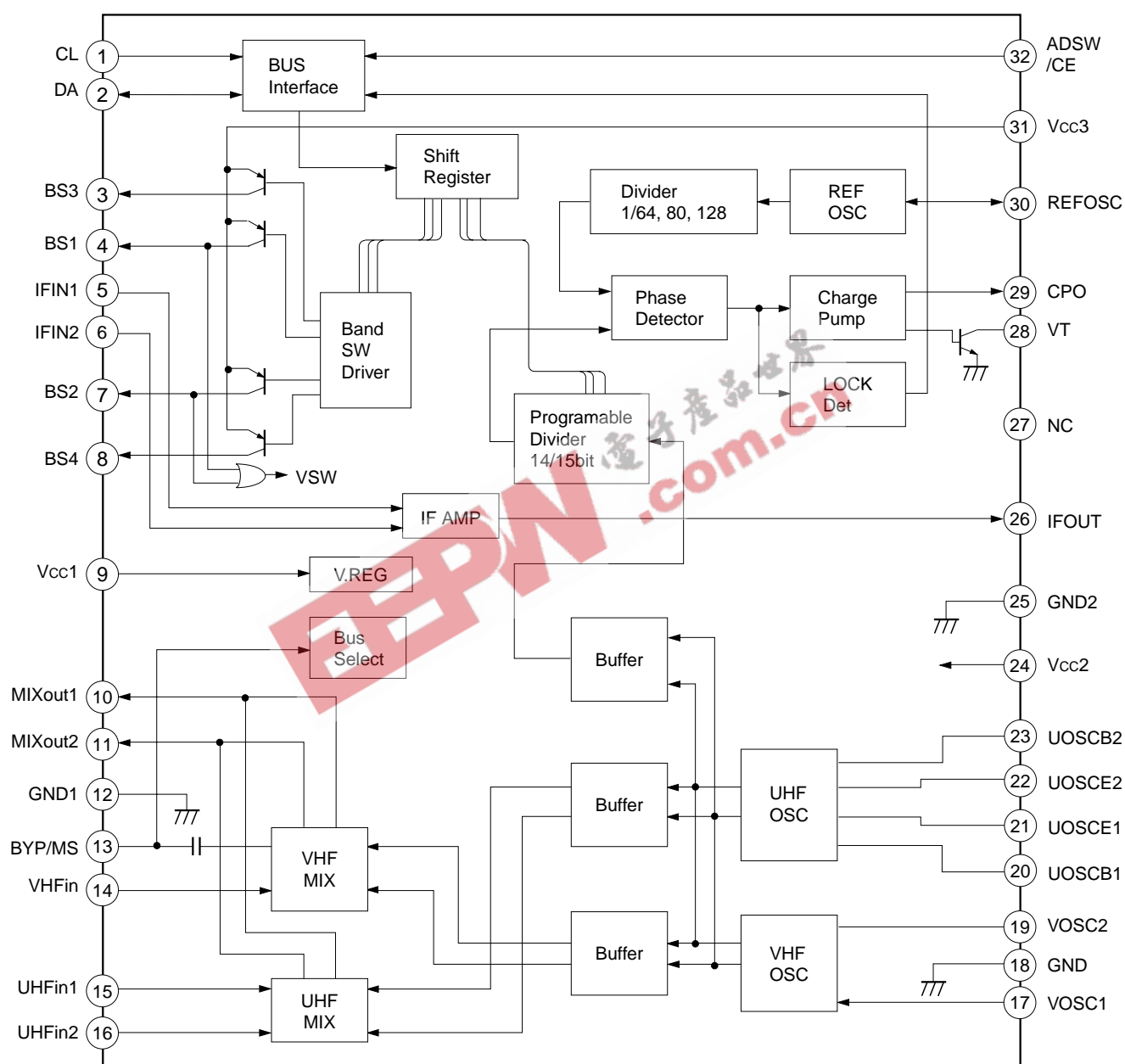
### Operating Conditions

- Supply voltage  $V_{cc1}, V_{cc2}$  4.75 to 5.30 V  
 $V_{cc3}$  4.75 to 9.45 V
- Operating temperature  $T_{opr}$  -25 to +75 °C  
 $P_d$  580 mW  
(when mounted on a printed circuit board)

This IC has the pins whose electrostatic discharge strength is weak as the operating frequency is high and the high-frequency process is used for this IC. Take care of handling the IC.

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## Block Diagram and Pin Configuration



## Pin Description

| Pin No. | Symbol  | Description                                     |
|---------|---------|---|
| 1       | CL      | CLOCK/SCL (I <sup>2</sup> C bus)                |
| 2       | DA      | DATA/SDA (I <sup>2</sup> C bus)                 |
| 3       | BS3     | Band switch output 3                            |
| 4       | BS1     | Band switch output 1 (VHF low band)             |
| 5       | IFIN1   | IF amplifier input 1                            |
| 6       | IFIN2   | IF amplifier input 2                            |
| 7       | BS2     | Band switch output 2 (VHF high band)            |
| 8       | BS4     | Band switch output 4                            |
| 9       | VCC1    | Analog circuit Vcc                              |
| 10      | MIXOUT1 | MIX output (open collector)                     |
| 11      | MIXOUT2 | MIX output (open collector)                     |
| 12      | GND1    | Analog circuit GND                              |
| 13      | BYP/MS  | VHF input GND and control bus switching         |
| 14      | VHFIN   | VHF input                                       |
| 15      | UHFIN1  | UHF input                                       |
| 16      | UHFIN2  | UHF input                                       |
| 17      | VOSC1   | VHF oscillator (base input)                     |
| 18      | GND     | GND   |
| 19      | VOSC2   | VHF oscillator (collector output)               |
| 20      | UOSCB1  | UHF oscillator (base pin)                       |
| 21      | UOSCE1  | UHF oscillator (emitter pin)                    |
| 22      | UOSCE2  | UHF oscillator (emitter pin)                    |
| 23      | UOSCB2  | UHF oscillator (base pin)                       |
| 24      | VCC2    | PLL circuit Vcc                                 |
| 25      | GND2    | PLL circuit GND                                 |
| 26      | IFOUT   | IF amplifier output                             |
| 27      | NC      | OPEN  |
| 28      | VT      | Tuning voltage output (open collector)          |
| 29      | CPO     | Charge pump output (loop filter connection)     |
| 30      | REFOSC  | Crystal connection                              |
| 31      | VCC3    | Band switch power supply                        |
| 32      | ADSW/CE | Enable/address selection (I <sup>2</sup> C bus) |

## Pin Description and Equivalent Circuit

| Pin No. | Symbol | Pin Voltage [V]       | Equivalent circuit | Description   |  |
|---------|--------|-----------------------|--------------------|---|--|
| 1       | CL     | —                     |                    | Clock input.  |  |
| 2       | DA     | —                     |                    | DATA input.   |  |
| 3       | BS3    | ON : 4.8<br>OFF : 0.0 |                    | Band switch outputs.<br>The pin corresponding to the selected band goes High. |  |
| 8       | BS4    |                       |                    |   |  |
| 4       | BS1    | 2.1                   |                    |   |  |
| 7       | BS2    |                       |                    |   |  |
| 5       | IFIN1  | 2.1                   |                    |   |  |
| 6       | IFIN2  |                       |                    |   |  |
| 9       | VCC1   | —                     |                    | Analog circuit power supply.  |  |

| Pin No. | Symbol  | Pin Voltage [V]                                      | Equivalent circuit | Description  |
|---------|---------|--|--------------------|--|
| 10      | MIXOUT1 | —  |                    | <p>Mixer output.</p> <p>These pins output the signal with open collector, and they must be connected to the power supply via the load.</p>                       |
| 11      | MIXOUT2 | —  |                    |  |
| 12      | GND1    | —  | —                  | Analog circuit GND.  |
| 13      | BYP/MS  | 3.8 during VHF reception<br>3.8 during UHF reception |                    | <p>Pin 12 : VHF input grounding and control bus switching.</p> <p>Pin 13 : VHF input.<br/>Input format is the unbalanced input.</p>                              |
| 14      | VHFin   | 2.6 during VHF reception<br>0.1 during UHF reception |                    |  |
| 15      | UHFin1  | 2.6 during UHF reception<br>0.1 during VHF reception |                    | <p>UHF inputs.</p> <p>Input the signal to Pins 14 and 15 symmetrically or ground either of Pin 14 or 15 with the capacitor and input the signal to the rest.</p> |
| 16      | UHFin2  | 2.6 during UHF reception<br>0.1 during VHF reception |                    |  |
| 17      | VOSC1   | 2.1 during VHF reception<br>2.3 during UHF reception |                    | <p>External resonance circuit connection for VHF oscillator.</p>   |
| 19      | VOSC2   | 4.2 during VHF reception<br>5.0 during UHF reception |                    |  |
| 18      | GND     | —  | —                  | GND for separating the analog and PLL systems.   |

| Pin No. | Symbol  | Pin Voltage [V]                                      | Equivalent circuit | Description  |
|---------|---------|--|--------------------|--|
| 20      | UOSCB1  | 2.1 during UHF reception<br>2.3 during VHF reception |                    | External resonance circuit connection for UHF oscillator.  |
| 21      | UOSCE1  | 1.4 during UHF reception<br>1.8 during VHF reception |                    |  |
| 22      | UOSCE2  | 1.4 during UHF reception<br>1.8 during VHF reception |                    |  |
| 23      | UOSCB2  | 2.1 during UHF reception<br>2.3 during VHF reception |                    |  |
| 24      | VCC2    | —  | —                  | PLL circuit power supply   |
| 25      | GND2    | —  | —                  | PLL circuit GND.   |
| 26      | IFOUT   | 2.7  |                    | I/F output.  |
| 27      | NC      | —  | —                  |  |
| 28      | VT      | —  |                    | Varicap drive voltage output. This pin outputs the signal with open collector, and this must be connected to the tuning power supply via the load. Charge pump output. Connects the loop filter. |
| 29      | CPO     | 2.0  |                    |  |
| 30      | REFOSC  | 4.3  |                    | Crystal connection for reference oscillator.   |
| 31      | VCC3    | —  | —                  | Power supply for external supply.  |
| 32      | ADSW/CE | 1.25<br>(when open)                                  |                    | <p>I<sup>2</sup>C bus setting :</p> <p>Address selection.<br/>Bits 1 and 2 of the address byte are controlled.</p> <p>3-wire bus setting :</p> <p>Enable input.</p>                              |

## Electrical Characteristics

Circuit Current

(VCC=5 V, Ta=25°C)

| Item              | Symbol | Measurement conditions                                     | Min. | Typ. | Max. | Unit |
|-------------------|--------|--|------|------|------|------|
| Circuit current A | Alccv  | Vcc1 current, band switch output open during VHF operation |      |      |      | mA   |
|                   | Alccu  | Vcc1 current, band switch output open during UHF operation |      |      |      | mA   |
| Circuit current D | DIcc   | Vcc2 current   |      |      |      | mA   |

## OSC/MIX/IF Amplifier Block

| Item                       | Symbol | Measurement conditions   | Min. | Typ. | Max. | Unit |
|----------------------------|--------|--|------|------|------|------|
| Conversion gain            | CG1    | VHF operation f <sub>RF</sub> =55 MHz  |      |      |      | dB   |
|                            | CG2    | VHF operation f <sub>RF</sub> =360 MHz   |      |      |      | dB   |
|                            | CG3    | UHF operation f <sub>RF</sub> =360 MHz   |      |      |      | dB   |
|                            | CG4    | UHF operation f <sub>RF</sub> =800 MHz   |      |      |      | dB   |
| Noise figure *1, *2        | NF1    | VHF operation f <sub>RF</sub> =55 MHz  |      |      |      | dB   |
|                            | NF2    | VHF operation f <sub>RF</sub> =360 MHz   |      |      |      | dB   |
|                            | NF3    | UHF operation f <sub>RF</sub> =360 MHz   |      |      |      | dB   |
|                            | NF4    | UHF operation f <sub>RF</sub> =800 MHz   |      |      |      | dB   |
| 1% cross modulation *1, *3 | CM1    | VHF operation<br>f <sub>D</sub> =55 MHz, f <sub>UD</sub> =±12 MHz                |      |      |      | dBμ  |
|                            | CM2    | VHF operation<br>f <sub>D</sub> =360 MHz, f <sub>UD</sub> =±12 MHz               |      |      |      | dBμ  |
|                            | CM3    | UHF operation<br>f <sub>D</sub> =360 MHz, f <sub>UD</sub> =±12 MHz               |      |      |      | dBμ  |
|                            | CM4    | UHF operation<br>f <sub>D</sub> =800 MHz, f <sub>UD</sub> =±12 MHz               |      |      |      | dBμ  |
| Maximum output power       | Pomax  | 50 Ω load saturation output  |      |      |      | dBm  |
| Switch ON drift *4         | Δ fsw1 | VHF operation f <sub>osc</sub> =100 MHz<br>Δ f from 3 s to 3 min after switch ON |      |      |      | kHz  |
|                            | Δ fsw2 | VHF operation f <sub>osc</sub> =405 MHz<br>Δ f from 3 s to 3 min after switch ON |      |      |      | kHz  |
|                            | Δ fsw3 | UHF operation f <sub>osc</sub> =405 MHz<br>Δ f from 3 s to 3 min after switch ON |      |      |      | kHz  |
|                            | Δ fsw4 | UHF operation f <sub>osc</sub> =845 MHz<br>Δ f from 3 s to 3 min after switch ON |      |      |      | kHz  |

| Item                                  | Symbol           | Measurement conditions  | Min. | Typ. | Max. | Unit   |
|---------------------------------------|------------------|---|------|------|------|--------|
| Supply voltage <sup>*4</sup><br>drift | $\Delta f_{st1}$ | VHF operation $f_{osc}=100$ MHz<br>$\Delta f$ when $V_{cc}$ 5 V changes $\pm 5\%$ |      |      |      | kHz    |
|                                       | $\Delta f_{st2}$ | VHF operation $f_{osc}=405$ MHz<br>$\Delta f$ when $V_{cc}$ 5 V changes $\pm 5\%$ |      |      |      | kHz    |
|                                       | $\Delta f_{st3}$ | UHF operation $f_{osc}=405$ MHz<br>$\Delta f$ when $V_{cc}$ 5 V changes $\pm 5\%$ |      |      |      | kHz    |
|                                       | $\Delta f_{st4}$ | UHF operation $f_{osc}=845$ MHz<br>$\Delta f$ when $V_{cc}$ 5 V changes $\pm 5\%$ |      |      |      | kHz    |
| Oscillator phase<br>noise             | C/N V            | 10 kHz offset   |      |      |      | dBc/Hz |
|                                       | C/N U            | 10 kHz offset   |      |      |      | dBc/Hz |
| Reference leak                        | REFL             | Phase comparison frequency of<br>62.5 kHz, CP : 1                                 |      |      |      | dB     |
| Lock-up time                          | LUT 1            |   |      |      |      | msec   |
|                                       | LUT 2            |   |      |      |      | msec   |

<sup>\*1</sup> Value measured with untuned input.

<sup>\*2</sup> NF meter direct-reading value (DSB measurement).

<sup>\*3</sup> Value with a desired reception signal input level of  $-30$  dBm, an interference signal of 100 kHz/30 % AM, and an interference signal level where  $S/I=46$  dB measured with a spectrum analyzer.

<sup>\*4</sup> Value when the PLL is not operating.



## PLL Block

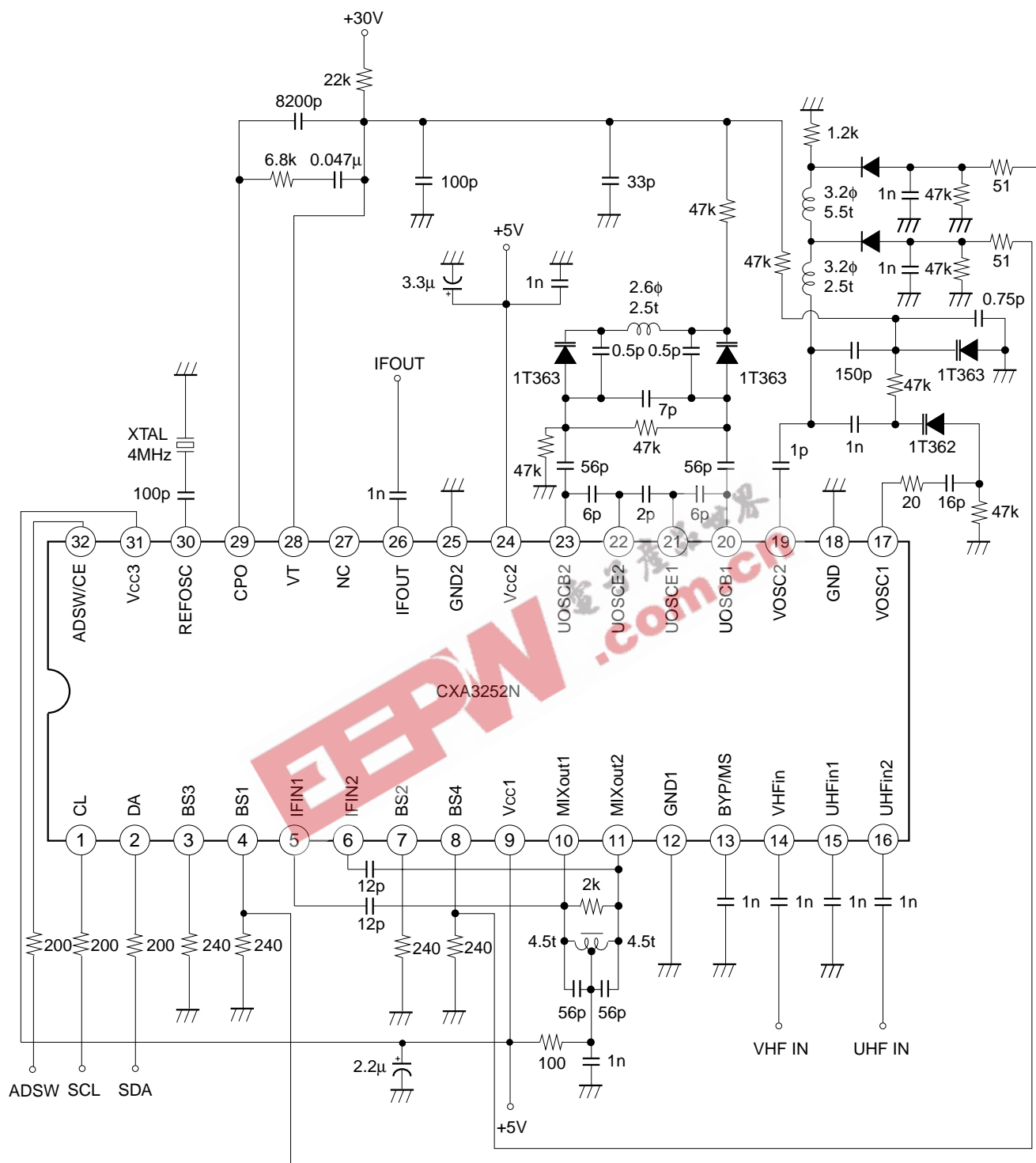
| Item                        | Symbol             | Measurement conditions           | Min.                 | Typ. | Max.            | Unit |
|-----------------------------|--------------------|----------------------------------|----------------------|------|-----------------|------|
| CL, DA pins                 |                    |                                  |                      |      |                 |      |
| "H" level input voltage     | V <sub>IH</sub>    |                                  | 3                    |      | V <sub>CC</sub> | V    |
| "L" level input voltage     | V <sub>IL</sub>    |                                  | GND                  |      | 1.5             | V    |
| "H" level input current     | I <sub>IH</sub>    | V <sub>IH</sub> =V <sub>CC</sub> |                      | 0    | -0.1            | μA   |
| "L" level input current     | I <sub>IL</sub>    | V <sub>IL</sub> =GND             |                      | -0.3 | -4              | μA   |
| CE input                    |                    |                                  |                      |      |                 |      |
| "H" level input voltage     | V <sub>IH</sub>    |                                  | 3                    |      | V <sub>CC</sub> | V    |
| "L" level input voltage     | V <sub>IL</sub>    |                                  | GND                  |      | 1.5             | V    |
| "H" level input current     | I <sub>IH</sub>    | V <sub>IH</sub> =V <sub>CC</sub> |                      | -100 | -200            | μA   |
| "L" level input current     | I <sub>IL</sub>    | V <sub>IL</sub> =GND             |                      | 35   | 100             | μA   |
| SDA output                  |                    |                                  |                      |      |                 |      |
| "H" output leak current     | V <sub>IH</sub>    | V <sub>in</sub> =5.5 V           |                      |      | 5               | V    |
| "L" output voltage          | V <sub>IL</sub>    | I <sub>out</sub> =-3 mA          | GND                  |      | 0.4             | V    |
| CPO (charge pump)           |                    |                                  |                      |      |                 |      |
| Output current 1            | I <sub>CPO1</sub>  | Byte4/Bit6=0                     | ±35                  | ±50  | ±75             | μA   |
| Leak current 1              | LeakCP1            | Byte4/Bit6=0                     |                      |      | 30              | nA   |
| Output current 2            | I <sub>CPO2</sub>  | Byte4/Bit6=1                     | ±140                 | ±200 | ±300            | μA   |
| Leak current 2              | LeakCP2            | Byte4/Bit6=1                     |                      |      | 100             | nA   |
| VT (VC voltage output)      |                    |                                  |                      |      |                 |      |
| Maximum output voltage      | V <sub>TH</sub>    |                                  |                      |      | 33              | V    |
| Minimum output voltage      | V <sub>TL</sub>    |                                  |                      | 0.5  | 0.8             | V    |
| LOCK                        |                    |                                  |                      |      |                 |      |
| "H" output voltage          | V <sub>LOCKH</sub> | When locked                      | V <sub>CC</sub> -0.5 |      | V <sub>CC</sub> | V    |
| "L" output voltage          | V <sub>LOCKL</sub> | When unlocked                    | 0                    |      | 0.5             | V    |
| REFOSC                      |                    |                                  |                      |      |                 |      |
| Oscillation frequency range | F <sub>XTOSC</sub> |                                  | 3                    |      | 12              | MHz  |
| Input capacitance           | C <sub>XTOSC</sub> |                                  | 22                   | 24   | 26              | pF   |
| Negative resistance         | R <sub>NEG</sub>   | Crystal source impedance         |                      | -2   | -1              | kΩ   |
| Band SW                     |                    |                                  |                      |      |                 |      |
| Output current              | I <sub>BS</sub>    | When ON                          |                      |      | -25             | mA   |
| Saturation voltage          | V <sub>SAT</sub>   | When ON Source current=20 mA     |                      | 120  | 240             | mV   |
| Leak current                | LeakBS             | When OFF                         |                      | 0.5  | 3               | μA   |

| Item                              | Symbol | Measurement conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--------|------------------------|------|------|------|------|
| Bus timing (I <sup>2</sup> C bus) |        |                        |      |      |      |      |
| SCL clock frequency               | fSCL   |                        | 0    |      | 400  | kHz  |
| Start waiting time                | twSTA  |                        | 1300 |      |      | ns   |
| Start hold time                   | thSTA  |                        | 600  |      |      | ns   |
| “L” hold time                     | tLOW   |                        | 1300 |      |      | ns   |
| “H” hold time                     | thIGH  |                        | 600  |      |      | ns   |
| Start setup time                  | tsSTA  |                        | 600  |      |      | ns   |
| Data hold time                    | taHDAT |                        | 1300 |      |      | ns   |
| Data setup time                   | tsDAT  |                        | 600  |      |      | ns   |
| Rise time                         | tr     |                        |      |      | 300  | ns   |
| Fall time                         | tf     |                        |      |      | 300  | ns   |
| Stop setup time                   | tsSTO  |                        | 600  |      |      | ns   |
| Bus timing (3-wire bus)           |        |                        |      |      |      |      |
| Data setup time                   | tsD    |                        | 300  |      |      | ns   |
| Data hold time                    | thD    |                        | 600  |      |      | ns   |
| Enable waiting time               | tWE    |                        | 300  |      |      | ns   |
| Enable setup time                 | tSE    |                        | 300  |      |      | ns   |
| Enable hold time                  | tHE    |                        | 600  |      |      | ns   |

The schematic diagram illustrates the internal structure and pin connections of the CXA3252N IC. The IC is a 32-pin device with pins 1-16 on the bottom and 17-32 on the top. The internal circuit includes a 4MHz XTAL oscillator, various input and output filters, and a complex internal circuit with multiple transistors and capacitors. External components include resistors, capacitors, and a 3.2MHz crystal. The diagram is labeled with 'CXA3252N' and 'EEPW.com'.

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Electrical Characteristics Measurement Circuit (3-wire bus control)



Unmarked Ls are air coils with a wire diameter of 0.5 mm.



The schematic diagram illustrates the internal structure and pin connections of the CXA3252N IC. The IC is a 32-pin device with pins 1-16 on the bottom and 17-32 on the top. Key pins and their connections are as follows:

- Pin 1 (CL):** Connected to a 47pF capacitor to ground.
- Pin 2 (DA):** Connected to a 200Ω resistor to ground.
- Pin 3 (BS3):** Connected to a 200Ω resistor to ground.
- Pin 4 (BS1):** Connected to a 1000pF capacitor to ground.
- Pin 5 (IFIN1):** Connected to a 3.2pF capacitor to ground.
- Pin 6 (IFIN2):** Connected to a 3.2pF capacitor to ground.
- Pin 7 (BS2):** Connected to a 68pF capacitor to ground.
- Pin 8 (BS4):** Connected to a 1000pF capacitor to ground.
- Pin 9 (Vcc1):** Connected to a 3.3μF capacitor to ground.
- Pin 10 (MIXout1):** Connected to a 2kΩ resistor to ground.
- Pin 11 (MIXout2):** Connected to a 2kΩ resistor to ground.
- Pin 12 (GND1):** Connected to ground.
- Pin 13 (BYPMIS):** Connected to a 1nF capacitor to ground.
- Pin 14 (VHFIn):** Connected to a 1nF capacitor to ground.
- Pin 15 (UHFIn1):** Connected to a 1nF capacitor to ground.
- Pin 16 (UHFIn2):** Connected to a 1nF capacitor to ground.
- Pin 17 (VOSC1):** Connected to a 10kΩ resistor to ground.
- Pin 18 (GND):** Connected to ground.
- Pin 19 (VOSC2):** Connected to a 10kΩ resistor to ground.
- Pin 20 (UOSGB1):** Connected to a 10kΩ resistor to ground.
- Pin 21 (UOSCE1):** Connected to a 10kΩ resistor to ground.
- Pin 22 (UOSCE2):** Connected to a 10kΩ resistor to ground.
- Pin 23 (UOSCB2):** Connected to a 10kΩ resistor to ground.
- Pin 24 (Vcc2):** Connected to a 3.3μF capacitor to ground.
- Pin 25 (GND2):** Connected to ground.
- Pin 26 (IFOUT):** Connected to a 10pF capacitor to ground.
- Pin 27 (NC):** Not connected.
- Pin 28 (VT):** Connected to a 4.7nF capacitor to ground.
- Pin 29 (CPO):** Connected to a 39kΩ resistor to ground.
- Pin 30 (REFOSC):** Connected to a 100pF capacitor to ground.
- Pin 31 (Vcc3):** Connected to a 100pF capacitor to ground.
- Pin 32 (ADSW/CE):** Connected to a 3kΩ resistor to ground.

The diagram also shows various external components like resistors, capacitors, and inductors connected to these pins. A large red watermark 'EEPW.com' is overlaid on the diagram.

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## Description of Functions

The CXA3252N is a ground wave broadcast tuner IC which converts frequencies to IF in order to tune and detect only the desired reception frequency of VHF, CATV and UHF band signals.

In addition to the mixer, local oscillation and IF amplifier circuits required for frequency conversion to IF, this IC also integrates a PLL circuit for local oscillation frequency control onto a single chip.

The functions of the various circuits are described below.

### 1. Mixer circuit

This circuit outputs the frequency difference between the signal input to VHFIN or UHFIN and the local oscillation signal.

### 2. Local oscillation circuit

A VCO is formed by externally connecting an LC resonance circuit composed of a varicap diode and inductance.

### 3. IF amplifier circuit

This circuit amplifies the mixer IF output, and consists of an amplifier stage and low impedance output stage.

### 4. PLL circuit

This PLL circuit fixes the local oscillation frequency to the desired frequency. It consists of a programmable divider, reference divider, phase detector, charge pump and reference oscillator. The control format supports both the I<sup>2</sup>C bus and 3-wire bus formats.

During I<sup>2</sup>C bus control, the frequency steps of 31.25, 50 or 62.5 kHz can be selected by the frequency division setting value of the data-based referencedivider.

During 3-wire bus control, these frequency steps can be selected by the combination of the data length (18 or 19 bits) and the voltage applied to the BYP/MS pin.

### 5. Band switch circuit

The CXA3252N has four sets of built-in PNP transistors for switching between the VL, VH and UHF bands and for switching the FM trap, etc. These PNP transistors can be controlled by the bus data.

The emitters for these PNP transistors are connected to an independent power supply pin (Vcc3) from the oscillator, mixer and PLL circuits, and support either 5 V or 9 V as the RF amplifier power supply.

## Description of Analog Block Operation

(See the Electrical Characteristics Measurement Circuit.)

### VHF oscillator circuit

- This circuit is a differential amplifier type oscillator circuit. Pin 19 is the output and Pin 17 is the input. Oscillation is performed by connecting an LC resonance circuit including a varicap to Pin 19 via coupled capacitance, inputting to Pin 17 with feedback capacitance, and applying positive feedback.
- The amplifier between Pins 17 and 19 has an extremely high gain. Therefore, care should be taken to avoid creating parasitic capacitance, resistance or other feedback loops as this may produce abnormal oscillation.

### VHF mixer circuit

- The mixer circuit employs a double balanced mixer with little local oscillation signal leakage. The input format is base input type, with Pin 13 grounded via a capacitor and the RF signal input to Pin 14. (Pin 13 can also be used to switch the PLL mode according to the applied DC voltage value.)
- The RF signal is converted to IF frequency by oscillator signal and output from Pins 10 and 11. Pins 10 and 11 are open collectors, so external power supply is necessary. In addition, single-tuned filters are connected to Pins 10 and 11.

### UHF oscillator circuit

- This oscillator circuit is designed so that two collector ground type Colpitts oscillators perform differential oscillation operation via an LC resonance circuit including a varicap.
- Resonance capacitance is connected between Pins 20 and 21, Pins 21 and 22, and Pins 22 and 23, and an LC resonance circuit including a varicap is connected between Pins 20 and 23.

### UHF mixer circuit

- This circuit employs a double balanced mixer like the VHF mixer circuit. The input format is base input type, with Pins 15 and 16 as the RF input pins. The input method can be selected from balanced input consisting of differential input to Pins 15 and 16 or unbalanced input consisting of grounding Pin 15 via a capacitor and input to Pin 16.
- Pins 10 and 11 are the mixer outputs. Pins 10 and 11 are open collectors, so external power supply is necessary. In addition, single-tuned filters are connected to Pins 10 and 11.

### IF amplifier circuit

- Pins 5 and 6 are IF amplifier inputs with an input impedance of approximately 1 k $\Omega$ .
- The signals frequency converted by the mixer are output from Pins 10 and 11, so Pins 10 and 11 are connected to Pins 5 and 6 via capacitors. (A neighboring channel trap circuit can be formed by connecting a L and C parallel circuit instead of capacitors.)
- The signal amplified by the IF amplifier is output from Pin 26. The output impedance is approximately 75  $\Omega$ .



## Description of PLL Block

This IC supports both I<sup>2</sup>C bus and 3-wire bus control.

The I<sup>2</sup>C bus conforms to the standard I<sup>2</sup>C bus format, and bidirectional bus control is possible consisting of a write mode in which various data are received and a read mode in which various data are sent.

The 3-wire bus is equipped with an 18- or 19-bit auto identify function, and the frequency step can be switched according to the voltage applied to the BYP/MS pin.

The PLL of this IC does not have a fixed frequency division circuit and performs high-speed phase comparison, providing low reference leak and quick lock-up time characteristics.

Pin Function Table

| Symbol  | I <sup>2</sup> C bus | 3-wire bus   |
|---------|----------------------|--------------|
| CL      | SCL input            | CLOCK input  |
| DA      | SDA I/O              | DATA input   |
| ADSW/CE | Address selection    | ENABLE input |

### 1) PLL Mode Setting Method

The selected control bus is set according to the BYP/MS pin (Pin 13) voltage.

| BYP/MS pin | Control bus          |
|------------|----------------------|
| GND        | I <sup>2</sup> C Bus |
| OPEN       | 3-wire bus           |
| Vcc        | 3-wire bus           |

During 3-wire bus control, the transferred bit length (18, 19 or 27 bits) is automatically identified.

During 18- or 19-bit transfer, the frequency steps in the table below are set according to the combination of the BYP/MS pin voltage and the bit length. This IC does not have a fixed frequency division circuit, so the phase comparison frequency becomes the frequency step.

| BYP/MS Pin voltage | Transfer bit length | Reference Divider             | Phase comparison frequency          | Frequency Step*                     |
|--------------------|---------------------|-------------------------------|-------------------------------------|-------------------------------------|
|                    | 18                  | 64                            | 62.5 kHz                            | 62.5 kHz                            |
| OPEN               | 19                  | 128                           | 31.25 kHz                           | 31.25 kHz                           |
| OPEN or VCC        | 27                  | Selectable from 64, 80 or 128 | 62.5 kHz/<br>50.0 kHz/<br>31.25 kHz | 62.5 kHz/<br>50.0 kHz/<br>31.25 kHz |
| VCC                | 18                  | 80                            | 50.0 kHz                            | 50.0 kHz                            |
| VCC                | 19                  | 80                            | 50.0 kHz                            | 50.0 kHz                            |

\* Phase comparison frequency and frequency step are for when the crystal oscillation=4 MHz.

## 2) Programming

The VCO lock frequency is obtained according to the following formula.

$$f_{osc} = f_{ref} \times (32 M + S)$$

$f_{osc}$  : local oscillator frequency

$f_{ref}$  : phase comparison frequency

$M$  : main divider frequency division ratio

$S$  : swallow counter frequency division ratio

The variable frequency division ranges of  $M$  and  $S$  are as follows, and are set as binary.

$$S < M \leq 1023 \text{ (} S < M \leq 511 \text{ during 18-bit transfer)}$$

$$0 \leq S \leq 31$$

## 3) I<sup>2</sup>C Bus Control

This IC conforms to the standard I<sup>2</sup>C bus format, and bidirectional bus control is possible consisting of a write mode in which various data are received and a read mode in which various data are sent. Write and read modes are recognized according to the setting of the final bit (R/W bit) of the address byte. Write mode is set when the R/W bit is "0" and read mode is set when the R/W bit is "1".

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## 3-1) Address settings

Up to four addresses can be selected by the hardware bit settings, so that multiple PLL can exist within one system.

The responding address can be set according to the ADSW/CE pin voltage.

|   |   |   |   |   |     |     |     |
|---|---|---|---|---|-----|-----|-----|
| 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/W |
|---|---|---|---|---|-----|-----|-----|

Address

| "CE" pin voltage              | MA1 | MA0 |
|-------------------------------|-----|-----|
| 0 to 0.1 VCC                  | 0   | 0   |
| OPEN or<br>0.2 VCC to 0.3 VCC | 0   | 1   |
| 0.4 VCC to 0.6 VCC            | 1   | 0   |
| 0.9 VCC to VCC                | 1   | 1   |

Hardware bits

## 3-2) Write mode

Write mode is used to receive various data. In this mode, byte 1 contains the address data, bytes 2 and 3 contain the frequency data, byte 4 contains the control data, and byte 5 contains the band switch data.

These data are latch transferred in the manner of byte 1, byte 2 + byte 3, and byte 4 + byte 5.

When the correct address is received and acknowledged, the data is recognized as frequency data if the first bit of the next byte is "0", and as control data and band switch data if this bit is "1".

Also, when data transmission is stopped part-way, the previously programmed data is valid. Therefore, once the control and band switch data have been programmed, 3-byte commands consisting of the address and frequency data are possible.

Further, even if the I<sup>2</sup>C bus stop conditions are not met, data can be input by sending the start conditions and the new address.

The control format is as shown in the table below.

Write-mode : Slave Receiver

|                | MSB  |      |      |      |      |      |      | LSB  |   |
|----------------|------|------|------|------|------|------|------|------|---|
| MODE           | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |   |
| Address byte   | 1    | 1    | 0    | 0    | 0    | MA1  | MA0  | 0    | A |
| Divider byte 1 | 0    | M9   | M8   | M7   | M6   | M5   | M4   | M3   | A |
| Divider byte 2 | M2   | M1   | M0   | S4   | S3   | S2   | S1   | S0   | A |
| Control byte   | 1    | CP   | 0    | CD   | X    | R1   | R0   | OS   | A |
| Band SW byte   | X    | X    | X    | X    | BS4  | BS3  | BS2  | BS1  | A |

X : Don't care

- A : Acknowledge bit  
 MA0, MA1 : address setting  
 M0 to : main divider frequency division ratio setting  
 S0 to : swallow counter frequency division ratio setting  
 CD : charge pump OFF (when "1")  
 OS : varicap output OFF (when "1")  
 CP : charge pump current switching (200  $\mu$ A when "1", 50  $\mu$ A when "0")  
 BS1 to BS4 : band switch control (output PNP transistor ON when "1")  
 R0, R1 : reference divider frequency division ratio setting.  
 (see the Reference Divider Frequency Division Ratio Table)

Reference Divider Frequency Division Ratio Table

| R1 | R0 | Reference divider |
|----|----|-------------------|
| 0  | 1  | 128               |
| 1  | 1  | 64                |
| X  | 0  | 80                |

X : Don't care

## 3-3) Read mode

In read mode, power- on reset operation status the phase comparator locked/unlocked status and 5-level A/D converter input pin voltage status are transmitted and output to the master.

The read data format is as shown in the table below.

Read mode : Slave Transmitter

| MODE         | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |   |
|--------------|------|------|------|------|------|------|------|------|---|
| Address byte | 1    | 1    | 0    | 0    | 0    | MA1  | MA0  | 1    | A |
| Status byte  | X    | FL   | 1    | 1    | 1    | 0    | 0    | 0    | A |

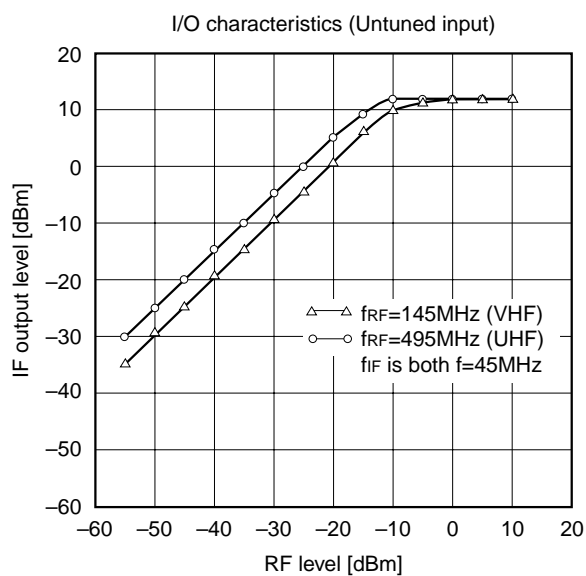
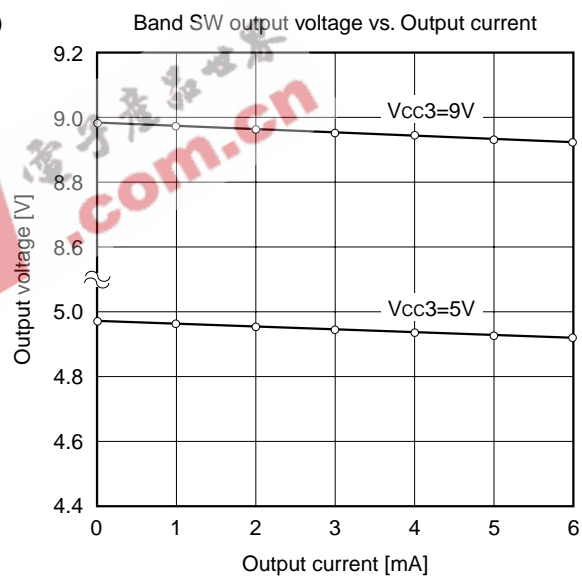
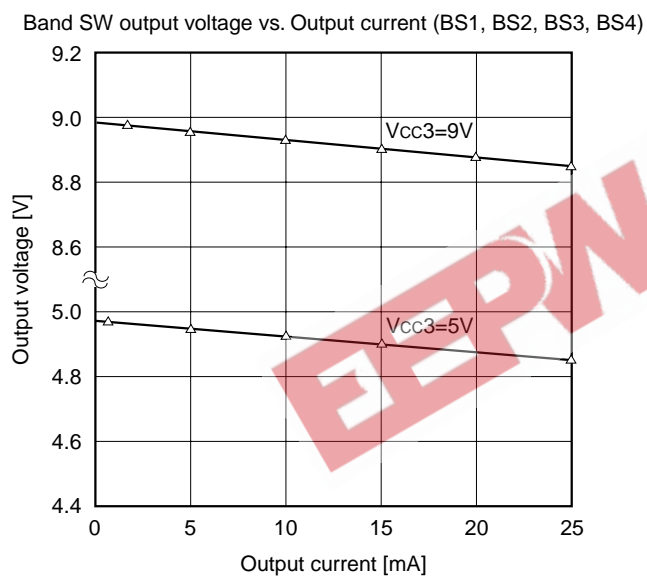
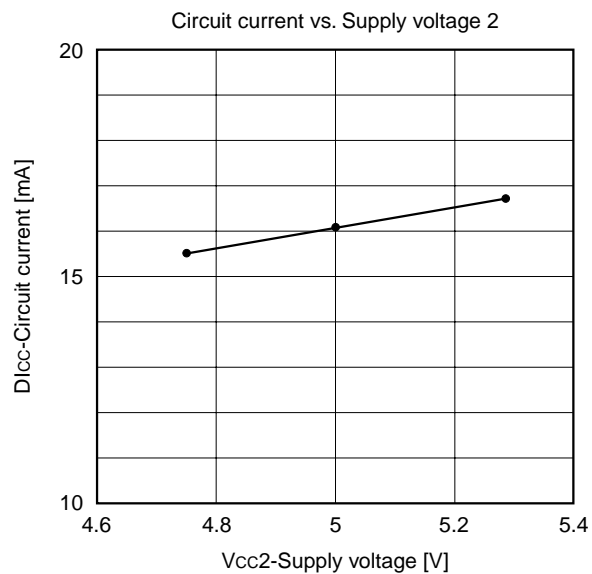
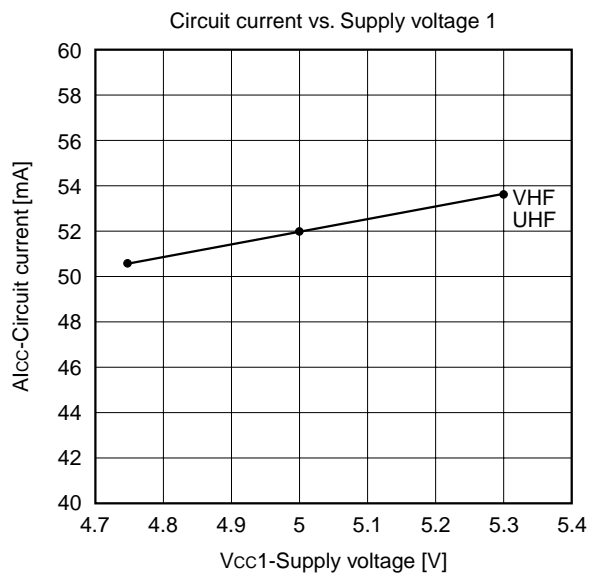
A : Acknowledge bit

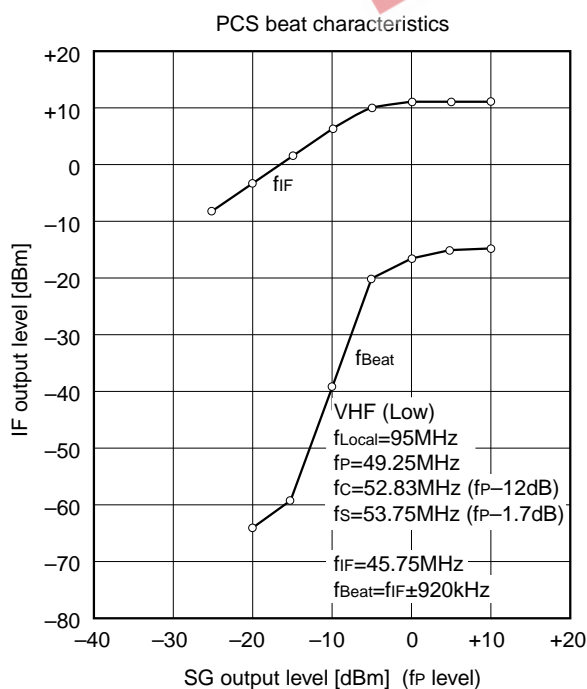
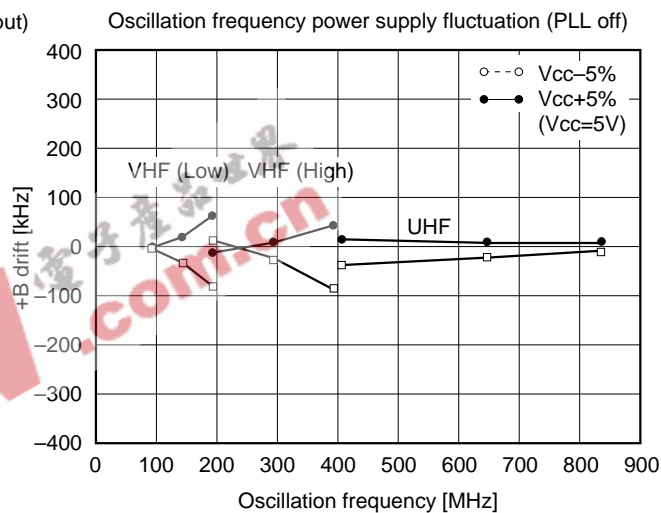
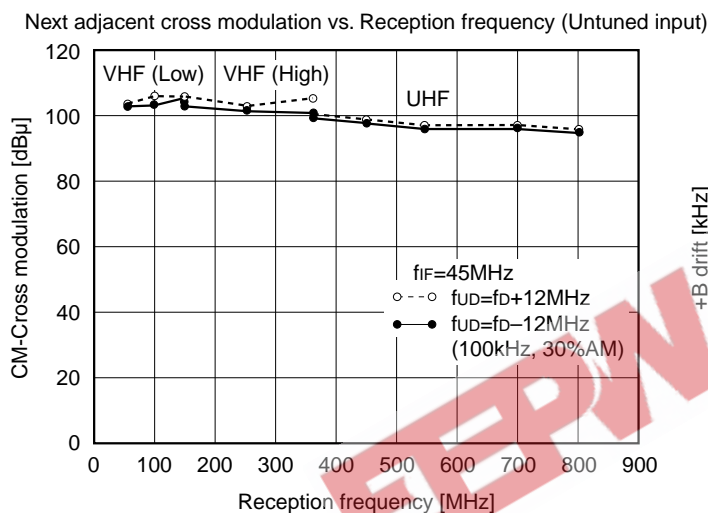
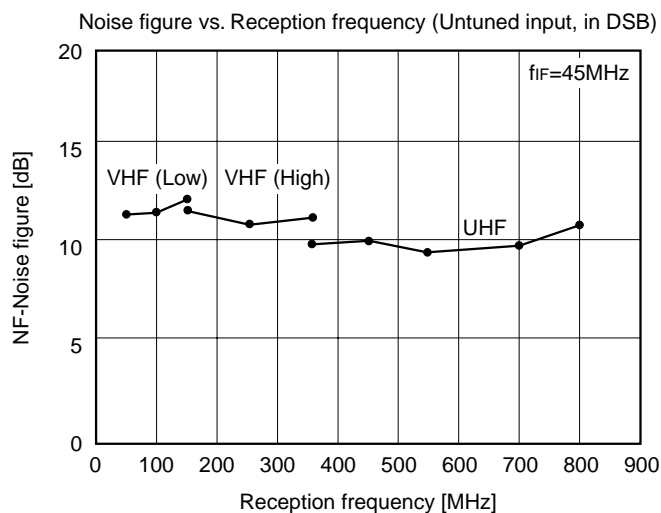
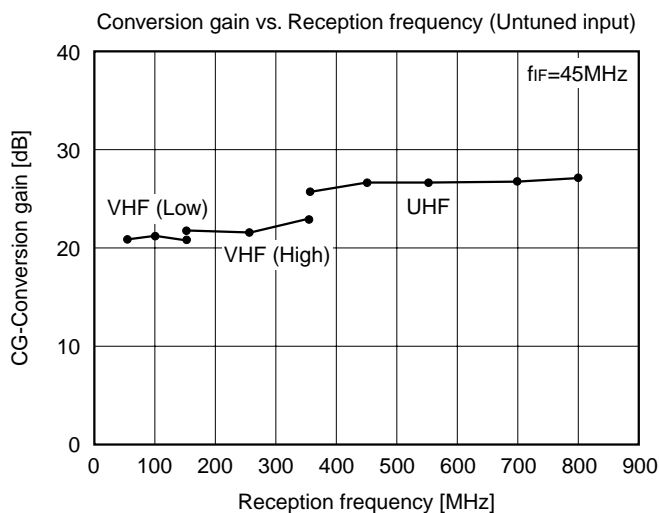
MA0, MA1 : address setting

FL : lock detection signal (1 : locked, 0 : unlocked)

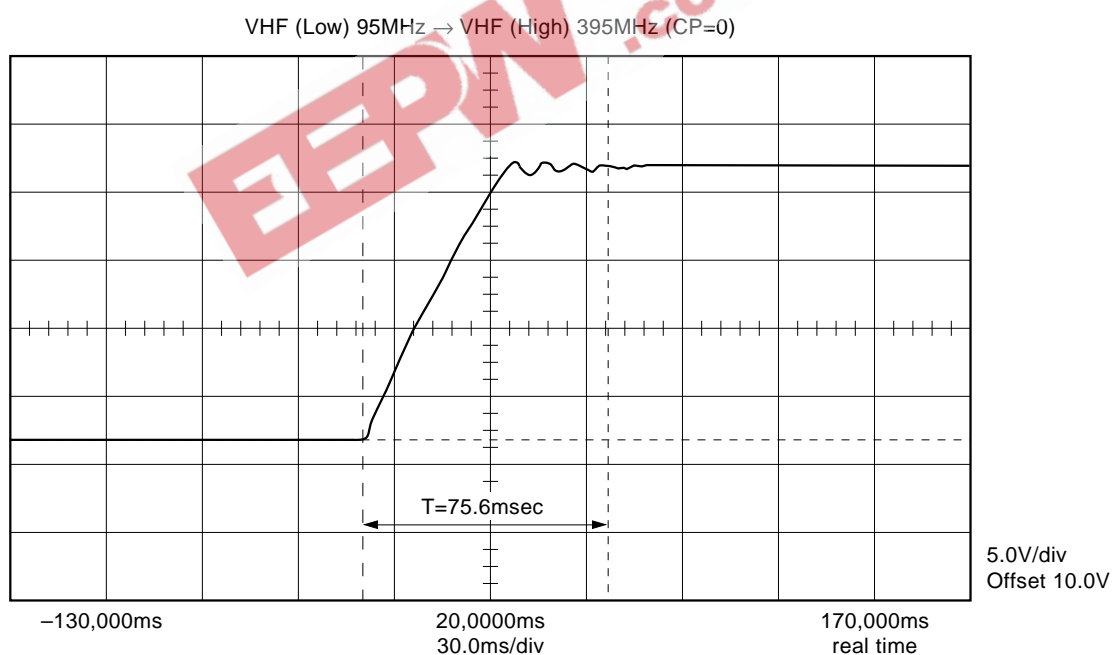
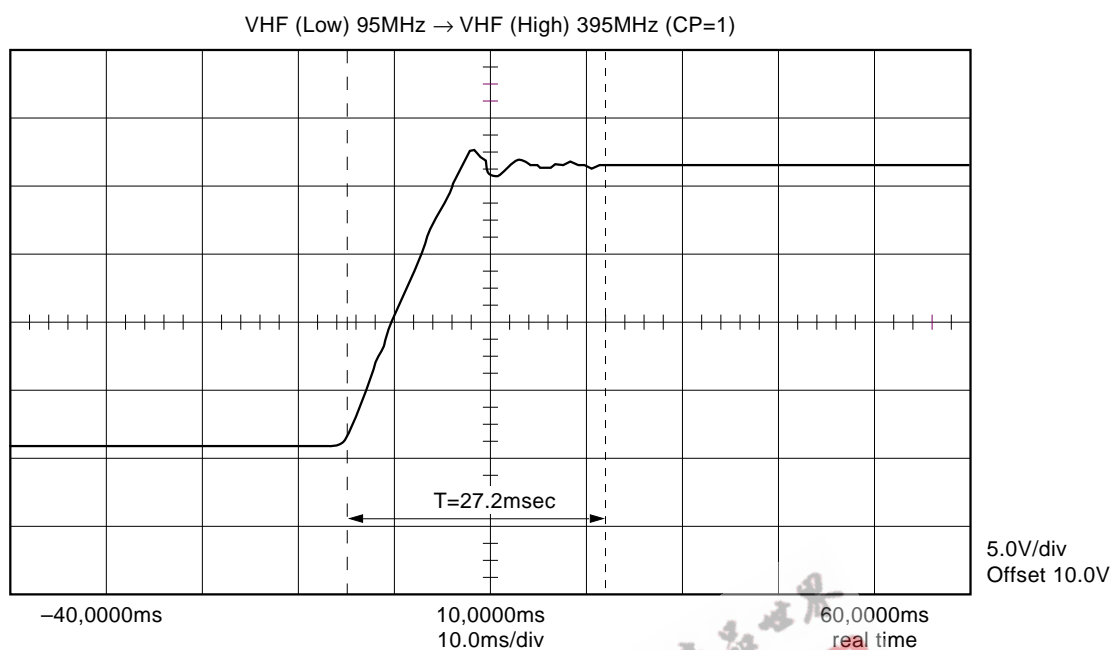
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## Example of Representative Characteristics



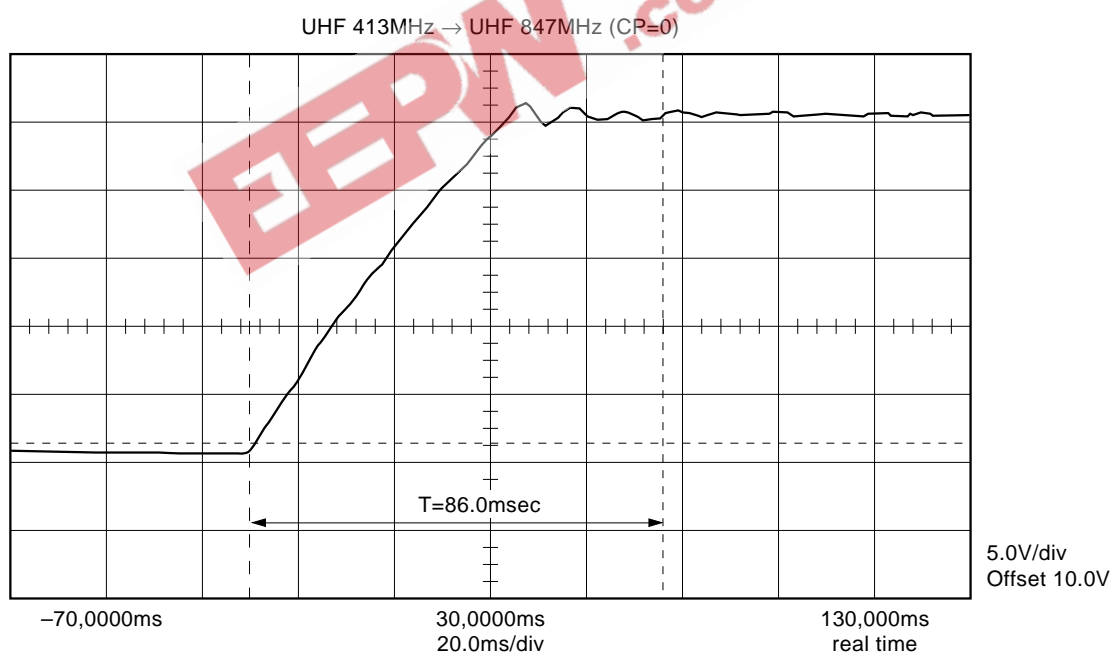
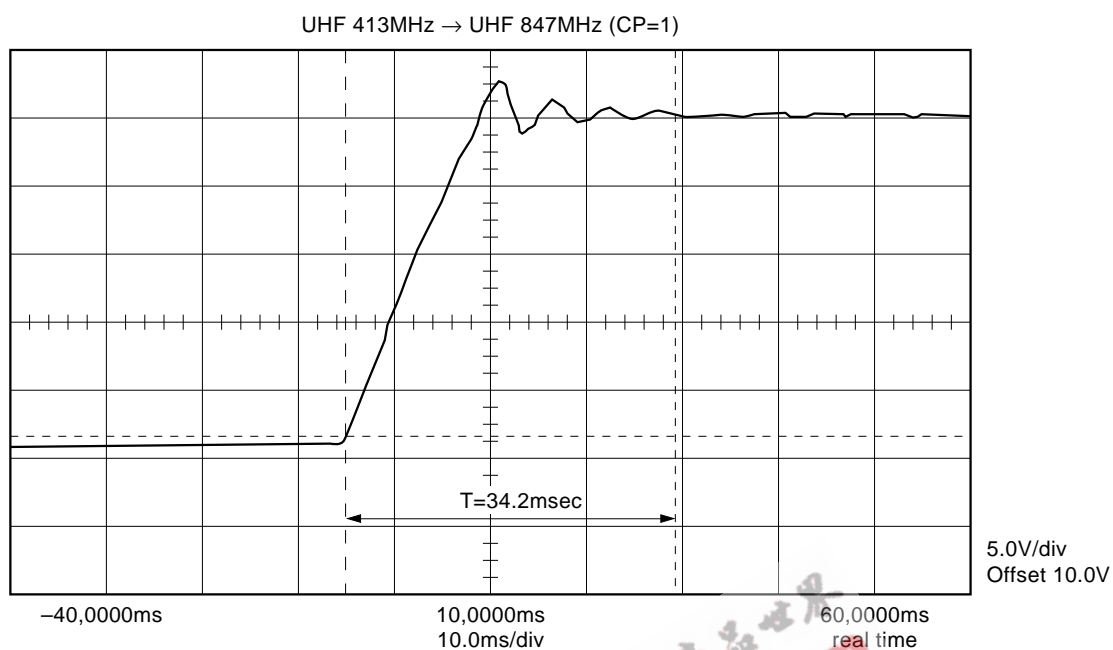


## Tuning Response Time 1

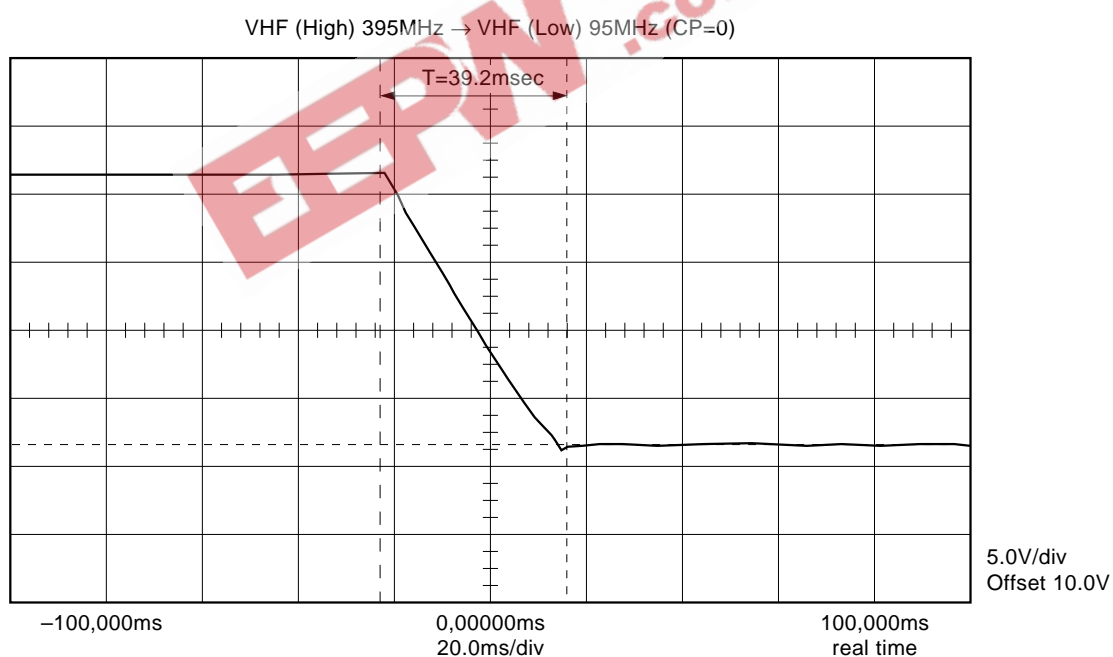
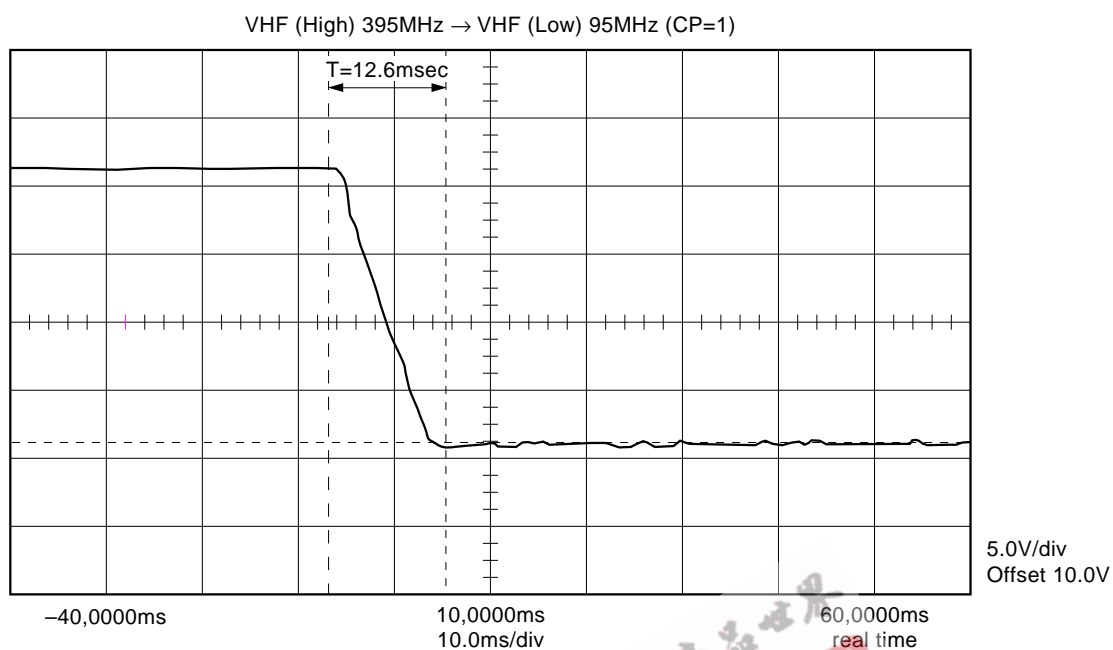




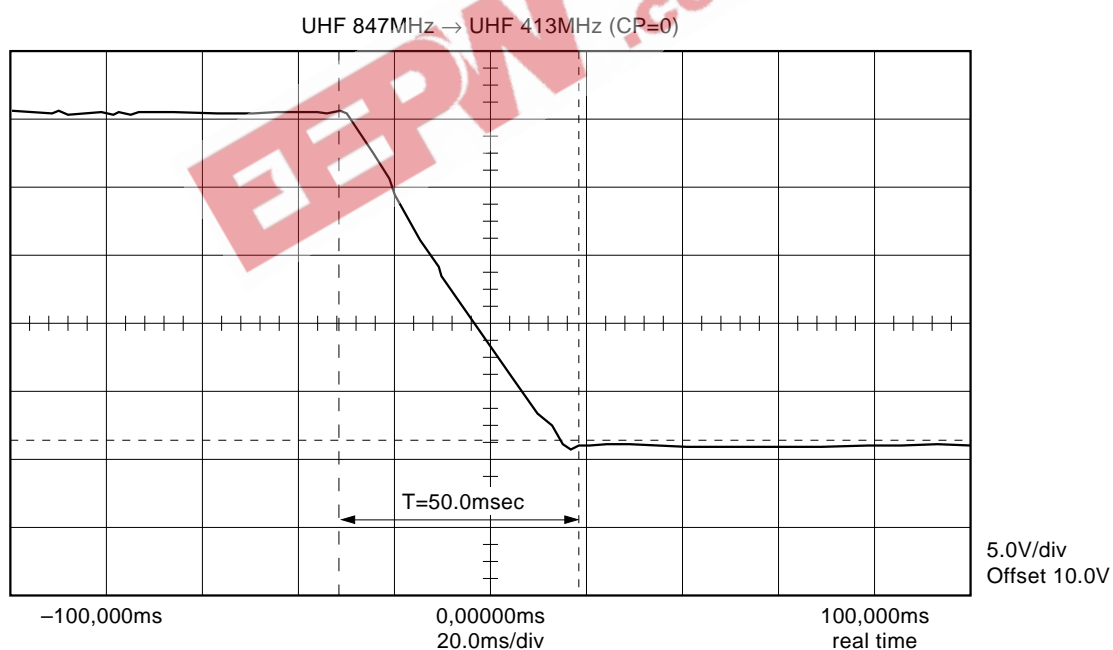
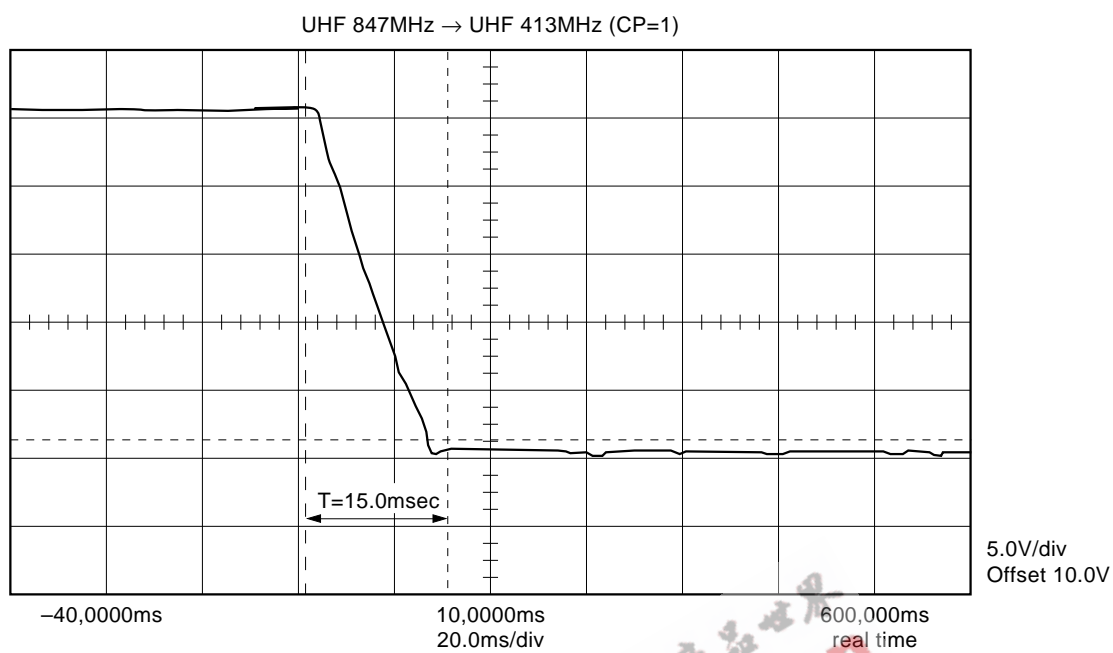
## Tuning Response Time 2



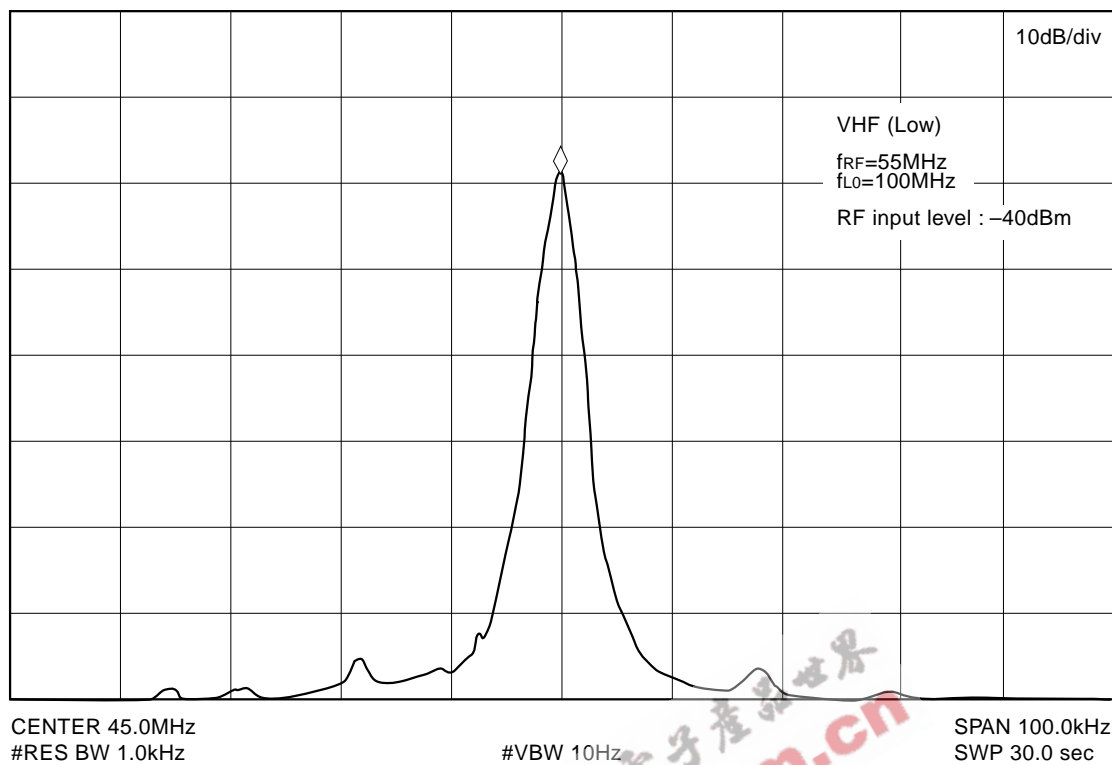
## Tuning Response Time 3



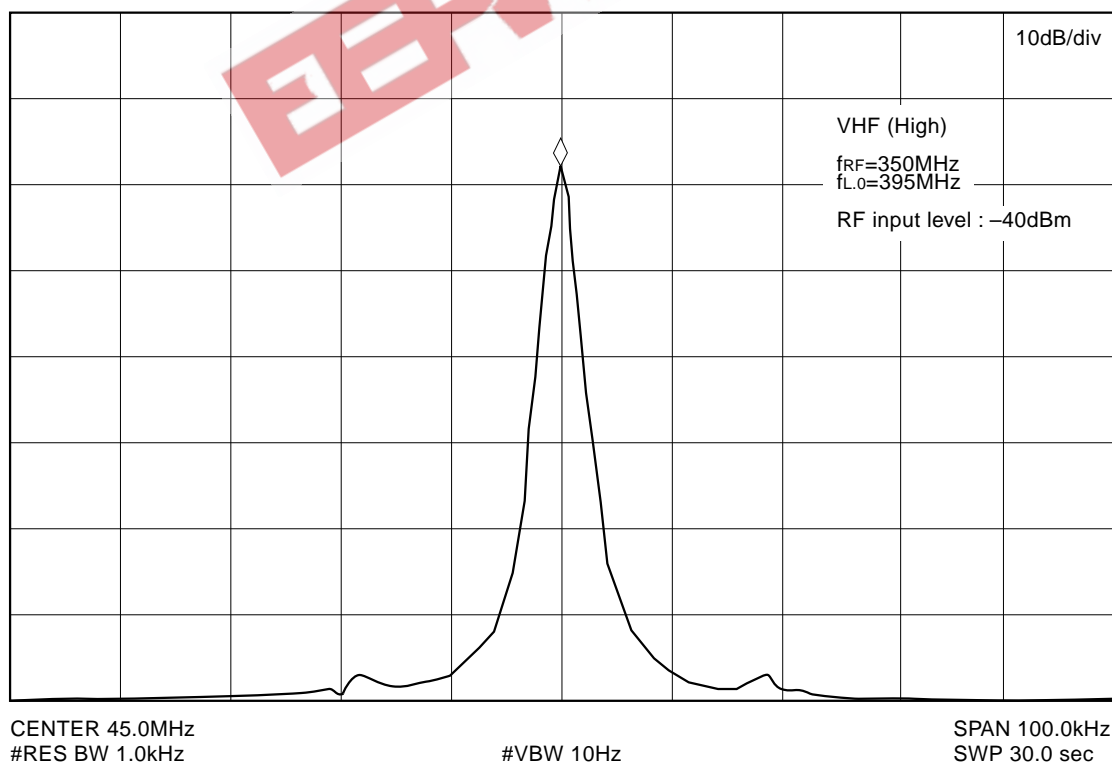
## Tuning Response Time 4

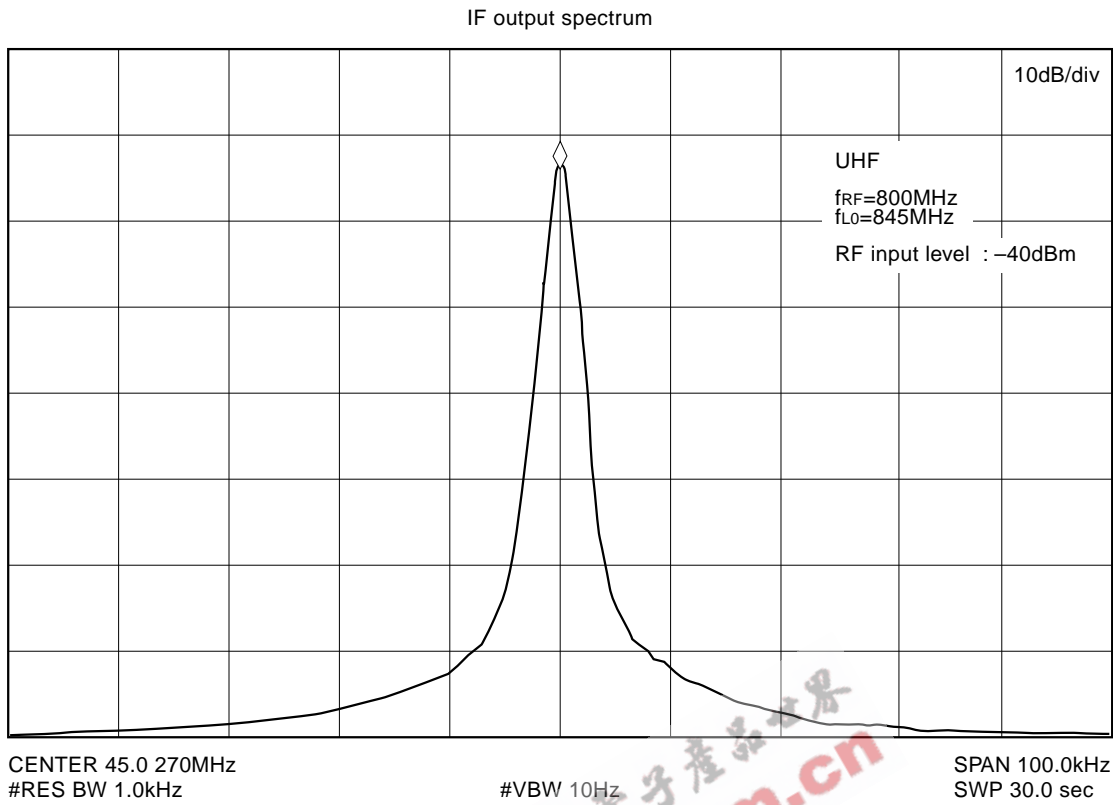


IF output spectrum

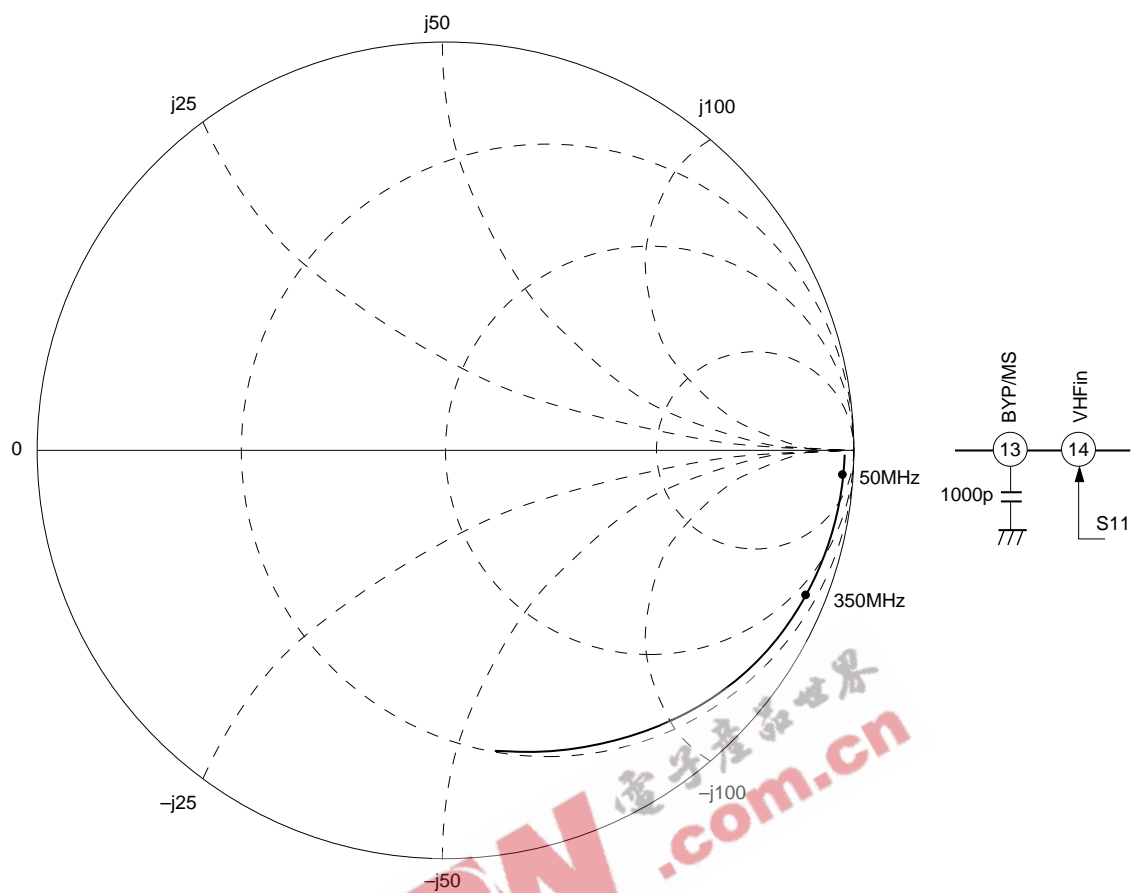


IF output spectrum

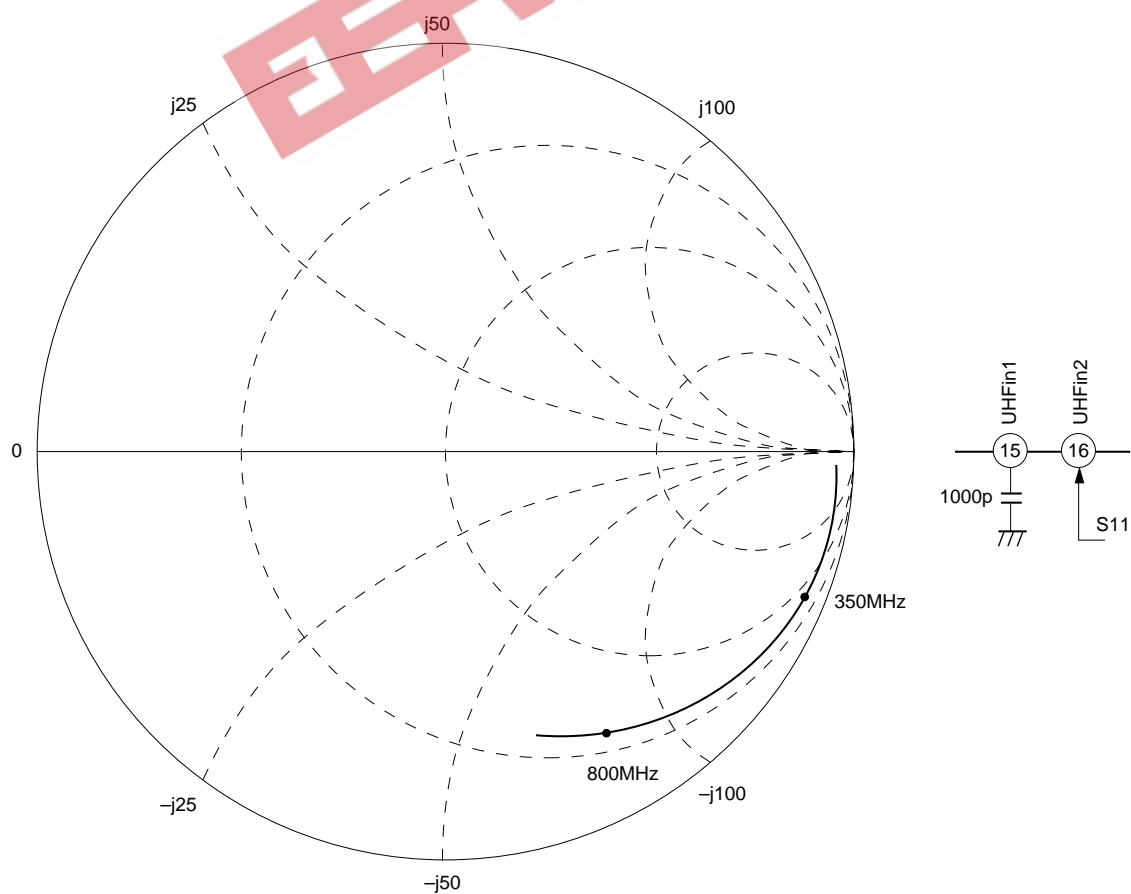




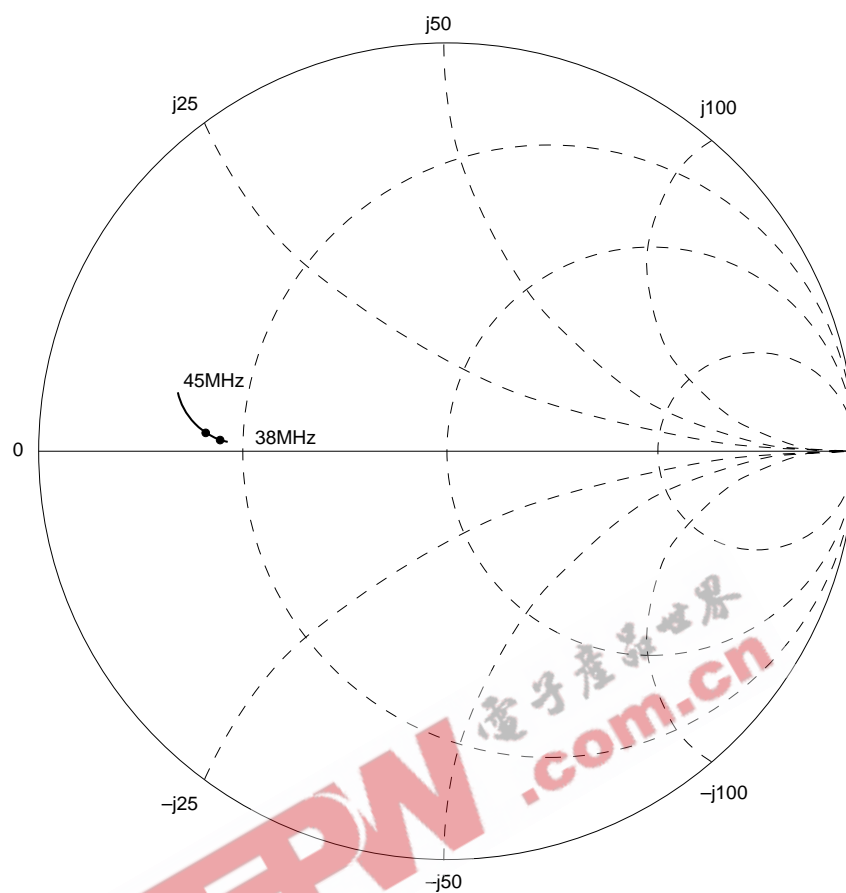
## VHF Input Impedance



## UHF Input Impedance

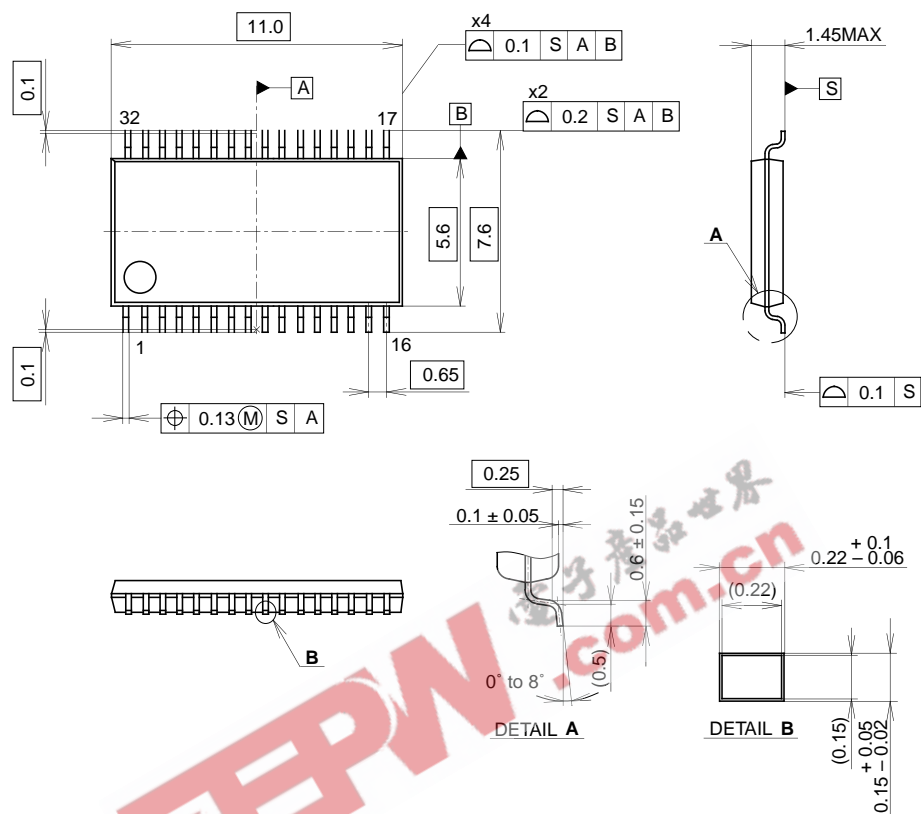


## IF Output Impedance



Package Outline    Unit : mm

32PIN SSOP(PLASTIC)



PACKAGE STRUCTURE

|            |                |
|------------|----------------|
| SONY CODE  | SSOP-32P-L01   |
| EIAJ CODE  | SSOP032-P-0056 |
| JEDEC CODE |                |

|                  |                   |
|------------------|-------------------|
| PACKAGE MATERIAL | EPOXY RESIN       |
| LEAD TREATMENT   | PALLADIUM PLATING |
| LEAD MATERIAL    | COPPER ALLOY      |
| PACKAGE MASS     | 0.1g              |