NEC Electronic U.S.A. Inc.
Electronic Arrays Division

NMOS
μPD2364

READ ONLY MEMORY 8192 WORDS, 8 BITS/WORD

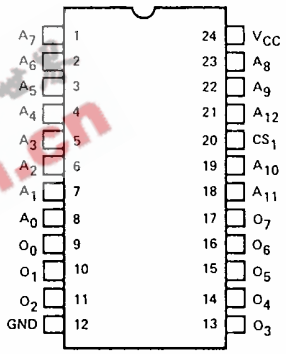
FEATURES:

- Three Fast Access Times
  -450nsec
  -350nsec
  -300nsec
- All Inputs and Outputs TTL Compatible
- Single +5V ± 10% Power Supply
- One Programmable Chip Select
- Three-State Outputs for Direct Bus Compatibility
- Pin Compatible to 2716, 2732, and 2564 EPROMS
- Fully Static Operation
- All Inputs Protected Against Static Charge
- 100% Burned-In

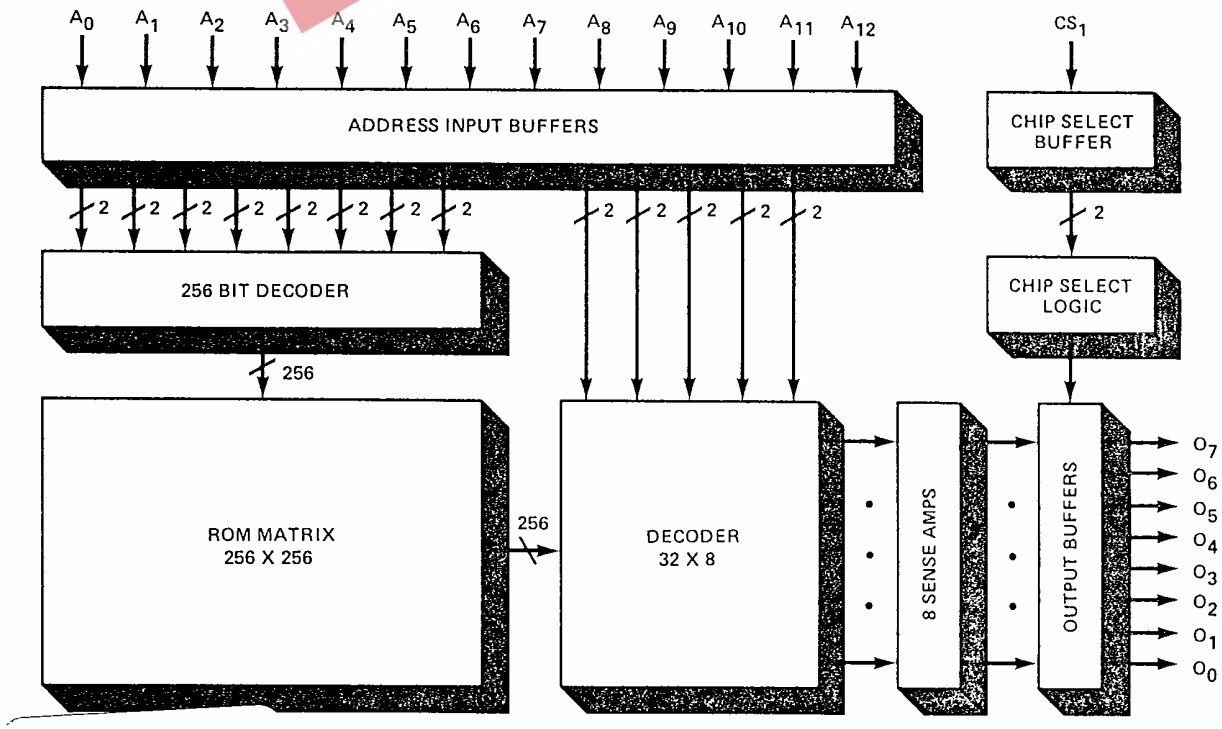
GENERAL DESCRIPTION:

The μPD2364 is a 65,536 bit Read Only Memory utilizing MOS N-Channel silicon gate technology. The device is completely static in operation, organized as 8192 words by 8 bits and operates from a single +5V power supply. All inputs and outputs are fully TTL compatible. It has one programmable chip select input and three-state outputs that allow memory expansion to 16,384 words by 8 bits without the use of external logic. Programming of the device is accomplished by a custom mask during fabrication. Pinout is compatible with 2716, 2732, and 2564 EPROMs.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



550 East Middlefield Road, Mountain View, CA 94043, Telephone (415) 964-4321, TWX 910-379-6985

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° to +70° C, V_{CC} = +5 ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input "Low" Voltage		−0.5		0.8	V
V_{IH}	Input "High" Voltage		2.0		V_{CC} + 1	V
I_{IL}	Input Load Current	V_{IN} = 0 to 5.5V			10	μA
V_{OL}	Output "Low" Voltage	I_{OL} = +2.1mA			0.4	V
V_{OH}	Output "High" Voltage	I_{OH} = −400μA	2.4			V
I_{LO}	Output Leakage Current	Chip Disabled V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Power Supply Current	All inputs +5.5V Output Disabled		80	140	mA

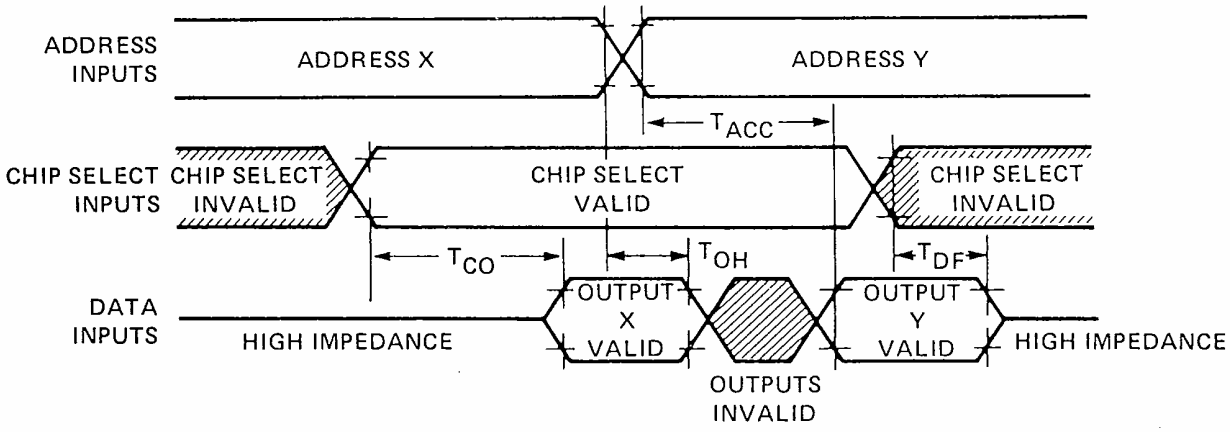
A.C. CHARACTERISTICS (T_a = 0° to +70° C, V_{CC} = +5 ± 10%)

		μPD2364-30		μPD2364-35		μPD2364-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{ACC}	Access Time		300		350		450	nsec
t_{CO}	Output Enable Time		120		150		150	nsec
t_{DF}	Output Disable Time		120		150		150	nsec
t_{OH}	Output Hold Delay	20		20		20		nsec
C_I	Input Capacitance		10		10		10	pf
C_O	Output Capacitance		15		15		15	pf

A.C. TEST CONDITIONS

Input rise and fall times (t_r, t_f) = 20 nsec
Timing Measurement Reference Levels:
Input and output high levels (V_{IH}, V_{OH}) = 2.0 Volts
Input and output low levels (V_{IL}, V_{OL}) = 0.8 Volts
Output load = 1 series 74 TTL + 100 pf

TIMING DIAGRAM



DEFINITIONS

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid Address and the corresponding valid Data Out.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an Address change that the previous data remains valid.

Output Enable Time, t_{CO}

Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Output Disable Time, t_{DF}

Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2764 EPROM
2. Two programmed 2732 EPROMs

BIT PATTERN VERIFICATIONS:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

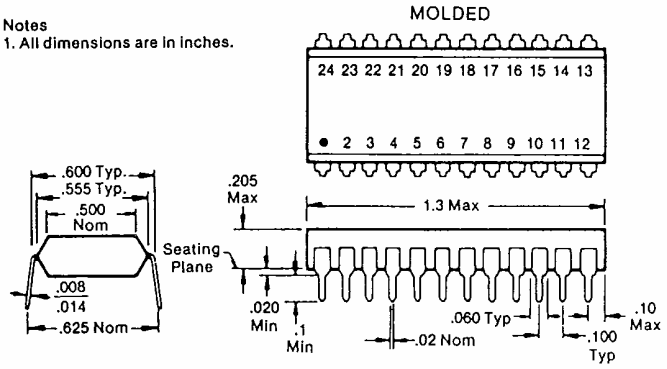
CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 2764 EPROM	Customer sends NEC one additional erased 2764. NEC programs the spare 2764 with the data from the programmed 2764, and returns to customer for verification.
2. Two programmed 2732 EPROMs	Customer sends NEC two additional erased 2732's. NEC programs the spare 2732's with the data from the programmed EPROMs and returns to customer for verification.

ORDERING INFORMATION

PART NUMBER INDUSTRIAL	ACCESS TIME	PACKAGE
μPD 2364-45PC	450nsec	Molded DIP
μPD 2364-35PC	350nsec	Molded DIP
μPD 2364-30PC	300nsec	Molded DIP

PHYSICAL DIMENSIONS

Notes
1. All dimensions are in inches.



Device also available in ceramic package.

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