

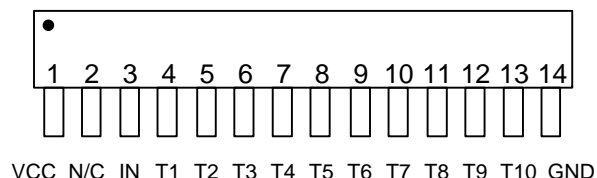
# 10-TAP, TTL-INTERFACED FIXED DELAY LINE (SERIES DDU224F)



## FEATURES

- Ten equally spaced outputs
- Very narrow device (SIP package)
- Stackable for PC board economy
- Input & outputs fully TTL interfaced & buffered
- 10 T<sup>2</sup>L fan-out capability

## PACKAGES



DDU224F-xx Commercial  
DDU224F-xxM Military

## FUNCTIONAL DESCRIPTION

The DDU224F-series device is a 10-tap digitally buffered delay line. The signal input (IN) is reproduced at the outputs (T1-T10), shifted in time by an amount determined by the device dash number. The nominal tap-to-tap delay increment is given by 1/10 of the dash number. For dash numbers less than 50, the total delay of the line is measured from T1 to T10, with the nominal value given by 9 times the increment. The inherent delay from IN to T1 is nominally 3.5ns. For dash numbers greater than or equal to 50, the total delay of the line is measured from IN to T10, with the nominal value given by the dash number.

## PIN DESCRIPTIONS

IN Signal Input  
T1-T10 Tap Outputs  
VCC +5 Volts  
GND Ground

## SERIES SPECIFICATIONS

- **Minimum input pulse width:** 20% of total delay
- **Output rise time:** 2ns typical
- **Supply voltage:** 5VDC  $\pm$  5%
- **Supply current:**  $I_{CCL}$  = 50ma typical  
 $I_{CCH}$  = 15ma typical
- **Operating temperature:** 0° to 70° C
- **Temp. coefficient of total delay:** 100 PPM/°C

## DASH NUMBER SPECIFICATIONS

Part Number	Total Delay (ns)	Delay Per Tap (ns)
DDU224F-10	9 $\pm$ 2.0 *	1.0 $\pm$ 0.5
DDU224F-20	18 $\pm$ 2.0 *	2.0 $\pm$ 1.0
DDU224F-25	22.5 $\pm$ 2.0 *	2.5 $\pm$ 1.0
DDU224F-50	50 $\pm$ 2.5	5.0 $\pm$ 2.0
DDU224F-100	100 $\pm$ 5.0	10.0 $\pm$ 3.0
DDU224F-150	150 $\pm$ 7.5	15.0 $\pm$ 3.0
DDU224F-200	200 $\pm$ 10.0	20.0 $\pm$ 3.0
DDU224F-250	250 $\pm$ 12.5	25.0 $\pm$ 3.0
DDU224F-300	300 $\pm$ 15.0	30.0 $\pm$ 3.0
DDU224F-400	400 $\pm$ 20.0	40.0 $\pm$ 4.0
DDU224F-500	500 $\pm$ 25.0	50.0 $\pm$ 5.0

\* Total delay is referenced to first tap output  
Input to first tap = 3.5ns  $\pm$  1ns

NOTE: Any dash number between 10 and 500 not shown is also available.

## APPLICATION NOTES

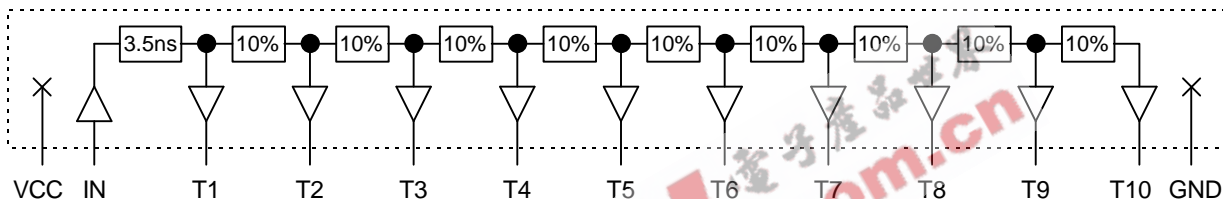
### HIGH FREQUENCY RESPONSE

The DDU224F tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 20% of the total delay and periods as small as 40% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data

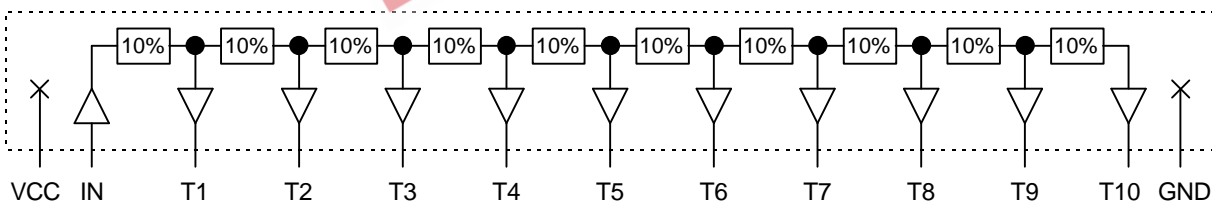
Delay Devices if your application requires device testing at a specific input condition.

### POWER SUPPLY BYPASSING

The DDU224F relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1 $\mu$ f capacitor from VCC to GND, located as close as possible to the VCC pin, is recommended. A wide VCC trace and a clean ground plane should be used.



Functional diagram for dash numbers < 50



Functional diagram for dash numbers  $\geq$  50

## DEVICE SPECIFICATIONS

**TABLE 1: ABSOLUTE MAXIMUM RATINGS**

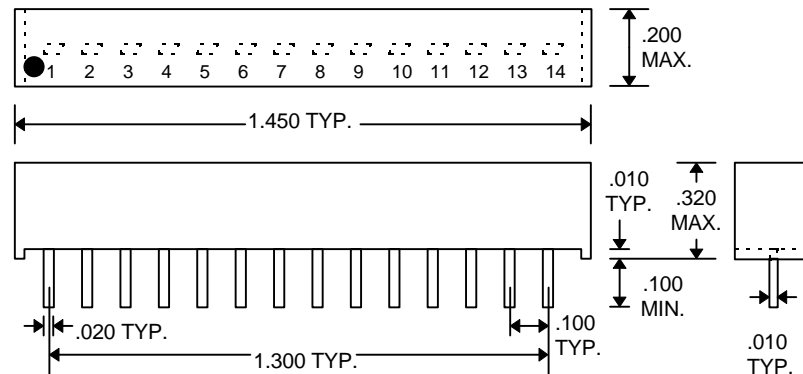
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	$V_{CC}$	-0.3	7.0	V	
Input Pin Voltage	$V_{IN}$	-0.3	$V_{DD}+0.3$	V	
Storage Temperature	$T_{STRG}$	-55	150	C	
Lead Temperature	$T_{LEAD}$		300	C	10 sec

**TABLE 2: DC ELECTRICAL CHARACTERISTICS**

(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	$V_{OH}$	2.5	3.4		V	$V_{CC} = \text{MIN}, I_{OH} = \text{MAX}$ $V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$
Low Level Output Voltage	$V_{OL}$		0.35	0.5	V	$V_{CC} = \text{MIN}, I_{OL} = \text{MAX}$ $V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$
High Level Output Current	$I_{OH}$			-1.0	mA	
Low Level Output Current	$I_{OL}$			20.0	mA	
High Level Input Voltage	$V_{IH}$	2.0			V	
Low Level Input Voltage	$V_{IL}$			0.8	V	
Input Clamp Voltage	$V_{IK}$			-1.2	V	$V_{CC} = \text{MIN}, I_I = I_{IK}$
Input Current at Maximum Input Voltage	$I_{IHH}$			0.1	mA	$V_{CC} = \text{MAX}, V_I = 7.0V$
High Level Input Current	$I_{IH}$			20	$\mu A$	$V_{CC} = \text{MAX}, V_I = 2.7V$
Low Level Input Current	$I_{IL}$			-0.6	mA	$V_{CC} = \text{MAX}, V_I = 0.5V$
Short-circuit Output Current	$I_{OS}$	-60		-150	mA	$V_{CC} = \text{MAX}$
Output High Fan-out				25	Unit	
Output Low Fan-out				12.5	Load	

## PACKAGE DIMENSIONS



**DDU224F-xx (Commercial)**  
**DDU224F-xxM (Military)**

## DELAY LINE AUTOMATED TESTING

### TEST CONDITIONS

**INPUT:**
**Ambient Temperature:**  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 
**Supply Voltage (Vcc):**  $5.0\text{V} \pm 0.1\text{V}$ 
**Input Pulse:** High =  $3.0\text{V} \pm 0.1\text{V}$   
 Low =  $0.0\text{V} \pm 0.1\text{V}$ 
**Source Impedance:**  $50\Omega$  Max.

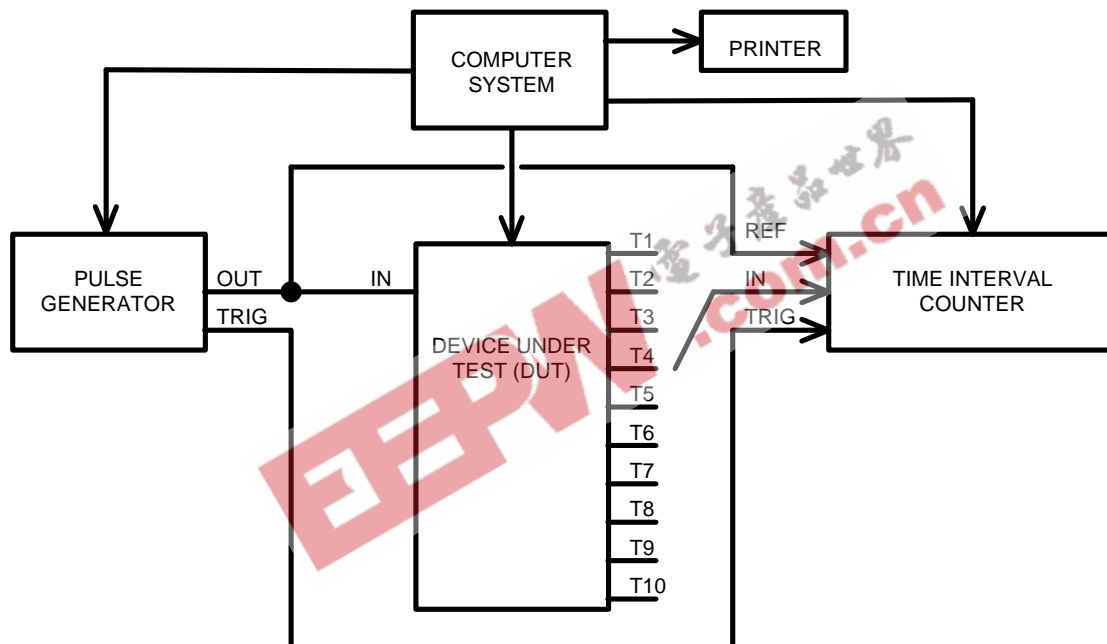
**Rise/Fall Time:** 3.0 ns Max. (measured  
 between 0.6V and 2.4V)

**Pulse Width:**  $\text{PW}_{\text{IN}} = 1.5 \times \text{Total Delay}$ 
**Period:**  $\text{PER}_{\text{IN}} = 10 \times \text{Total Delay}$ 
**OUTPUT:**
**Load:** 1 FAST-TTL Gate

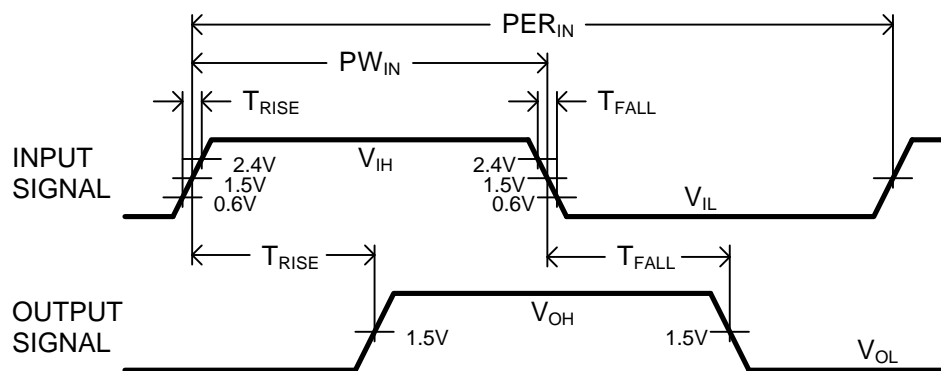
**C<sub>load</sub>:** 5pf  $\pm$  10%

**Threshold:** 1.5V (Rising & Falling)

**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.



**Test Setup**



**Timing Diagram For Testing**