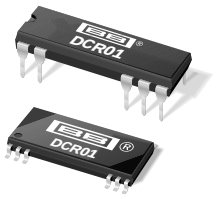
Burr-Brown Products from Texas Instruments



DCR01 Series

SBVS013C – OCTOBER 2001 – REVISED MAY 2003

Miniature, 1W Isolated REGULATED DC/DC CONVERTERS

FEATURES

- UL1950 RECOGNIZED
- DIP-18, SO-28
- 53W/in^3 (3.3W/cm^3) POWER DENSITY
- DEVICE-TO-DEVICE SYNCHRONIZATION
- THERMAL PROTECTION
- 1000Vrms ISOLATION
- 400kHz SWITCHING
- 125 FITS AT 55°C
- ±10% INPUT RANGE
- SHORT-CIRCUIT PROTECTED
- 5V, 12V, 24V INPUTS
- 3.3V, 5V OUTPUTS
- HIGH EFFICIENCY

APPLICATIONS

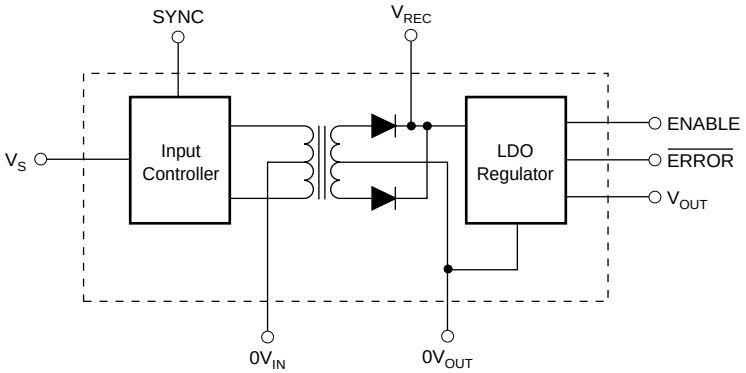
- POINT-OF-USE POWER CONVERSION
- DIGITAL INTERFACE POWER
- GROUND LOOP ELIMINATION
- POWER-SUPPLY NOISE REDUCTION

DESCRIPTION

The DCR01 family is a series of high-efficiency, input-isolated, output-regulated DC/DC converters. In addition to 1W nominal, galvanically-isolated output power capability, this range of DC/DCs offer very low output noise, thermal protection, and high accuracy.

The DCR01 family is implemented in standard molded IC packaging, giving standard JEDEC outlines suitable for high-volume assembly.

The DCR01 is manufactured using the same technology as standard IC packages, thereby achieving very high reliability.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Input Voltage:
- DCR0105 ..... 7V
- DCR0112 ..... 15V
- DCR0124 ..... 29V

Storage Temperature ..... –60°C to +125°C
Lead Temperature (soldering, 10s) ..... 270°C

ORDERING INFORMATION

DCR01 05 05 (P)

Basic Model Number: 1W Product
Voltage Input:
5V In
Voltage Output:
5V Out
Package Code:
P = 18-Pin Plastic DIP, U = 28-Pin SO

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DCR010503P	DIP-18	NVE	–40°C to +85°C	DCR010503P	DCR010503P	Rails, 20
DCR010503U	SO-28	DVB	–40°C to +85°C	DCR010503U	DCR010503U/1K	Tape and Reel, 1000
DCR010505P	DIP-18	NVE	–40°C to +85°C	DCR010505P	DCR010505P	Rails, 20
DCR010505U	SO-28	DVB	–40°C to +85°C	DCR010505U	DCR010505U/1K	Tape and Reel, 1000
DCR011203P	DIP18	NVE	–40°C to +85°C	DCR011203P	DCR011203P	Rails, 20
DCR011203U	SO-28	DVB	–40°C to +85°C	DCR011203U	DCR011203U/1K	Tape and Reel, 1000
DCR011205P	DIP-18	NVE	–40°C to +85°C	DCR011205P	DCR011205P	Rails, 20
DCR011205U	SO-28	DVB	–40°C to +85°C	DCR011205U	DCR011205U/1K	Tape and Reel, 1000
DCR012403P	DIP-18	NVE	–40°C to +85°C	DCR012403P	DCR012403P	Rails, 20
DCR012403U	SO-28	DVB	–40°C to +85°C	DCR012403U	DCR012403U/1K	Tape and Reel, 1000
DCR012405P	DIP-18	NVE	–40°C to +85°C	DCR012405P	DCR012405P	Rails, 20
DCR012405U	SO-28	DVB	–40°C to +85°C	DCR012405U	DCR012405U/1K	Tape and Reel, 1000

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = nominal, I_O = 10mA, C_O = 0.1µF, unless otherwise specified.

PARAMETER	CONDITIONS	DCR01 SERIES MIN	DCR01 SERIES TYP	DCR01 SERIES MAX	UNITS
OUTPUT					
Setpoint					
DCR010503			3.3		V
DCR010505			5		V
DCR011203			3.3		V
DCR011205			5		V
DCR012403			3.3		V
DCR012405			5		V
Setpoint Accuracy			0.5	2.0	%
Maximum Output Current					
DCR010503P		300			mA
DCR010503U		300			mA
DCR010505P		200			mA
DCR010505U		200			mA
DCR011203P		390			mA
DCR011203U		300			mA
DCR011205P		200			mA
DCR011205U		200			mA
DCR012403P		390			mA
DCR012403U		300			mA
DCR012405P		200			mA
DCR012405U		200			mA
Output Short-Circuit Protected	Duration		Infinite		
Line Regulation					
DCR010503			1		mV/V
DCR010505			1		mV/V
DCR011203			1		mV/V
DCR011205			1		mV/V
DCR012403			1		mV/V
DCR012405			1		mV/V
Over Line and Load					
DCR010503	10mA to 300mA Load, 4.5V to 5.5V Line		1.0	2.5	%
DCR010505	10mA to 200mA Load, 4.5V to 5.5V Line		1.0	2.5	%
DCR011203P	10mA to 390mA Load, 10.8V to 13.2V Line		1.0	2.5	%
DCR011203U	10mA to 300mA Load, 10.8V to 13.2V Line		1.0	2.5	%
DCR011205	10mA to 200mA Load, 10.8V to 13.2V Line		1.0	2.5	%
DCR012403P	10mA to 390mA Load, 21.6V to 26.4V Line		1.0	2.5	%
DCR012403U	10mA to 300mA Load, 21.6V to 26.4V Line		1.0	2.5	%
DCR012405	10mA to 200mA Load, 21.6V to 26.4V Line		1.0	2.5	%
Versus Temperature	–40°C to +85°C		1.0		%
Ripple and Noise					
DCR010503P Ripple	20MHz Bandwidth, 50% Load[1]		5		mVp-p
DCR010503P Noise	100MHz Bandwidth, 50% Load[1]		35		mVp-p
DCR010503U Ripple	20MHz Bandwidth, 50% Load[1]		8		mVp-p
DCR010503U Noise	100MHz Bandwidth, 50% Load[1]		23		mVp-p
DCR010505P Ripple	20MHz Bandwidth, 50% Load[1]		6		mVp-p
DCR010505P Noise	100MHz Bandwidth, 50% Load[1]		20		mVp-p
DCR010505U Ripple	20MHz Bandwidth, 50% Load[1]		9		mVp-p
DCR010505U Noise	100MHz Bandwidth, 50% Load[1]		20		mVp-p
DCR011203P Ripple	20MHz Bandwidth, 50% Load[1]		10		mVp-p
DCR011203P Noise	100MHz Bandwidth, 50% Load[1]		54		mVp-p
DCR011203U Ripple	20MHz Bandwidth, 50% Load[1]		8		mVp-p
DCR011203U Noise	100MHz Bandwidth, 50% Load[1]		22		mVp-p
DCR011205P Ripple	20MHz Bandwidth, 50% Load[1]		6		mVp-p
DCR011205P Noise	100MHz Bandwidth, 50% Load[1]		45		mVp-p
DCR011205U Ripple	20MHz Bandwidth, 50% Load[1]		6		mVp-p
DCR011205U Noise	100MHz Bandwidth, 50% Load[1]		21		mVp-p
DCR012403P Ripple	20MHz Bandwidth, 50% Load[1]		10		mVp-p
DCR012403P Noise	100MHz Bandwidth, 50% Load[1]		22		mVp-p
DCR012403U Ripple	20MHz Bandwidth, 50% Load[1]		8		mVp-p
DCR012403U Noise	100MHz Bandwidth, 50% Load[1]		22		mVp-p
DCR012405P Ripple	20MHz Bandwidth, 50% Load[1]		10		mVp-p
DCR012405P Noise	100MHz Bandwidth, 50% Load[1]		22		mVp-p
DCR012405U Ripple	20MHz Bandwidth, 50% Load[1]		13		mVp-p
DCR012405U Noise	100MHz Bandwidth, 50% Load[1]		32		mVp-p
INPUT					
Nominal Voltage (V_S)	DCR0105xx		5		V
	DCR0112xx		12		V
	DCR0124xx		24		V
Voltage Range		–10		+10	%

ELECTRICAL CHARACTERISTICS (Cont.)

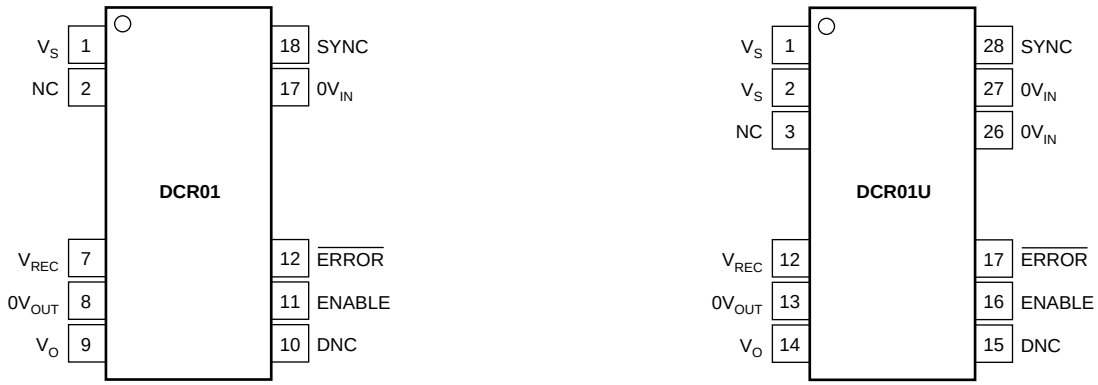
At T_A = +25°C, V_S = nominal, I_O = 10mA, C_O = 0.1µF, unless otherwise specified.

PARAMETER	CONDITIONS	DCR01 SERIES MIN	DCR01 SERIES TYP	DCR01 SERIES MAX	UNITS
Supply Current					
DCR010503P	I_O = 0mA		18		mA
	I_O = 10mA		28		mA
	I_O = 300mA		335		mA
DCR010503U	I_O = 0mA		24		mA
	I_O = 10mA		33		mA
	I_O = 300mA		339		mA
DCR010505P	I_O = 0mA		25		mA
	I_O = 10mA		40		mA
	I_O = 200mA		306		mA
DCR010505U	I_O = 0mA		25		mA
	I_O = 10mA		40		mA
	I_O = 200mA		306		mA
DCR011203P	I_O = 0mA		13		mA
	I_O = 10mA		17		mA
	I_O = 390mA		173		mA
DCR011203U	I_O = 0mA		13		mA
	I_O = 10mA		17		mA
	I_O = 390mA		136		mA
DCR011205P	I_O = 0mA		13		mA
	I_O = 10mA		18		mA
	I_O = 200mA		125		mA
DCR011205U	I_O = 0mA		14		mA
	I_O = 10mA		19		mA
	I_O = 200mA		123		mA
DCR012403P	I_O = 0mA		17		mA
	I_O = 10mA		18		mA
	I_O = 390mA		97		mA
DCR012403U	I_O = 0mA		15		mA
	I_O = 10mA		17		mA
	I_O = 390mA		75		mA
DCR012405P	I_O = 0mA		15		mA
	I_O = 10mA		18		mA
	I_O = 200mA		69		mA
DCR012405U	I_O = 0mA		15		mA
	I_O = 10mA		18		mA
	I_O = 200mA		67		mA
Reflected Ripple Current	20MHz Bandwidth, 100% Load C_{IN} = 2.2µF, C_{FILTER} = 1µF		8		mAp-p
ISOLATION					
Voltage	1s Flash Test	1			kVrms
	60s Test, UL1950[2]	1			kVrms
Input/Output Capacitance			25		pF
OUTPUT ENABLE CONTROL					
Logic High Input Voltage		2.0		V_{REC}	V
Logic High Input Current	2.0 < V_{ENABLE} < V_{REC}		100		nA
Logic Low Input Voltage		–0.2		0.5	V
Logic Low Input Current	0 < V_{ENABLE} < 0.5		100		nA
V_{REC}	All 3.3V Outputs		3.3		V
V_{REC}	All 5V Outputs		5		V
ERROR FLAG					
Logic High Open Collector Leakage	V_{ERROR} = 5V			10	µA
Logic Low Output Voltage	Sinking 2mA			0.4	V
THERMAL SHUTDOWN					
Junction Temperature					
Temperature Activated			150		°C
Temperature Deactivated			130		°C
SYNCHRONIZATION PIN					
Max External Capacitance on SYNC Pin				3	pF
Internal Oscillator Frequency		720	800	880	kHz
External Synchronization Frequency		720		880	kHz
External Synchronization Signal High		2.5	2.5	5.0	V
External Synchronization Signal Low		0		0.4	V
TEMPERATURE RANGE					
Operating		–40		+85	°C

NOTES: (1) C_{IN} = 2.2µF, C_{FILTER} = 1µF, C_{OUT} = 0.1µF. (2) During UL approval only.

PIN CONFIGURATIONS

Top View **DIP** **SO**



PIN DEFINITION (DIP)

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input
2	NC	No Connection
7	V_{REC}	Rectified Output
8	$0V_{OUT}$	Output Ground
9	V_O	Voltage Output
10	DNC	Do Not Connect
11	ENABLE	Output Voltage Enable
12	$\overline{ERROR}$	Error Flag Active Low
17	$0V_{IN}$	Input Ground
18	SYNC	Synchronization Input

PIN DEFINITION (SO)

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input
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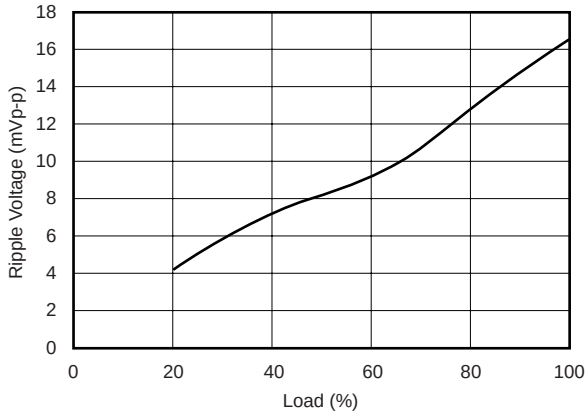
13	V_{OUT}	Output Ground
14	V_O	Voltage Output
15	DNC	Do Not Connect
16	ENABLE	Output Voltage Enable
17	$\overline{ERROR}$	Error Flag Active Low
26	$0V_{IN}$	Input Ground
27	$0V_{IN}$	Input Ground
28	SYNC	Synchronization Input

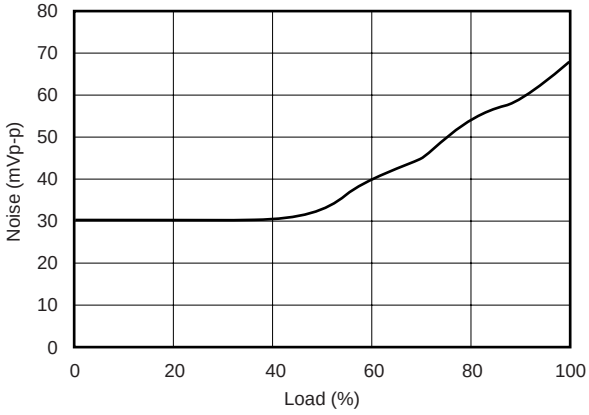
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 5V, I_O = 10mA, C_{FILTER} = 1µF, C_O = 0.1µF, unless otherwise specified.

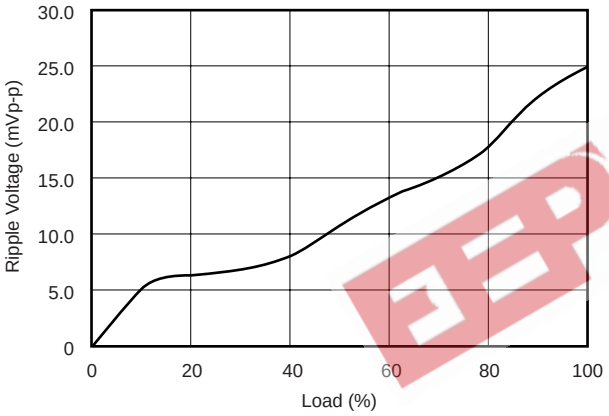
OUTPUT VOLTAGE RIPPLE
(all “U”, all 5V Output “P” Devices, and DCR010503P)



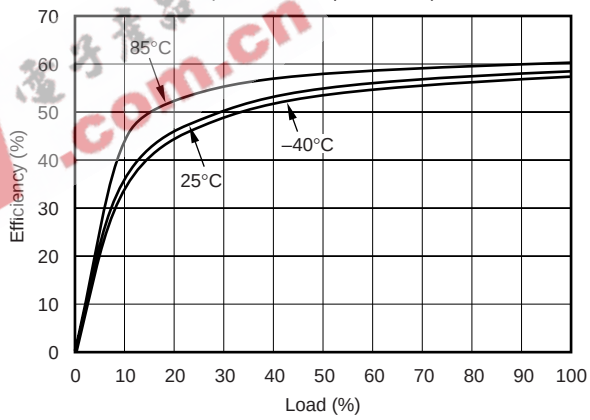
DCR0105 OUTPUT NOISE
(100MHz Bandwidth)



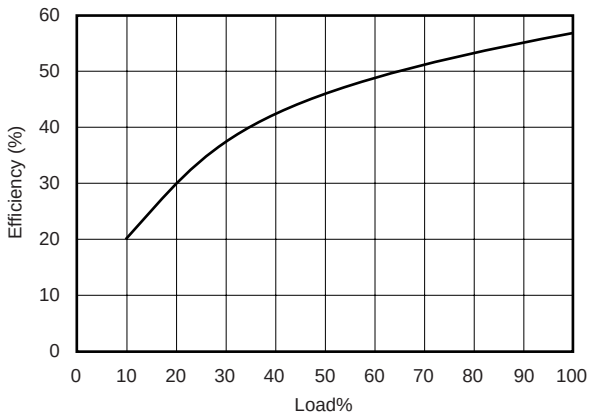
DCR011203P AND DCR012403P
OUTPUT VOLTAGE RIPPLE



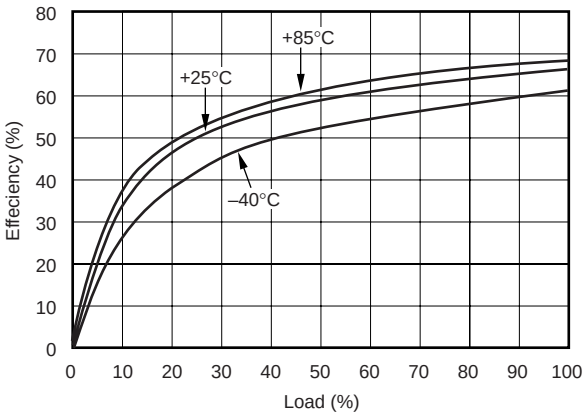
3V OUTPUT EFFICIENCY
(5V and 12V Input Devices)



DCR012403P AND U OUTPUT EFFICIENCY



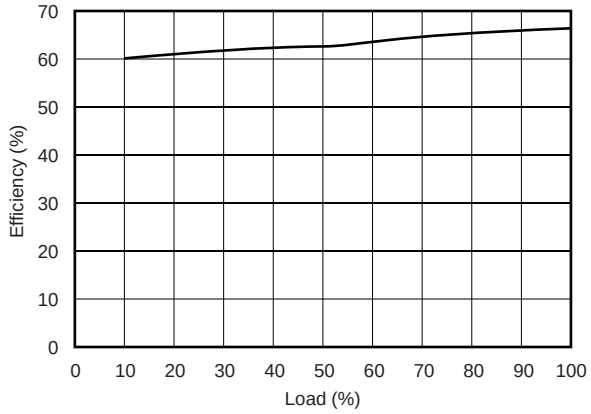
5V OUTPUT EFFICIENCY
(5V and 12V Input Devices.



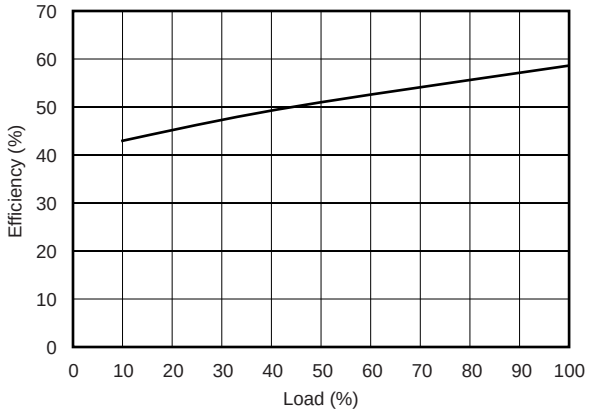
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, I_O = 10mA, C_{FILTER} = 1µF, C_O = 0.1µF, unless otherwise specified.

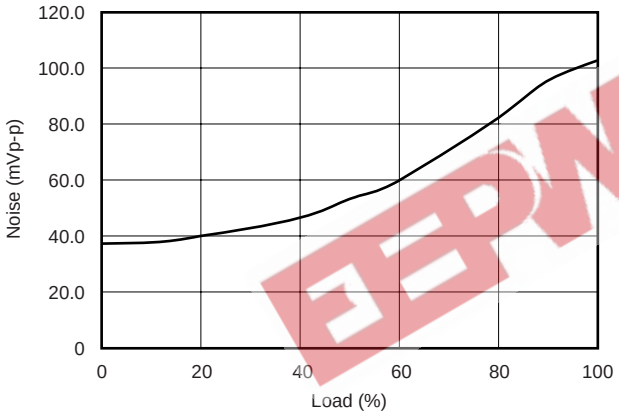
EFFICIENCY FOR 5V AND 12V INPUT
"U" DEVICES, 5V OUTPUT



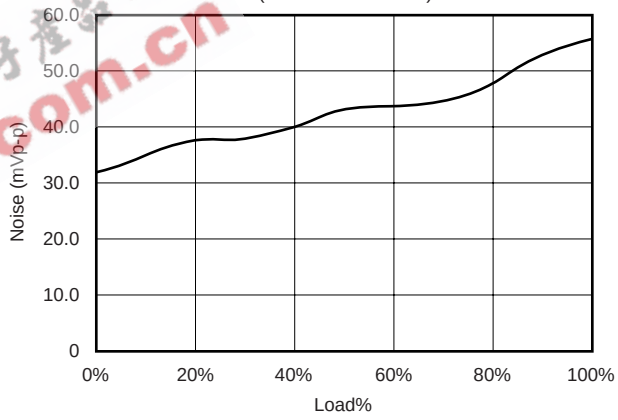
EFFICIENCY vs LOAD
DCR0112405 "P" and "U" DEVICES



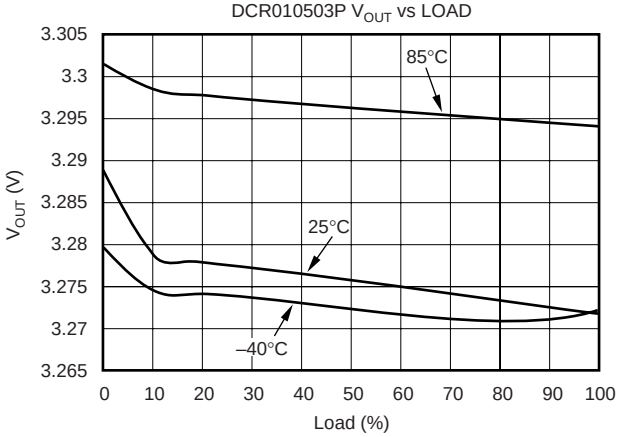
DCR011203P OUTPUT NOISE
(100MHz Bandwidth)



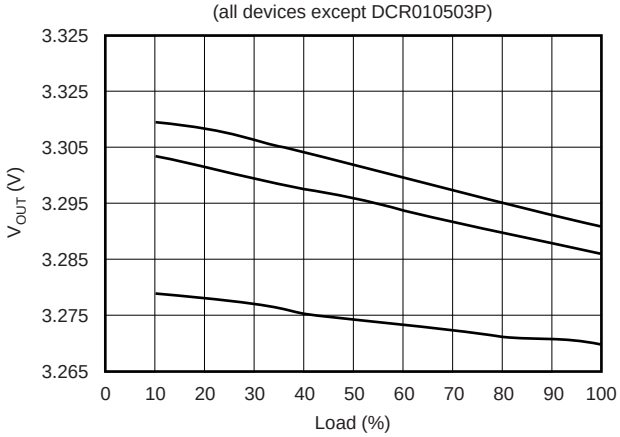
DCR011205P OUTPUT NOISE
(100MHz Bandwidth)



DCR010503P V_{OUT} vs LOAD



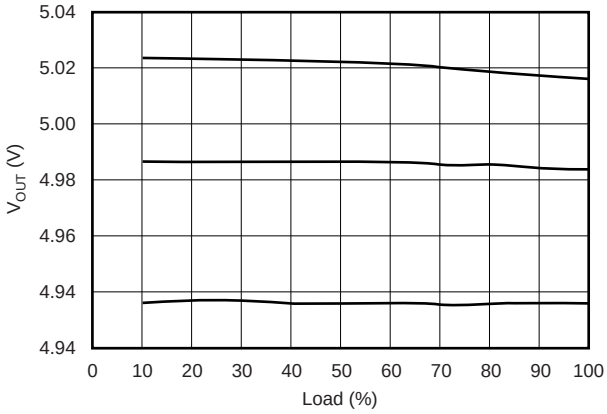
3V OUTPUT vs LOAD
(all devices except DCR010503P)



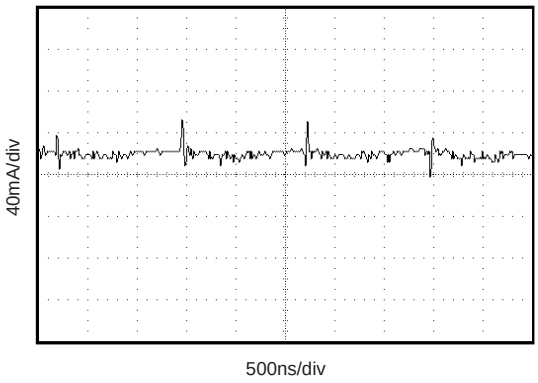
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, I_O = 10mA, C_{FILTER} = 1µF, C_O = 0.1µF, unless otherwise specified.

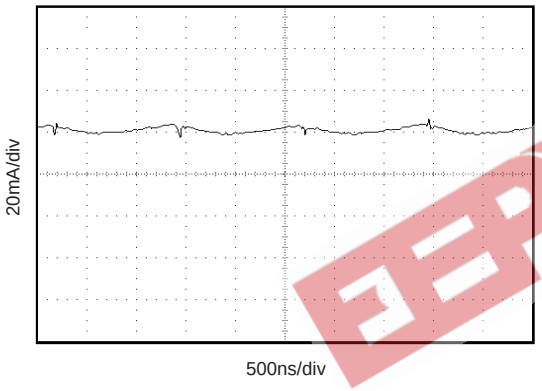
LOAD vs V_{OUT}
(for all 5V Output Devices)



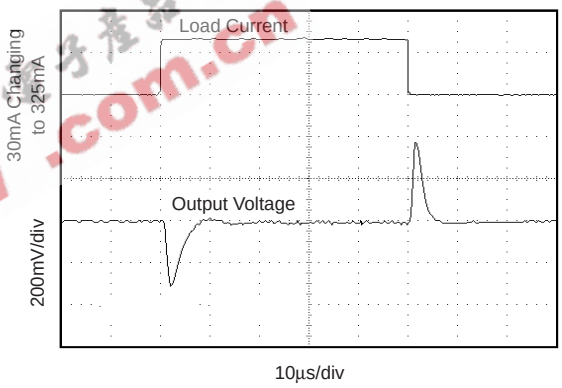
DCR0105 SERIES INPUT CURRENT
REFLECTED NOISE (100MHz Bandwidth)



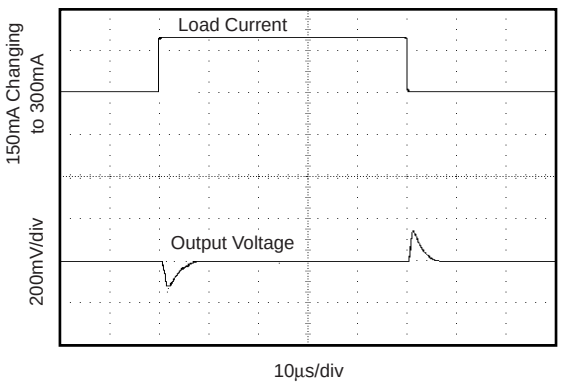
DCR01 SERIES INPUT
CURRENT REFLECTED RIPPLE



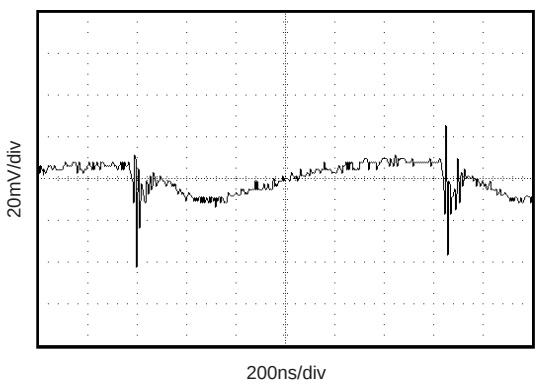
DCR010503P LOAD TRANSIENT RESPONSE



DCR010503P LOAD TRANSIENT RESPONSE



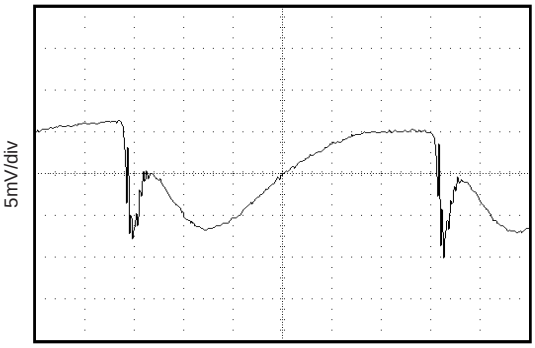
DCR010503P OUTPUT VOLTAGE NOISE
AT 100% LOAD (100MHz Bandwidth)



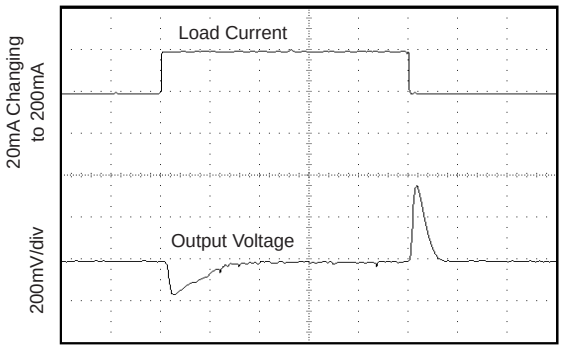
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, I_O = 10mA, C_{FILTER} = 1µF, C_O = 0.1µF, unless otherwise specified.

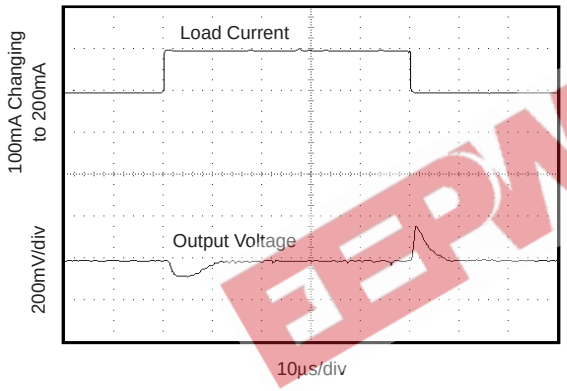
DCR010503P OUTPUT VOLTAGE RIPPLE
AT 100% LOAD (20MHz Bandwidth)



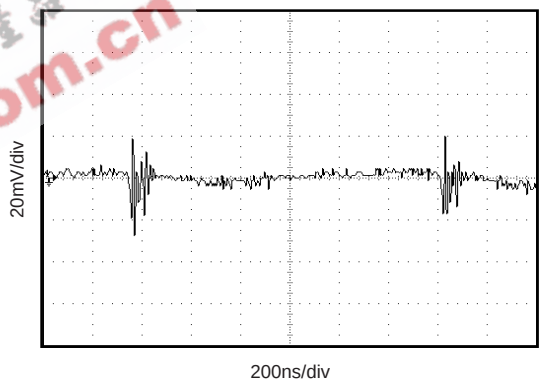
DCR010505P LOAD TRANSIENT RESPONSE



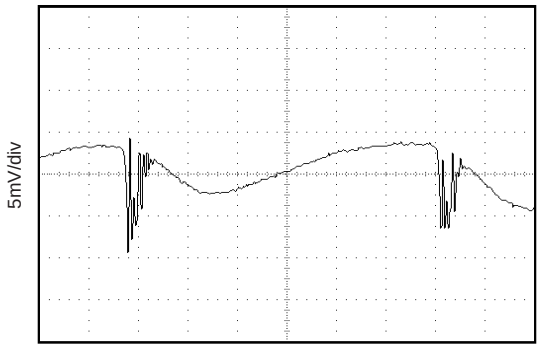
DCR010505P LOAD TRANSIENT RESPONSE



DCR010505P OUTPUT VOLTAGE NOISE
AT 100% LOAD (100MHz Bandwidth)



DCR010505P OUTPUT VOLTAGE RIPPLE
AT 100% LOAD (20MHz Bandwidth)



FUNCTIONAL DESCRIPTION

OVERVIEW

The DCR01 series offers isolation from an unregulated power supply operating from a choice of input voltages. The DCR01s provide a variety of regulated output voltages at a nominal output power of 1W or above.

POWER STAGE

The input supply is chopped at a frequency of 400kHz (internal oscillator divided by 2), which is used to drive the center-tapped toroidal transformer.

RECTIFICATION

The transformer's output is full wave rectified and smoothed by the external capacitor connected to V_{REC}.

REGULATOR

The internal low drop-out regulator provides a well-regulated output voltage, throughout the operating range of the device.

OSCILLATOR AND WATCHDOG

The DCR01 uses an internal saw-tooth generator to provide the 800kHz on-board oscillator that is used to drive the power switching circuit. The operation of the oscillator is monitored by the watchdog, which will tri-state the output driver circuit if the oscillator fails, or if the SYNC pin is taken LOW, (shutdown mode). When the SYNC pin is returned HIGH, normal operation resumes.

SYNCHRONIZATION

If more than one DCR01 is being used, beat frequencies and other electrical interference can be generated. This is due to the small variations in switching frequencies between the converters.

The DCR01 overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, with care being taken to minimize the capacitance of tracking.

Significant stray capacitance on the SYNC pin will have the effect of reducing the frequency of the internal oscillator. If this is large, the DCR01 may be taken outside its optimized operating parameters, and saturation of the magnetics may result, damaging the device.

If devices are synchronized, it should be noted that all devices will draw maximum current simultaneously at start up. This can cause the input voltage to dip. Should it fall below the minimum input voltage, the devices may not start up. A 2.2µF capacitor (low ESR) should be connected as close to the device input pins as possible for the 5V input devices, and a 0.47µF capacitor for the 12V and 24V devices.

If more than eight devices are required to be synchronized, it is recommended that external synchronization be used. Details are contained in Texas Instruments Application Report literature number SBAA035 (AB-153) available at www.ti.com.

CONSTRUCTION

The DCR01 is manufactured using the same technology as standard IC packages. There is no substrate within the package. The DCR01 is constructed using a driver IC, low-dropout voltage regulator, rectifier diodes, and a wound magnetic toroid, all mounted on a leadframe. The DCR01 requires no special PCB assembly processing, as there is no solder within the package. The result is an isolated DC/DC converter with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCR01 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled LOW, the DCR01 will be disabled. The disable time depends upon the external loading. The internal disable function is implemented in 2µs. Removal of the pull down will enable the DCR01.

Capacitance loading on the SYNC pin should be minimized in order to prevent a reduction in the internal oscillator's frequency. See Application Report (SBAA035) "External Synchronization of the DCP01/02 Series of DC/DC Converters". This document contains information on how to null the effects of additional capacitance on the SYNC pin. The oscillator's frequency can be measured at V_{REC}, as this is the fundamental frequency of the ripple component.

OUTPUT ENABLE/DISABLE

The regulated output of the DCR01 can be disabled by pulling the ENABLE pin LOW (connect ENABLE to $0V_{OUT}$). Holding the ENABLE pin HIGH (connect ENABLE to V_{REC}) enables the regulated output voltage, thus allowing the output to be controlled from the isolated side, see Figure 1.

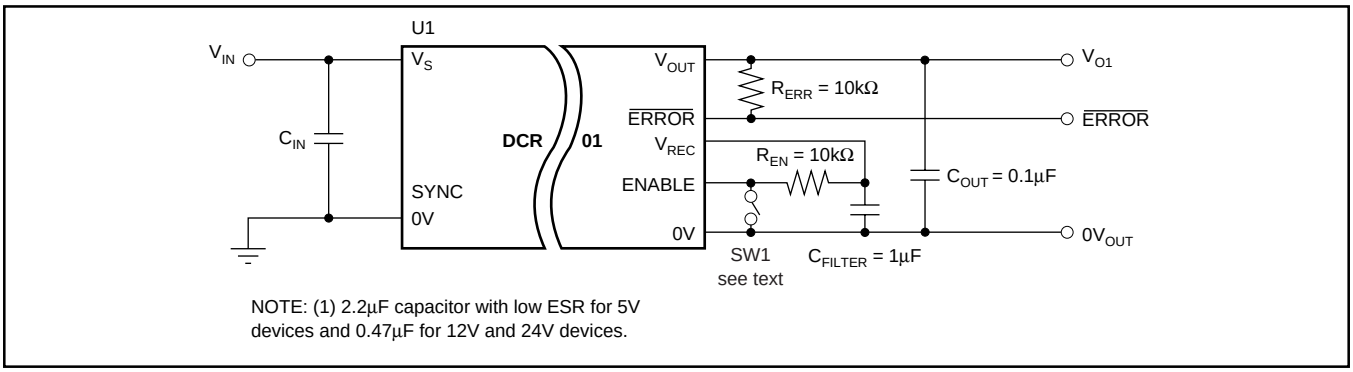


FIGURE 1. DCR01 with a Single Output.

$\overline{\text{ERROR}}$ FLAG

The DCR01 has an $\overline{\text{ERROR}}$ pin which provides a “power good” flag, as long as the internal regulator is in regulation.

DECOUPLING

Ripple Reduction

Due to the very low forward resistance of the DMOS switching transistors, high current demands are placed upon the input supply for a short time. By using a good quality low Equivalent Series Resistance (ESR) capacitor of 2.2µF (minimum) for the 5V input devices and a 0.47µF capacitor for the 12V and 24V devices, placed close to the IC supply input pins, the effects on the power supply can be minimized.

The high switching frequency of 400kHz allows relatively small values of capacitors to be used for filtering the rectified output voltage. A good quality low ESR capacitor of 1µF placed close to the V_{REC} pin and output ground will reduce the ripple.

It is not recommended that the DCR01 be fitted using an IC socket as this will degrade performance.

The output at V_{REC} is full wave rectified and produces a ripple of 800kHz.

It is recommended that a 0.1µF low ESR capacitor is connected close to the output pin and ground to reduce noise on the output. The capacitor values listed are minimum values. If lower ripple is required then the filter capacitor should be increased in value to 2.2µF.

NOTE: As with all switching power supplies the best performance is only obtained with low ESR capacitors connected close to the switcher. If low ESR capacitors are not used, the ESR will generate a voltage drop when the capacitor is supplying the load power. Often a larger capacitor is chosen for this purpose when a low ESR smaller capacitance would perform as well.

APPLICATION NOTES

DCR01 SINGLE VOLTAGE OUTPUT

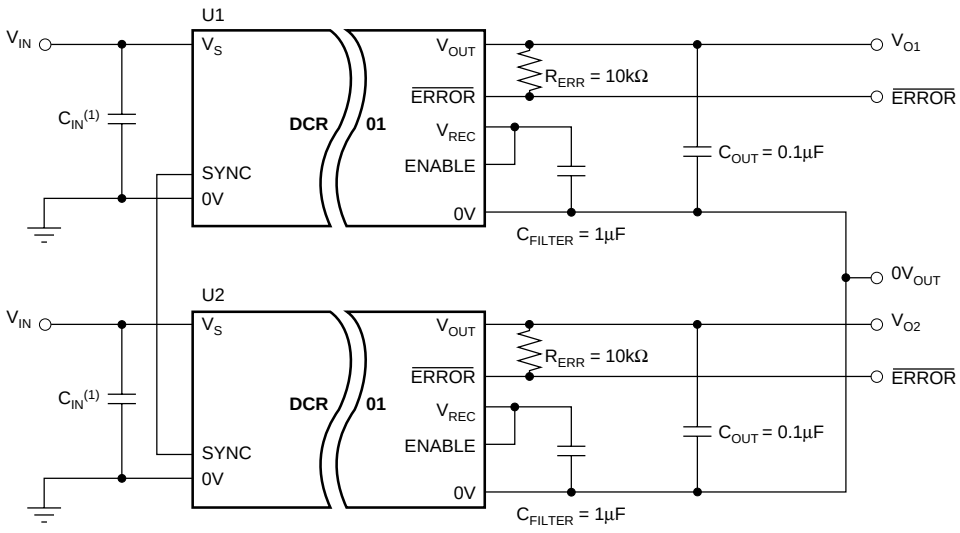
The DCR01 can be used to provide a single voltage output by connecting, see Figure 1. The $\overline{\text{ERROR}}$ output signal will be pulled up to the value of V_{OUT} for the particular DCR01 being used. The value of R_{ERR} will depend on the loading on the $\overline{\text{ERROR}}$ line however, the total load on the $\overline{\text{ERROR}}$ line must not exceed the value given in the specification.

The output may be permanently enabled by connecting the ENABLE pin to the V_{REC} pin. The DCR01 may be enabled remotely by connecting the ENABLE pin to V_{REC} via a pull-up resistor (R_{EN}), the value of this resistor is not critical for the DCR01 as only a small current flows. The switch SW1 can be used to pull the ENABLE pin LOW, thus disabling the output. The switching devices can be a bipolar transistor, FET or a mechanical device, the main load that it will see is R_{EN}.

GENERATING TWO POSITIVE OUTPUT VOLTAGES

Two DCR01s can be used to create output voltages of +3.3V and +5V, as shown in Figure 2. The two DCR01s are connected in self-synchronization, thus locking the oscillators of both devices to a single frequency.

The $\overline{\text{ERROR}}$ and ENABLE facilities may be used in a similar configuration for a single DCR01. The filter capacitors connected to the V_{REC} pins (C_{FILTER}), should be kept separate from each other and connected in close proximity to their respective DCR01. If similar output voltages are being used, it is not recommended that a single filter capacitor (with an increased capacitance) be used with both V_{REC} pins connected together, as this could result is the overloading of one of the devices.



NOTE: (1) 2.2µF capacitor with low ESR for 5V devices and 0.47µF for 12V and 24V devices.

FIGURE 2. Generating Two Positive Voltages from Self-Synchronized DCR01s.

GENERATION OF DUAL POLARITY VOLTAGES FROM TWO SELF-SYNCHRONIZED DCR01s

Two DCR01s can be configured to produce a dual polarity supply (i.e., ±5V); the circuit must be connected as shown in Figure 3.

It must be observed that both devices are producing a positive regulated output, therefore the $\overline{\text{ERROR}}$, ENABLE, and V_{REC} are all relative to that particular devices 0V and must not be directly connected together, or in the case of the negative output device connected to the common 0V output.

PCB LAYOUT

RIPPLE AND NOISE

Careful consideration should be given to the layout of the PCB in order for the best results to be obtained.

The DCR01 is a switching power supply and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to track the power to the input of DCR01 (this will also serve to reduce noise on the circuit). If this is not possible, the supplies must be connected in a star formation, with the tracks made as wide as possible.

If the SYNC pin is being used, the tracking between device SYNC pins should be short to avoid stray capacitance. If the SYNC pin is not being used it is advisable to place a guard ring (connected to input ground) around this pin to avoid any noise pick up.

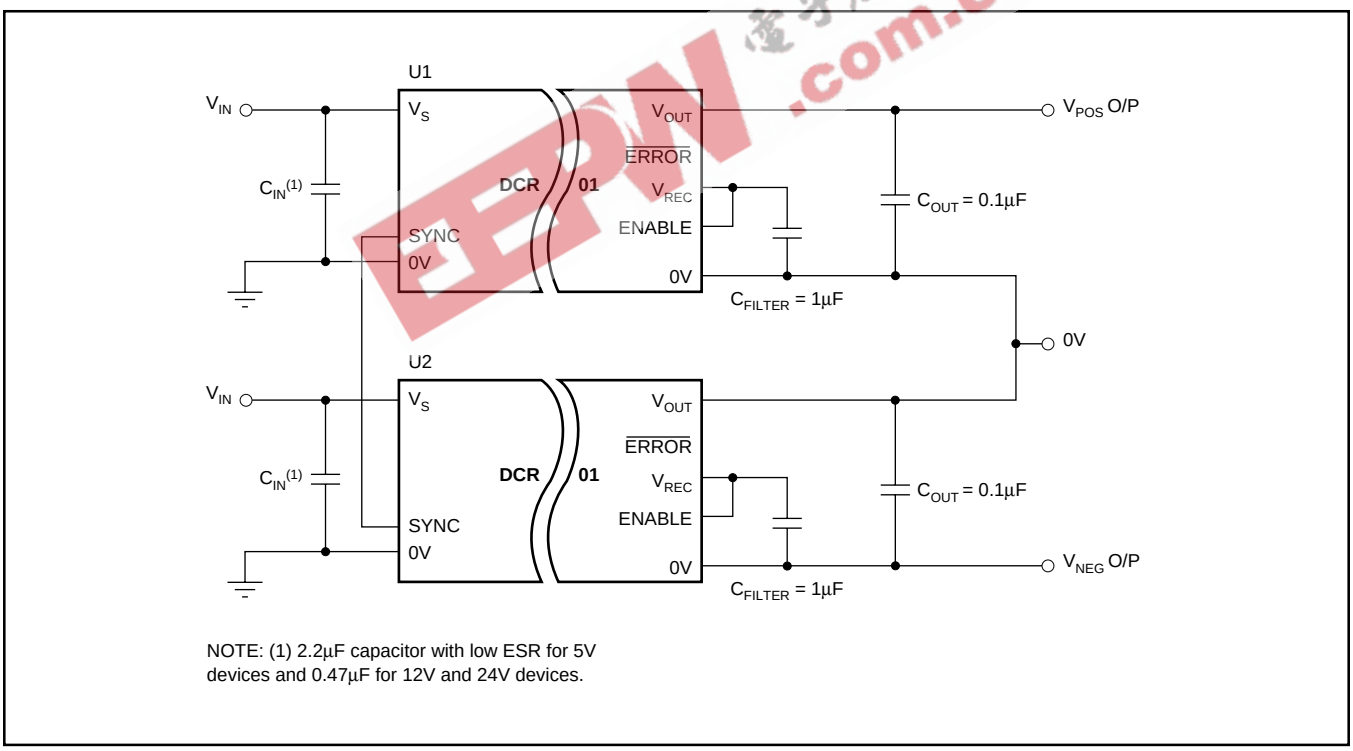
The output should be taken from the device using ground and power planes. This will ensure minimum losses.

A good quality low ESR capacitor placed as close as practicable across the input will reduce reflected ripple and ensure a smooth start up.

A good quality low ESR capacitor placed as close as practicable across the rectifier output terminal and output ground will give the best ripple and noise performance.

THERMAL MANAGEMENT

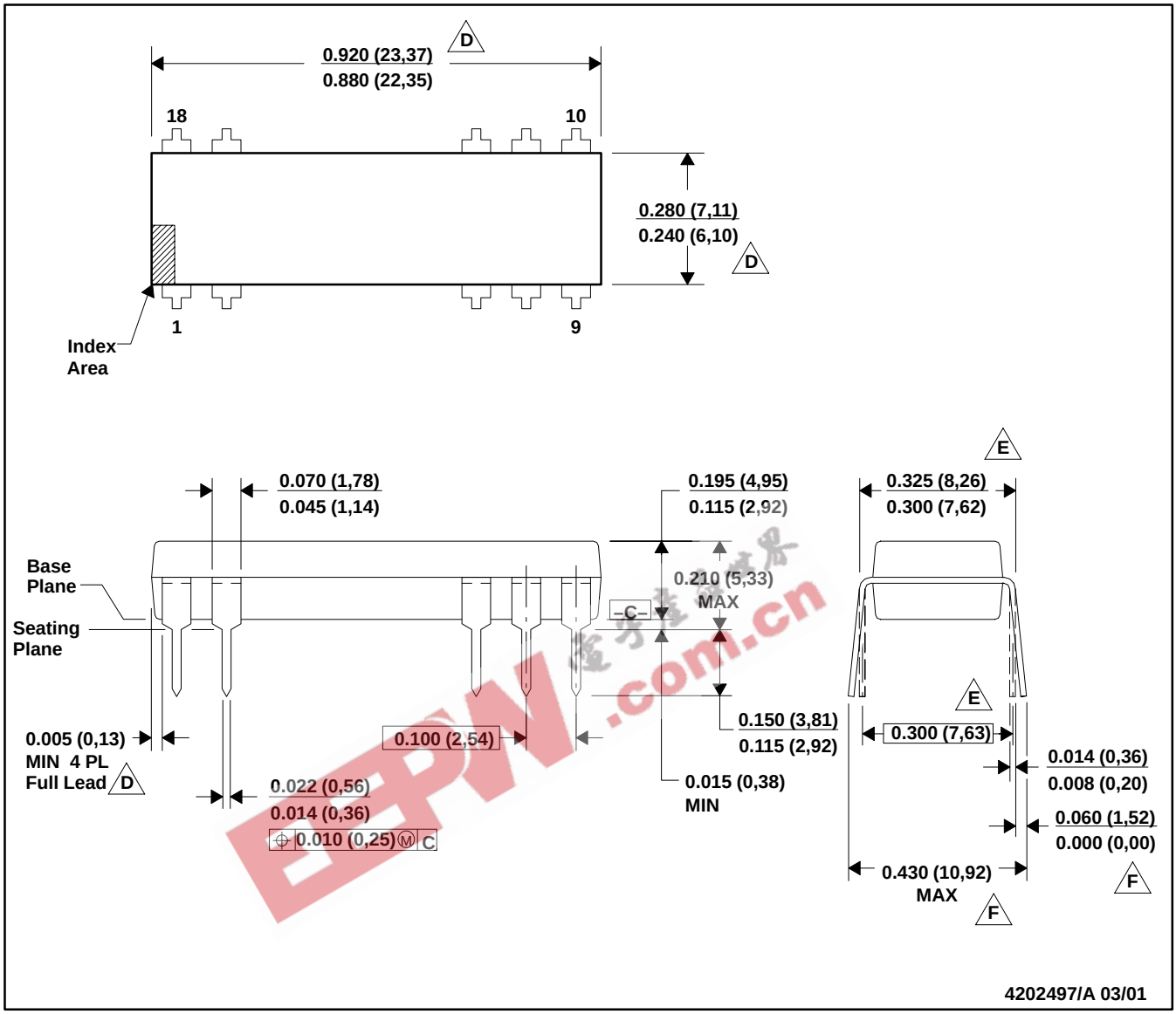
Due to the high power density of this device, it is advisable to provide a ground plane on the output. The output regulator is mounted on a copper leadframe, and a ground plane will serve as an efficient heatsink.



NOTE: (1) 2.2µF capacitor with low ESR for 5V devices and 0.47µF for 12V and 24V devices.

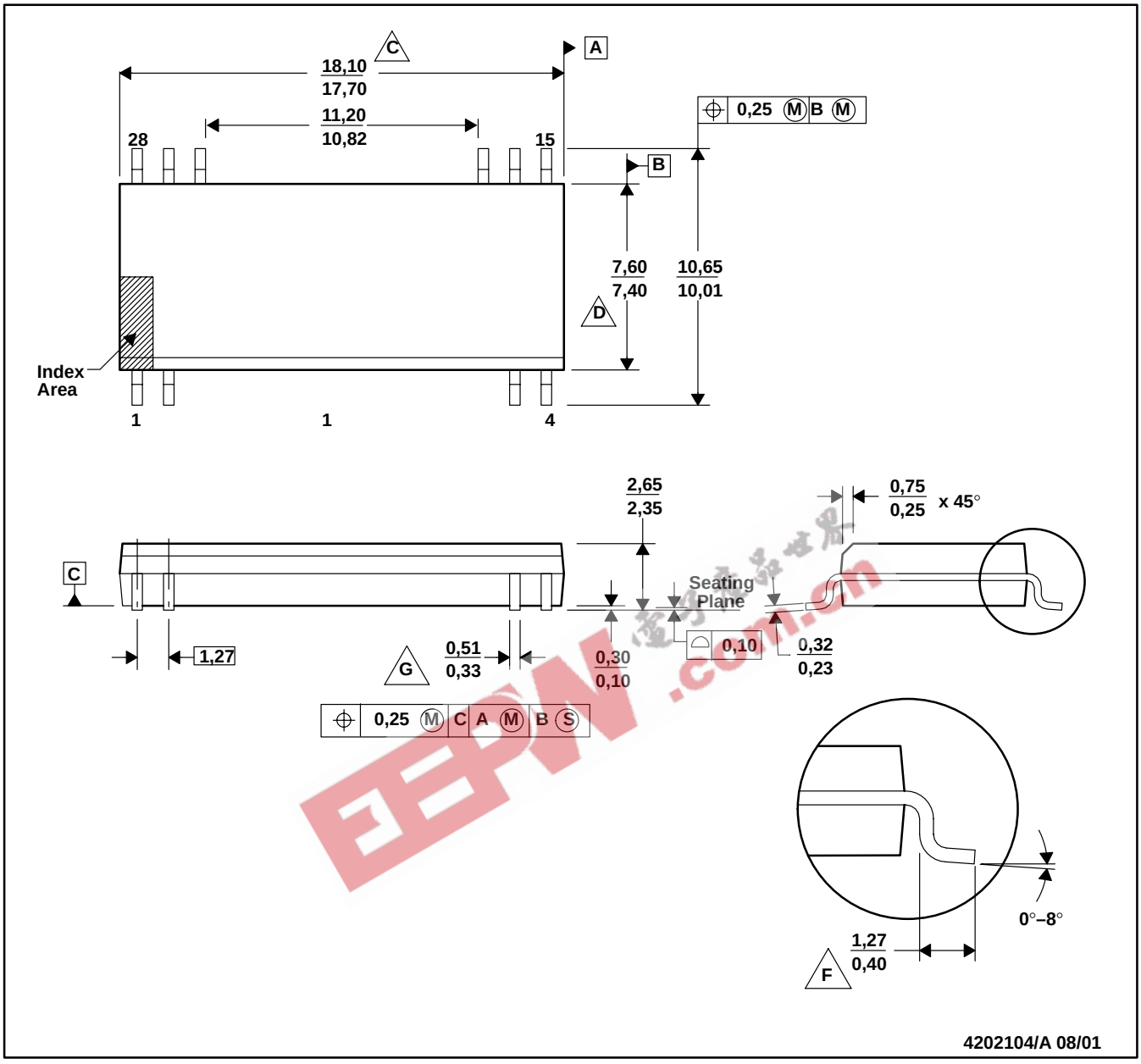
FIGURE 3. Dual Polarity Voltage Generation from Two Self-Synchronized DCR01's.

NVE (R-PDIP-T10/18) PLASTIC DUAL-IN-LINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-AC with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

DVB(R-PDSO-G12/28) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

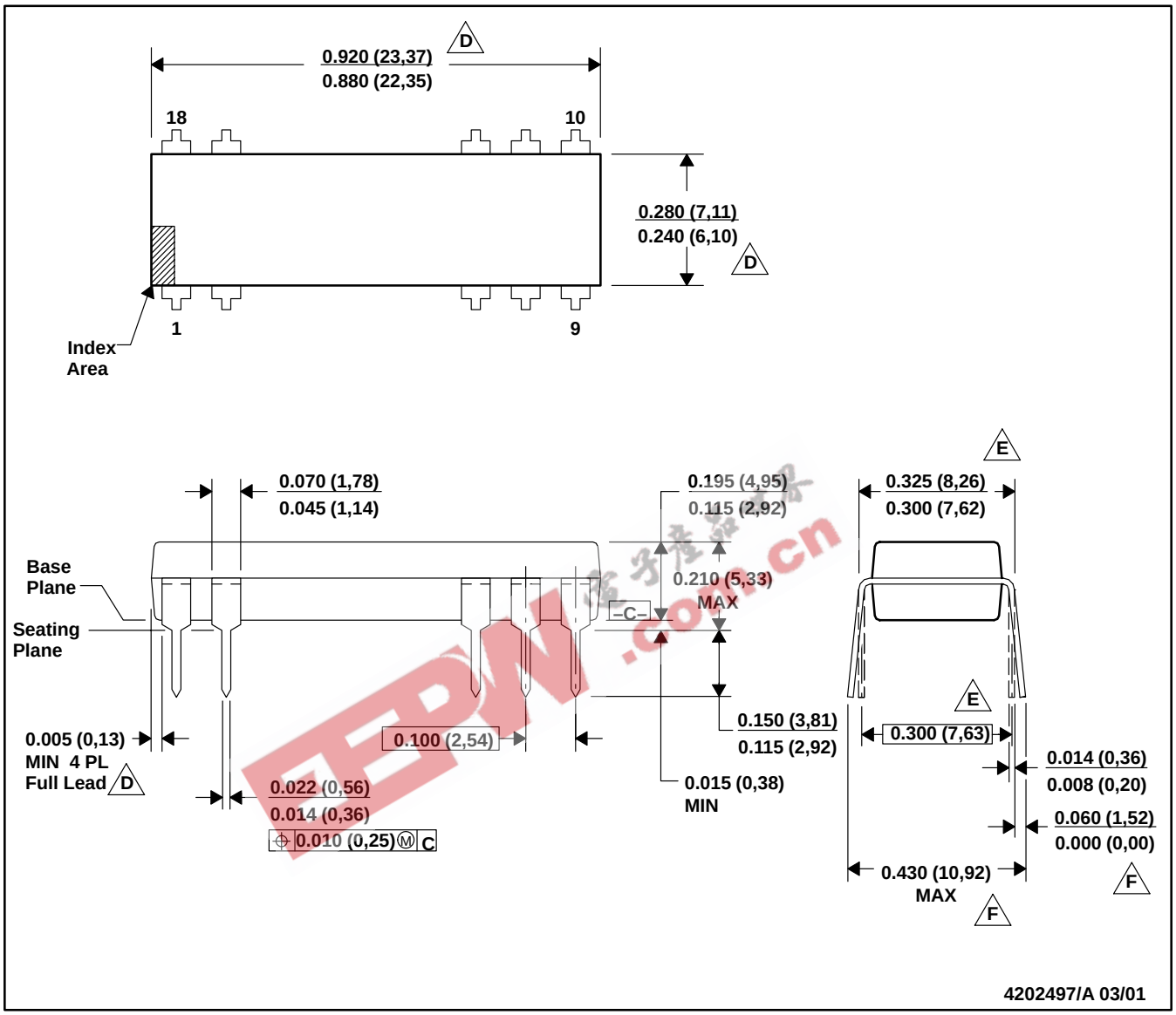
PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
DCR010503P	ACTIVE	PDIP	NVE	10	20
DCR010503U	ACTIVE	SOP	DVB	12	28
DCR010503U/1K	ACTIVE	SOP	DVB	12	1000
DCR010505P	ACTIVE	PDIP	NVE	10	20
DCR010505U	ACTIVE	SOP	DVB	12	28
DCR010505U/1K	ACTIVE	SOP	DVB	12	1000
DCR011203P	ACTIVE	PDIP	NVE	10	20
DCR011203U	ACTIVE	SOP	DVB	12	28
DCR011203U/1K	ACTIVE	SOP	DVB	12	1000
DCR011205P	ACTIVE	PDIP	NVE	10	20
DCR011205U	ACTIVE	SOP	DVB	12	28
DCR011205U/1K	ACTIVE	SOP	DVB	12	1000
DCR012403P	ACTIVE	PDIP	NVE	10	20
DCR012403U	ACTIVE	SOP	DVB	12	28
DCR012403U/1K	ACTIVE	SOP	DVB	12	1000
DCR012405P	ACTIVE	PDIP	NVE	10	20
DCR012405U	ACTIVE	SOP	DVB	12	28
DCR012405U/1K	ACTIVE	SOP	DVB	12	1000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

NVE (R-PDIP-T10/18) **PLASTIC DUAL-IN-LINE**



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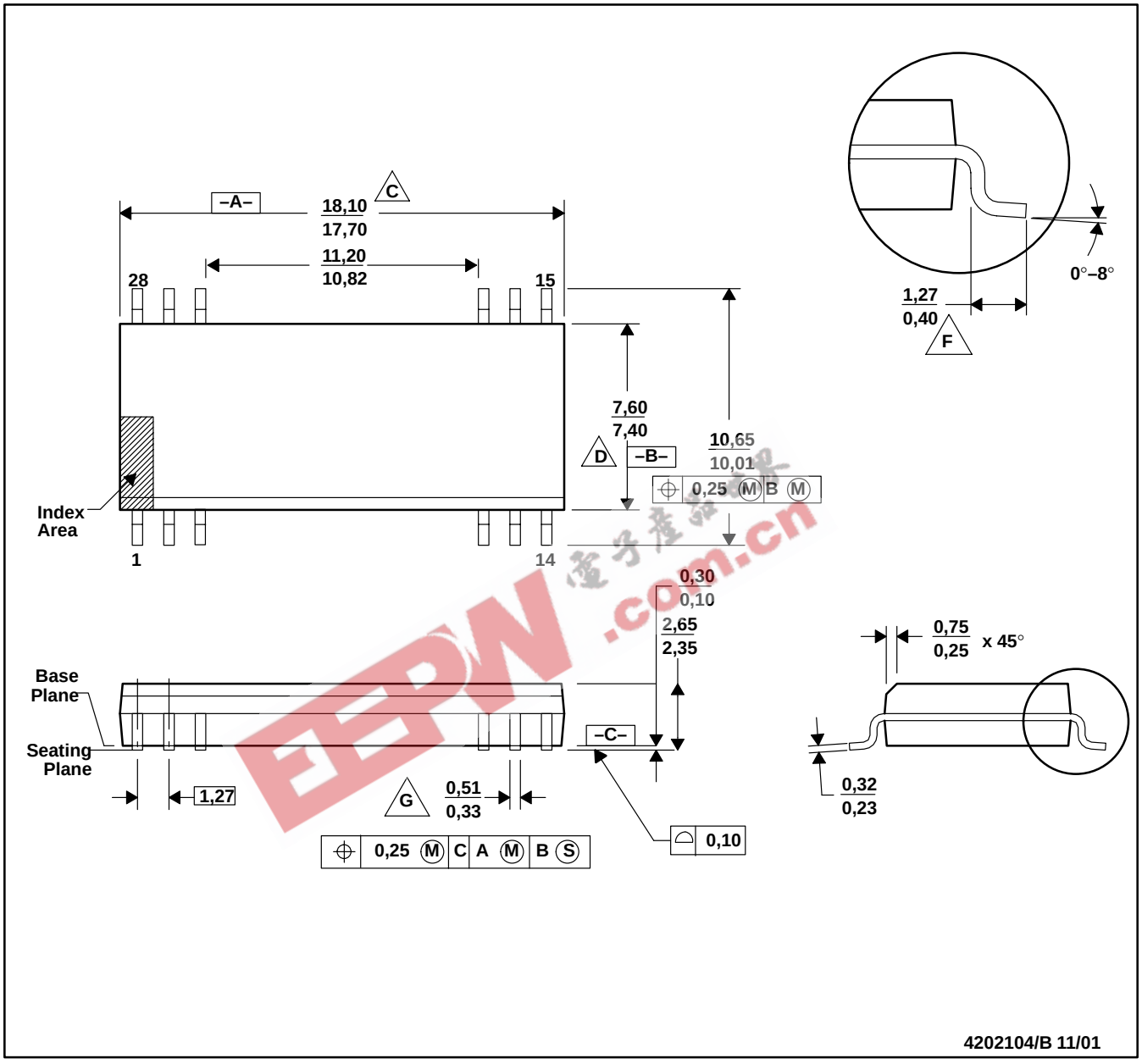
G. A visual index feature must be located within the cross-hatched area.

MPDS106A – AUGUST 2001 – REVISED NOVEMBER 2001

DVB(R-PDSO-G12/28) **PLASTIC SMALL-OUTLINE**



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