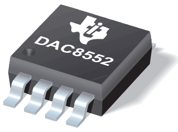
Burr-Brown Products
from Texas Instruments



DAC8552

SLAS430 – JULY 2006

16-BIT, DUAL CHANNEL, ULTRA-LOW GLITCH VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy: 4LSB**
- **Glitch Energy: 0.15nV-s**
- ***Micro*Power Operation: 155µA per Channel at 2.7V**
- **Power-On Reset to Zero-Scale**
- **Power Supply: 2.7V to 5.5V**
- **16-Bit Monotonic Over Temperature**
- **Settling Time: 10µs to ±0.003% FSR**
- **Ultra-Low AC Crosstalk: –100dB Typ**
- **Low-Power Serial Interface With Schmitt-Triggered Inputs**
- **On-Chip Output Buffer Amplifier With Rail-to-Rail Operation**
- **Double-Buffered Input Architecture**
- **Simultaneous or Sequential Output Update and Powerdown**
- **Available in a Tiny MSOP-8 Package**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo Control**
- **Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**

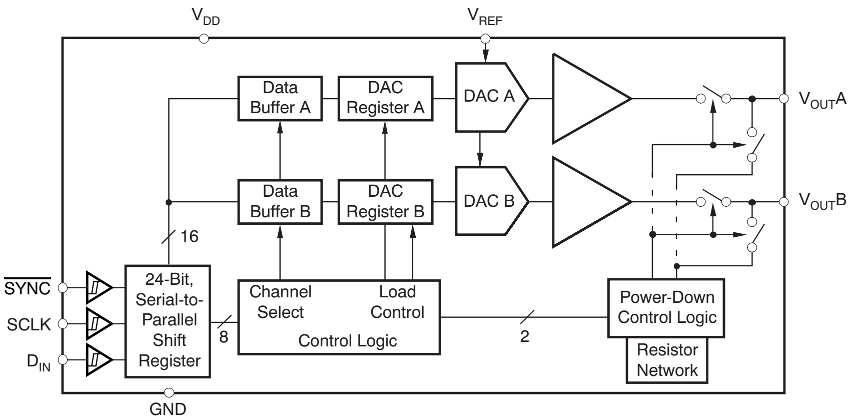
DESCRIPTION

The DAC8552 is a 16-bit, dual channel, voltage output digital-to-analog converter (DAC) offering low power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7V to 5.5V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30MHz for V_{DD} = 5V.

The DAC8552 requires an external reference voltage to set the output range of each DAC channel. Also incorporated into the device is a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place. The DAC8552 provides a flexible power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 700nA at 5V.

The low-power consumption of this device in normal operation makes it ideally suited for portable battery-operated equipment and other low-power applications. The power consumption is 0.5mW per channel at 2.7V, reducing to 1µW in power-down mode.

The DAC8552 is available in a MSOP-8 package with a specified operating temperature range of –40°C to +105°C.



SPI, QSP are trademarks of Motorola.
Microwire is a trademark of National Semiconductor.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8552	±12	±1	MSOP-8	DGK	–40°C to +105°C	D82	DAC8552IDGKT	Tape and Reel, 250
							DAC8552IDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
V_{DD} to GND	–0.3V to 6V
Digital input voltage to GND	–0.3V to V_{DD} + 0.3V
V_{OUTA} or V_{OUTB} to GND	–0.3V to V_{DD} + 0.3V
Operating temperature range	–40°C to +105°C
Storage temperature range	–65°C to +150°C
Junction temperature (T_J max)	+150°C
Power dissipation	(T_J max – T_A)/θ_{JA}
θ_{JA} thermal impedance	206°C/W
θ_{JC} thermal impedance	44°C/W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, all specifications –40°C to +105°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)					
Resolution		16			Bits
Relative accuracy	Measured by line passing through codes 513 and 64741		±4	±12	LSB
Differential nonlinearity	16-bit monotonic		±0.35	±1	LSB
Zero code error	Measured by line passing through codes 485 and 64741		±2.5	±12	mV
Zero code error drift			±5		µV/°C
Full-scale error	Measured by line passing through codes 485 and 64741		±0.1	±0.5	% of FSR
Gain error	Measured by line passing through codes 485 and 64741		±0.08	±0.2	% of FSR
Gain temperature coefficient			±1		ppm of FSR/°C
PSRR	Output unloaded		0.75		mV/V
OUTPUT CHARACTERISTICS(2)					
Output voltage range		0		V_{REF}	V

(1) Linearity calculated using a reduced code range of 513 to 64741. Output unloaded.
(2) Specified by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

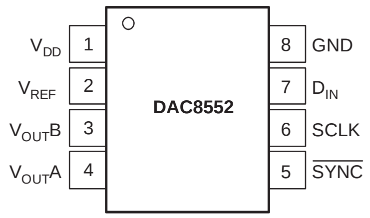
V_{DD} = 2.7V to 5.5V, all specifications –40°C to +105°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage settling time	To ±0.003% FSR 0200$_H$ to FD00$_H$, R_L = 2kΩ; 0pF < C_L < 200pF		8	10	µs
	R_L = 2kΩ; C_L = 500pF		12		
Slew rate			1.8		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		
Code change glitch impulse	1LSB change around major carry		0.15		nV-s
Digital feedthrough	50kΩ series resistance on digital lines		0.15		nV-s
DC crosstalk	Full-scale swing on adjacent channel. V_{DD} = 5V, V_{REF} = 4.096V		0.25		LSB
AC crosstalk	1kHz Sine wave		–100		dB
DC output impedance	At mid-point input		1		Ω
Short circuit current	V_{DD} = 5V		50		mA
	V_{DD} = 3V		20		
Power-up time	Coming out of power-down mode V_{DD} = 5V		2.5		µs
	Coming out of power-down mode V_{DD} = 3V		5		µs
AC PERFORMANCE					
SNR	BW = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		95		dB
THD			-85		
SFDR			87		
SINAD			84		
REFERENCE INPUT					
Reference current	V_{REF} = V_{DD} = 5.5V		90	120	µA
	V_{REF} = V_{DD} = 3.6V		60	100	
Reference input range		0		V_{DD}	V
Reference input impedance			62		kΩ
LOGIC INPUTS (3)					
Input current				±1	µA
V_{IN}L, Input LOW voltage	V_{DD} = 5V			0.8	V
	V_{DD} = 3V			0.6	
V_{IN}H, Input HIGH voltage	V_{DD} = 5V	2.4			V
	V_{DD} = 3V	2.1			
Pin capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD} (normal mode)	Input Code = 32768, no load, does not include reference current				
V_{DD} = 3.6V to 5.5V	V_{IH} = V_{DD} and V_{IL} = GND		340	500	µA
V_{DD} = 2.7V to 3.6V			310	480	
I_{DD} (all power-down modes)					
V_{DD} = 3.6V to 5.5V	V_{IH} = V_{DD} and V_{IL} = GND		0.7	2	µA
V_{DD} = 2.7V to 3.6V			0.4	2	
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2mA, V_{DD} = 5V		89%		
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

(3) Specified by design and characterization, not production tested.

PIN CONFIGURATION

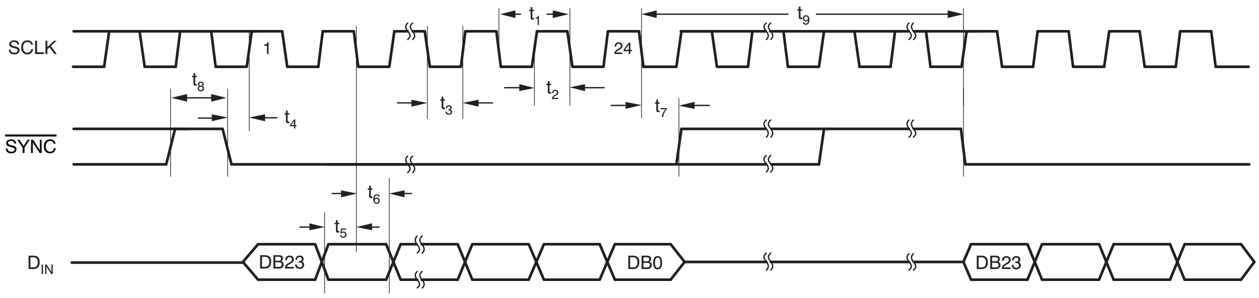
DGK PACKAGE
MSOP-8
(Top View)



PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	V_{DD}	Power supply input, 2.7V to 5.5V
2	V_{REF}	Reference voltage input
3	$V_{OUT}B$	Analog output voltage from DAC B
4	$V_{OUT}A$	Analog output voltage from DAC A
5	$\overline{SYNC}$	Level triggered $\overline{SYNC}$ input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred on the falling edges of SCLK. The action specified by the 8-bit control byte and 16-bit data word is executed following the 24th falling SCLK clock edge (unless $\overline{SYNC}$ is taken HIGH before this edge in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8552). Schmitt-Trigger logic input.
6	SCLK	Serial Clock Input. Data can be transferred at rates up to 30MHz at 5V. Schmitt-Trigger logic input.
7	D_{IN}	Serial Data Input. Data is clocked into the 24-bit input shift register on the falling edge of the serial clock input. Schmitt-Trigger logic input.
8	GND	Ground reference point for all circuitry on the part.

SERIAL WRITE OPERATION



TIMING CHARACTERISTICS (1)(2)

V_{DD} = 2.7V to 5.5V, all specifications –40°C to +105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1 (3)	SCLK cycle time	V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			
t_2	SCLK HIGH time	V_{DD} = 2.7V to 3.6V	13			ns
		V_{DD} = 3.6V to 5.5V	13			
t_3	SCLK LOW time	V_{DD} = 2.7V to 3.6V	22.5			ns
		V_{DD} = 3.6V to 5.5V	13			
t_4	$\overline{SYNC}$ to SCLK rising edge setup time	V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			
t_5	Data setup time	V_{DD} = 2.7V to 3.6V	5			ns
		V_{DD} = 3.6V to 5.5V	5			
t_6	Data hold time	V_{DD} = 2.7V to 3.6V	4.5			ns
		V_{DD} = 3.6V to 5.5V	4.5			
t_7	24th SCLK falling edge to $\overline{SYNC}$ rising edge	V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			
t_9	24th SCLK falling edge to $\overline{SYNC}$ falling edge	V_{DD} = 2.7V to 5.5V	100			ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See Serial Write Operation timing diagram.
(3) Maximum SCLK frequency is 30MHz at V_{DD} = 3.6V to 5.5V and 20MHz at V_{DD} = 2.7V to 3.6V.

TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE

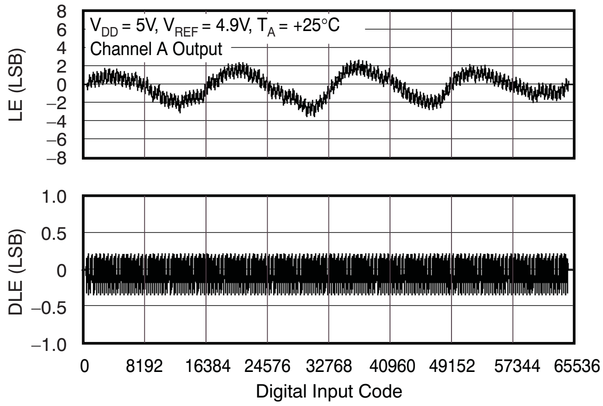


Figure 1.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE

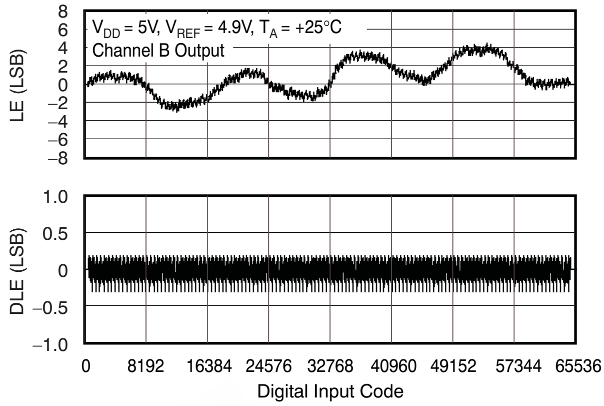


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE

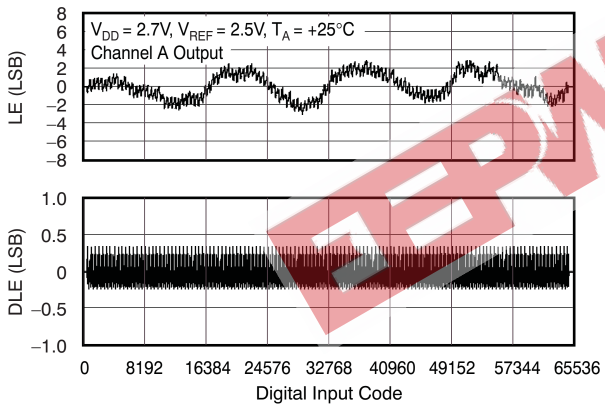


Figure 3.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE

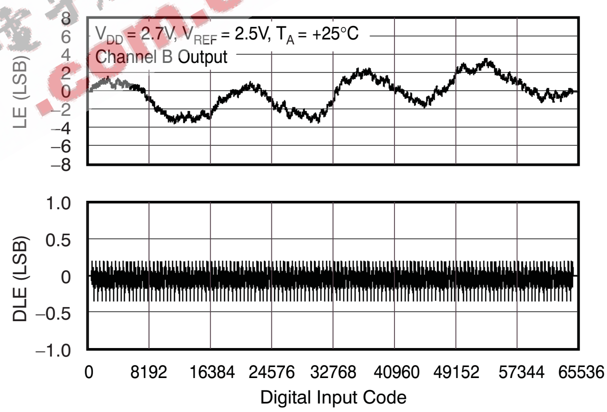


Figure 4.

ZERO-SCALE ERROR vs TEMPERATURE

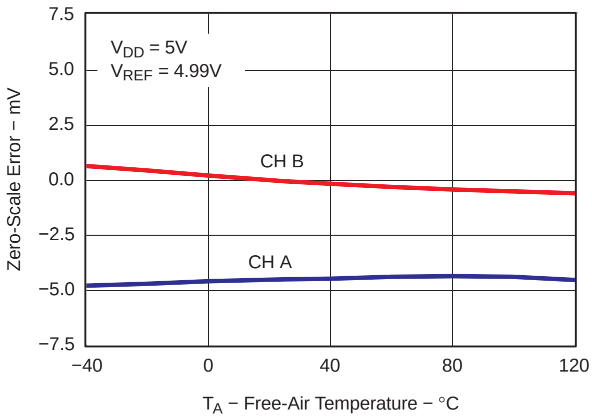


Figure 5.

ZERO-SCALE ERROR vs TEMPERATURE

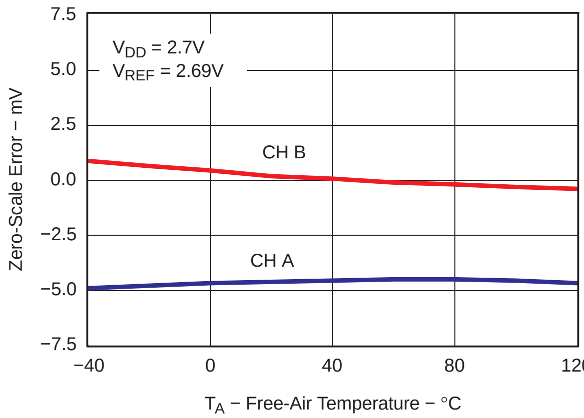


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

FULL-SCALE ERROR vs TEMPERATURE

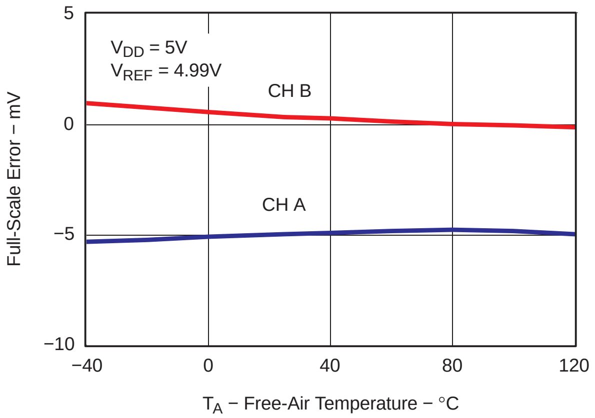


Figure 7.

FULL-SCALE ERROR vs TEMPERATURE

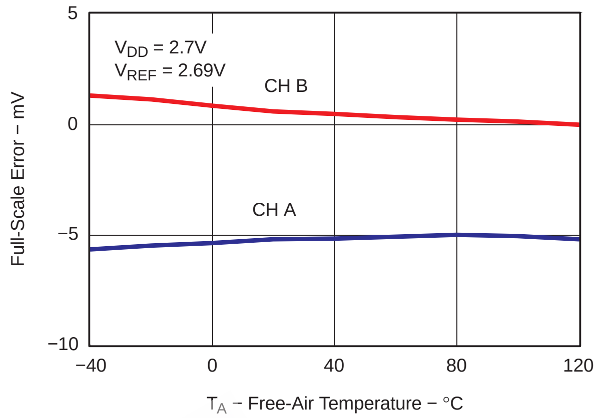


Figure 8.

SINK CURRENT CAPABILTY AT NEGATIVE RAIL

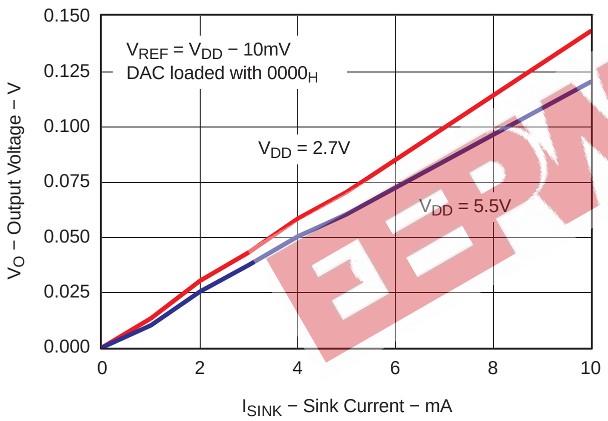


Figure 9.

SOURCE CURRENT CAPABILITY AT POSITIVE RAIL

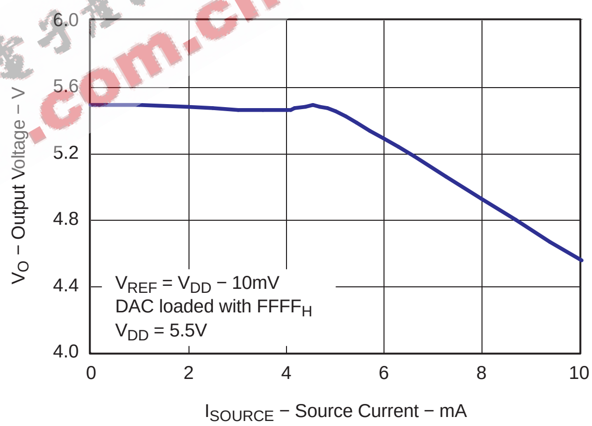


Figure 10.

SOURCE CURRENT CAPABILITY AT POSITIVE RAIL

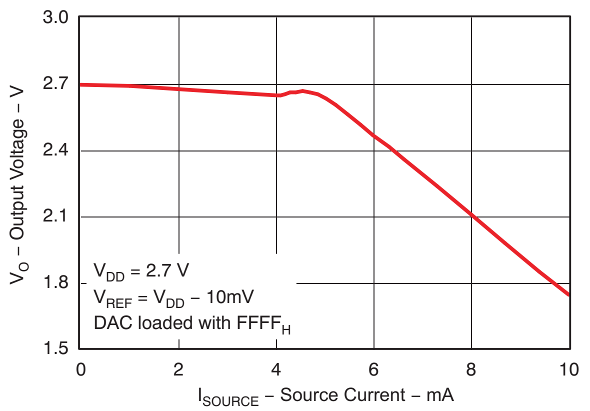


Figure 11.

SUPPLY CURRENT vs DIGITAL INPUT CODE

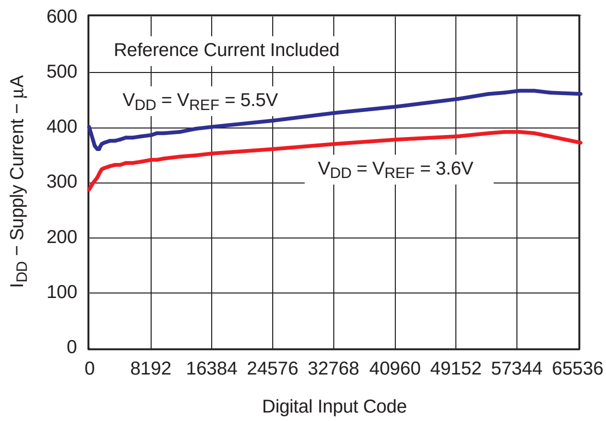


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

SUPPLY CURRENT vs SUPPLY VOLTAGE

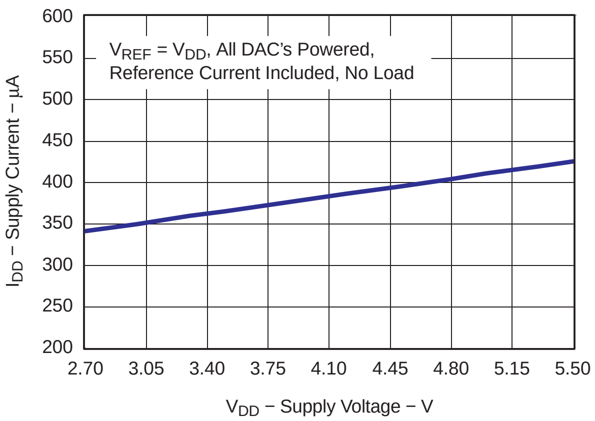


Figure 13.

SUPPLY CURRENT vs TEMPERATURE

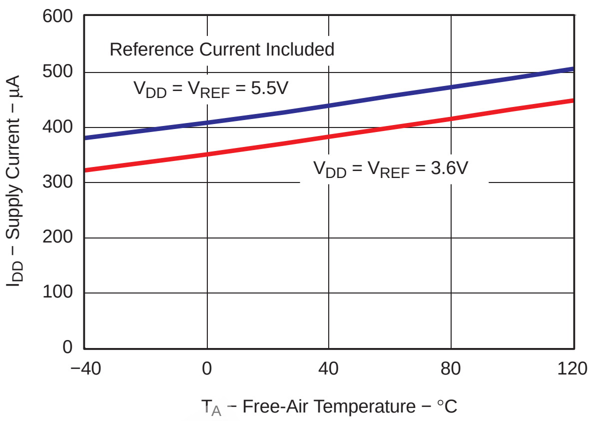


Figure 14.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

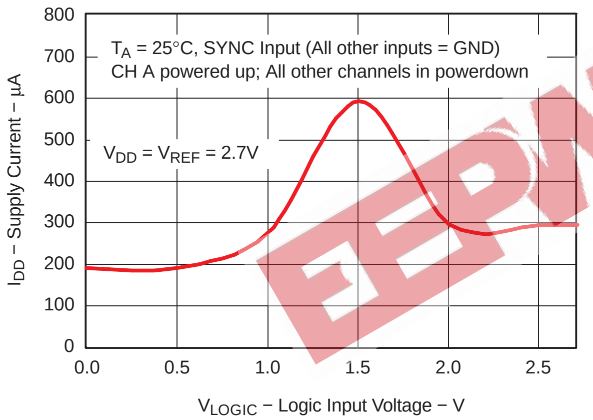


Figure 15.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

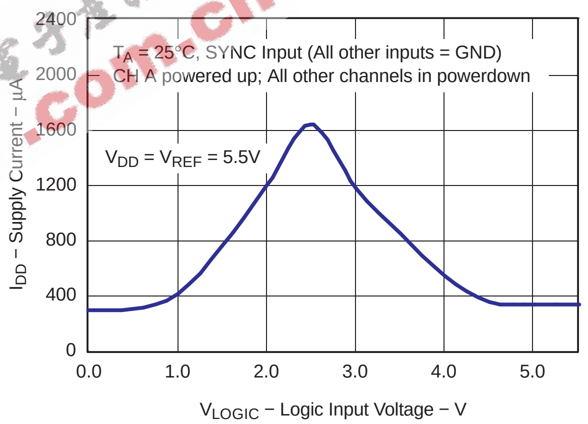


Figure 16.

POWER SPECTRAL DENSITY

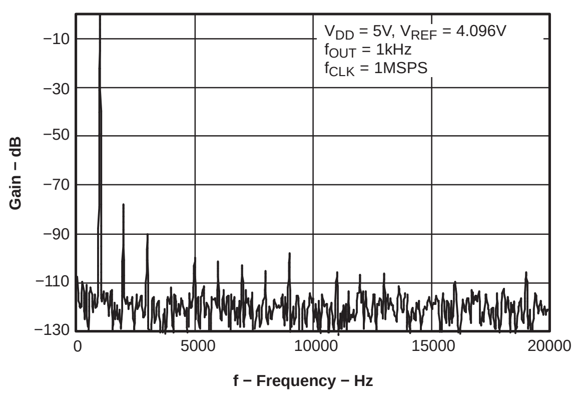


Figure 17.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

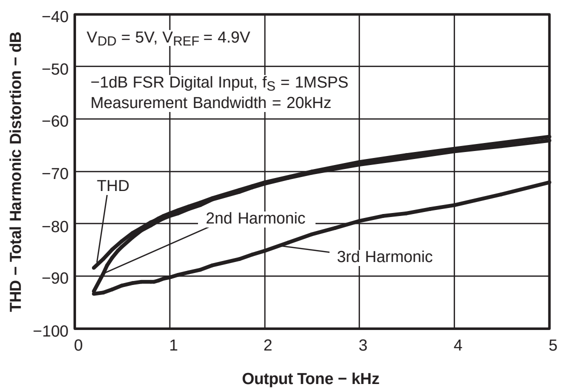


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

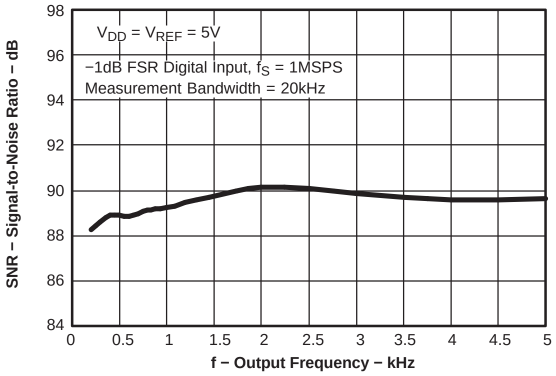


Figure 19.

OUTPUT NOISE DENSITY

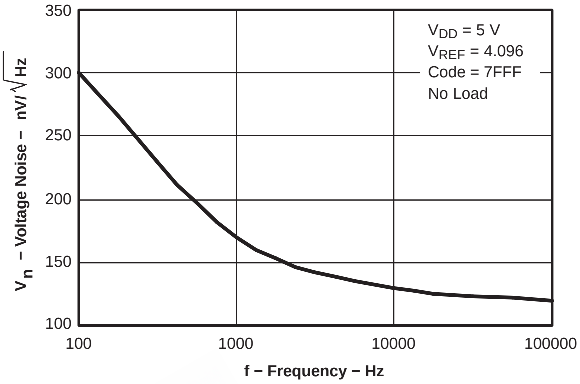


Figure 20.

FULL-SCALE SETTLING TIME: 5V RISING EDGE

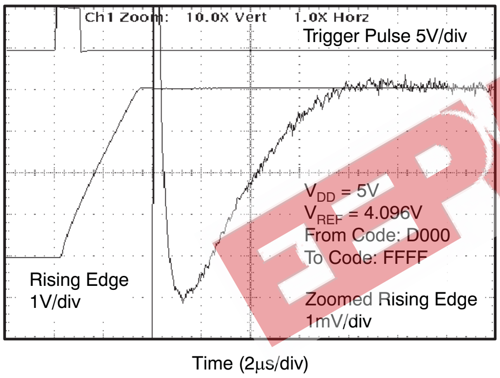


Figure 21.

FULL-SCALE SETTLING TIME: 5V FALLING EDGE

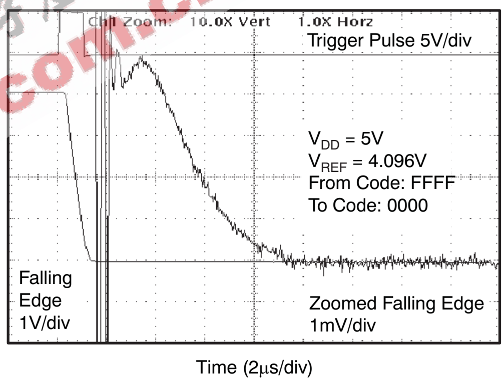


Figure 22.

HALF-SCALE SETTLING TIME: 5V RISING EDGE

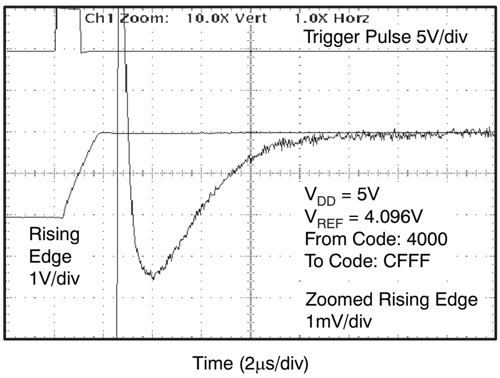


Figure 23.

HALF-SCALE SETTLING TIME: 5V FALLING EDGE

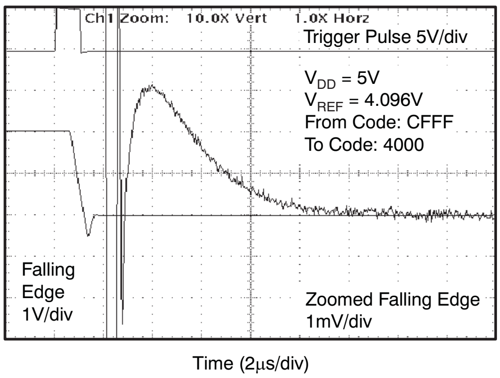


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

FULL-SCALE SETTLING TIME: 2.7V RISING EDGE

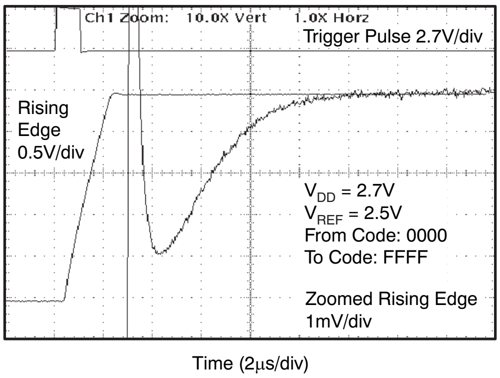


Figure 25.

FULL-SCALE SETTLING TIME: 2.7V FALLING EDGE

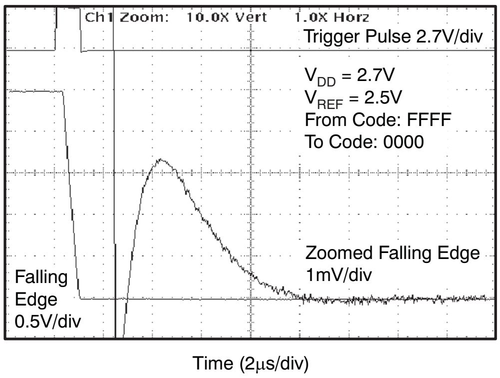


Figure 26.

HALF-SCALE SETTLING TIME: 2.7V RISING EDGE

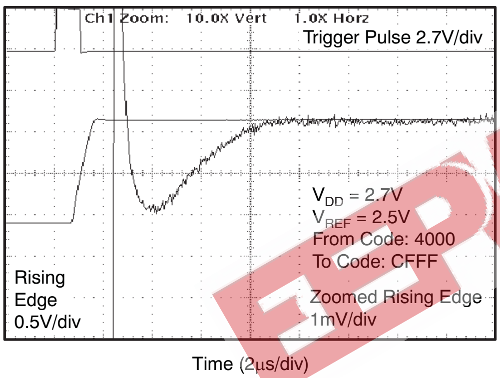


Figure 27.

HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE

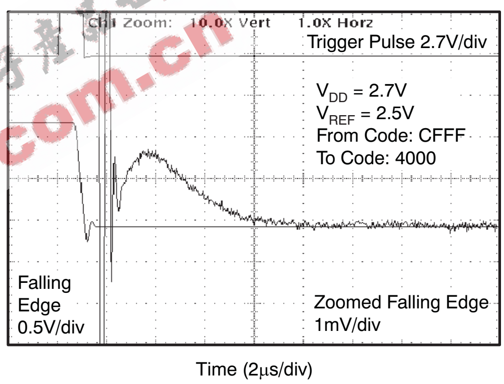


Figure 28.

GLITCH ENERGY: 5V, 1LSB STEP, RISING EDGE

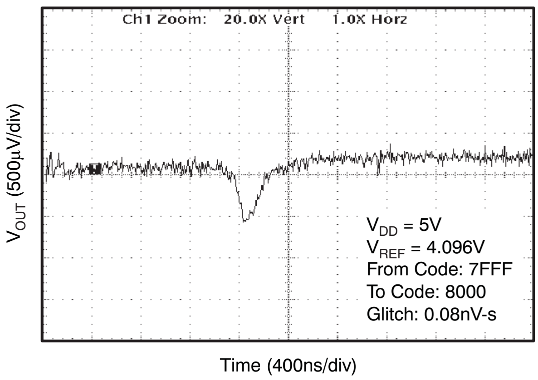


Figure 29.

GLITCH ENERGY: 5V, 1LSB STEP, FALLING EDGE

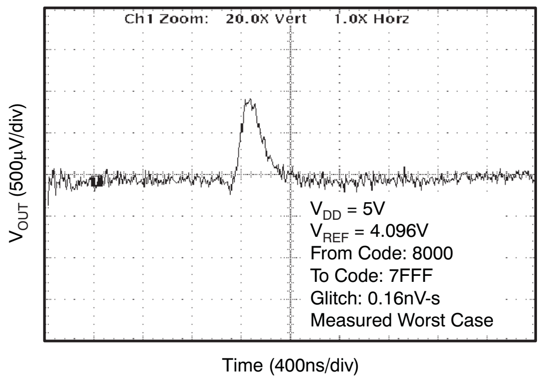


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

GLITCH ENERGY: 5V, 16LSB STEP, RISING EDGE

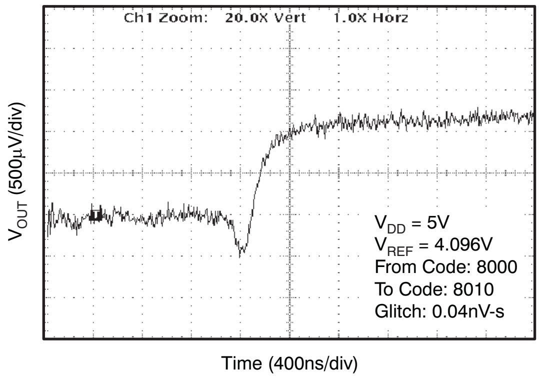


Figure 31.

GLITCH ENERGY: 5V, 16LSB STEP, FALLING EDGE

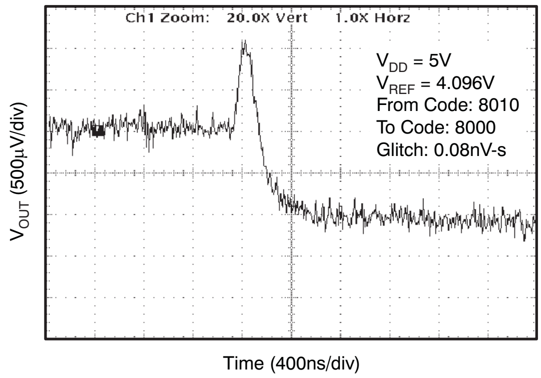


Figure 32.

GLITCH ENERGY: 5V, 256LSB STEP, RISING EDGE

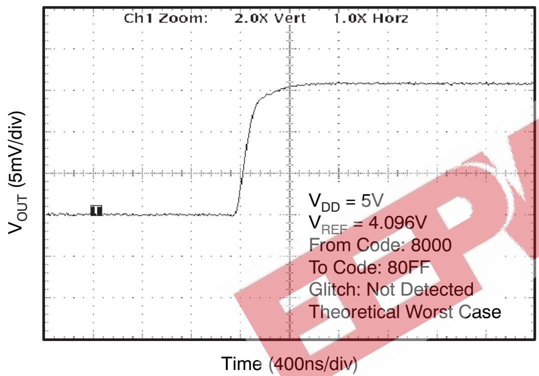


Figure 33.

GLITCH ENERGY: 5V, 256LSB STEP, FALLING EDGE

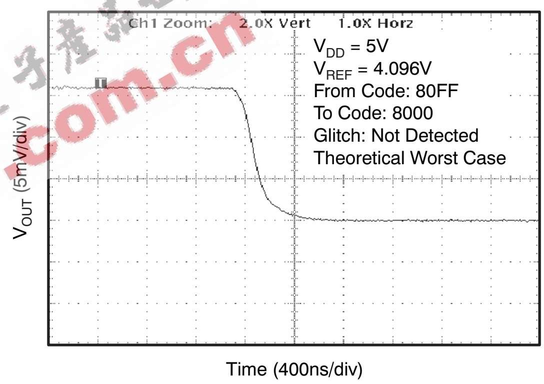


Figure 34.

GLITCH ENERGY: 2.7V, 1LSB STEP, RISING EDGE

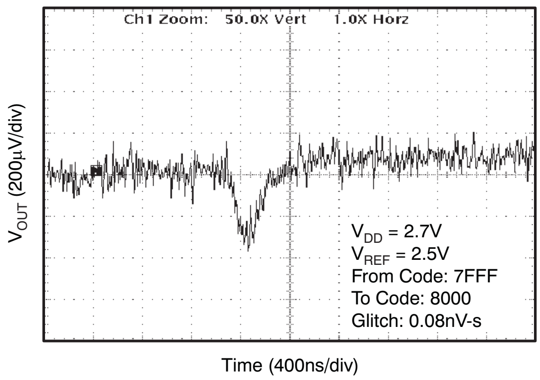


Figure 35.

GLITCH ENERGY: 2.7V, 1LSB STEP, FALLING EDGE

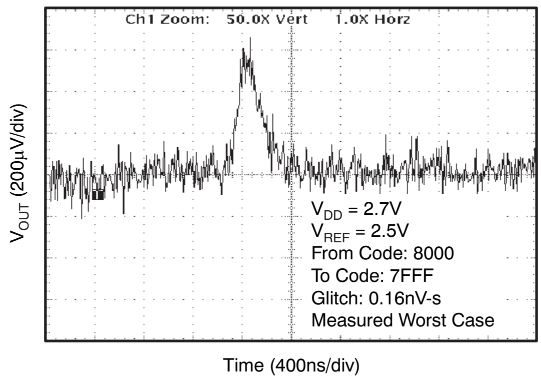


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

GLITCH ENERGY: 2.7V, 16LSB STEP, RISING EDGE

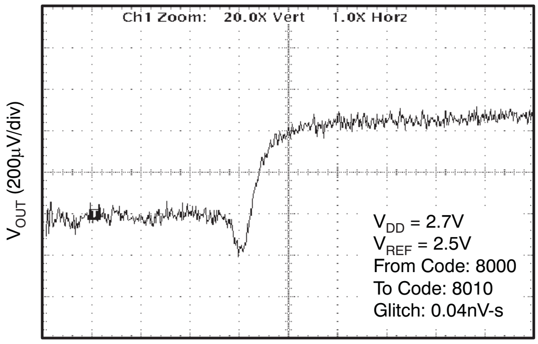


Figure 37.

GLITCH ENERGY: 2.7V, 16LSB STEP, FALLING EDGE

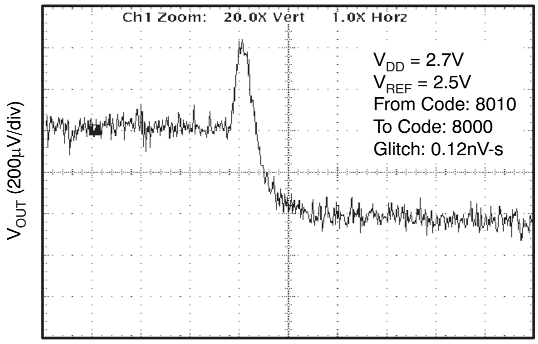


Figure 38.

GLITCH ENERGY: 2.7V, 256LSB STEP, RISING EDGE

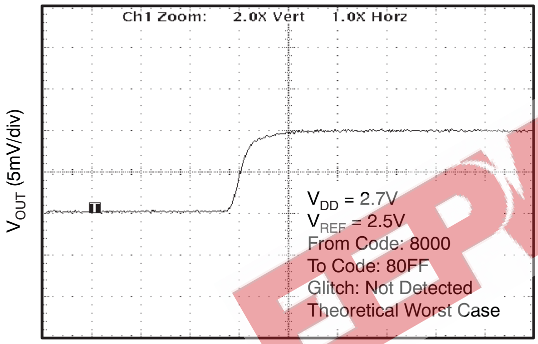


Figure 39.

GLITCH ENERGY: 2.7V, 256LSB STEP, FALLING EDGE

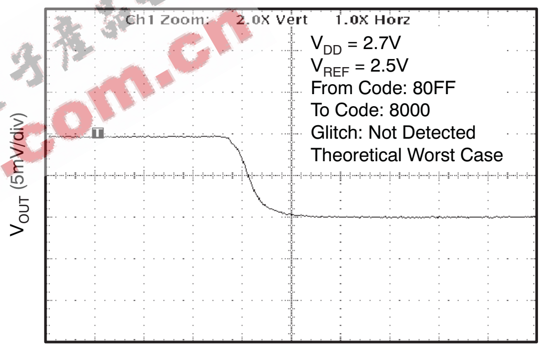


Figure 40.

THEORY OF OPERATION

DAC SECTION

The architecture of each channel of the DAC8552 consists of a resistor-string DAC followed by an output buffer amplifier. Figure 41 shows a simplified block diagram of the DAC architecture.

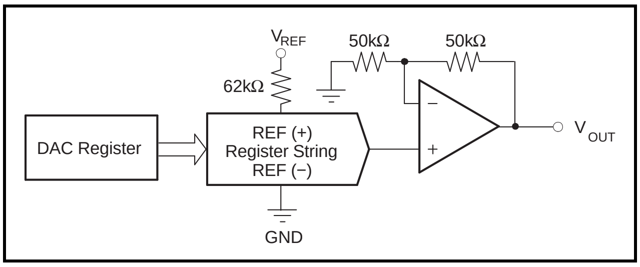


Figure 41. DAC8552 Architecture

The input coding for each device is unipolar straight binary, so the ideal output voltage is given by:

$$V_{OUT}A, B = V_{REF} \times \frac{D}{65536} \quad (1)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535. V_{OUT}A,B refers to channel A or B.

RESISTOR STRING

The resistor string section is shown in Figure 42. It is simply a divide-by-2 resistor followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. This voltage is then applied to the output amplifier by closing one of the switches connecting the string to the amplifier.

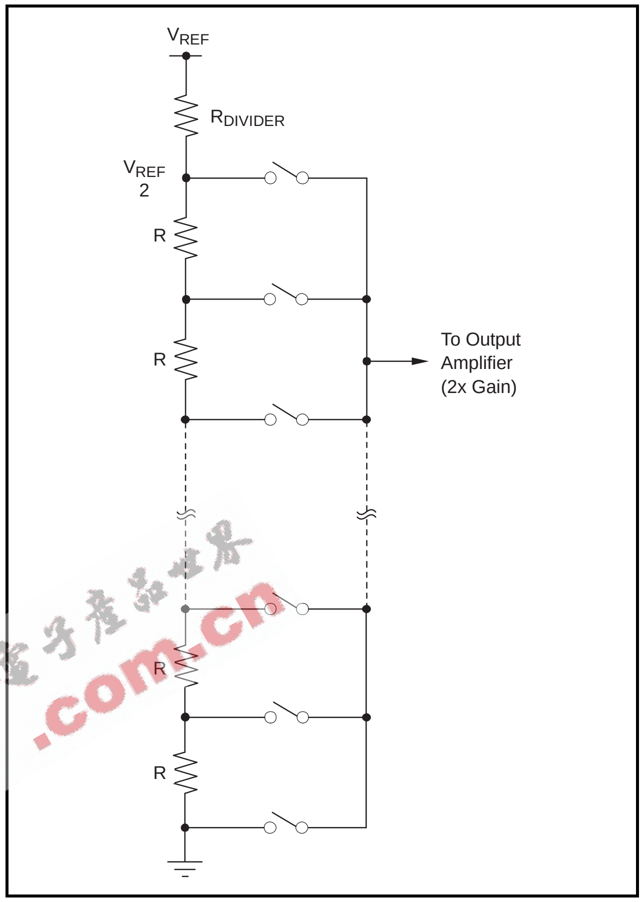


Figure 42. Resistor String

OUTPUT AMPLIFIER

Each output buffer amplifier is capable of generating rail-to-rail voltages on its output which approaches an output range of 0V to V_{DD} (gain and offset errors must be taken into account). Each buffer is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics.

SERIAL INTERFACE

The DAC8552 uses a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI™ and QSP™, and Microwire™ interface standards, as well as most DSPs. See the *Serial Write Operation* timing diagram for an example of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8552 compatible with high speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register is locked. Further clocking does not change the shift register data. Once 24 bits are locked into the shift register, the 8 MSBs are used as control bits and the 16 LSBs are used as data. After receiving the 24th falling clock edge, the DAC8552 decodes the 8 control bits and 16 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. A new SPI sequence starts at the next falling edge of $\overline{SYNC}$. A rising edge of $\overline{SYNC}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs.

After the 24th falling edge of SCLK is received, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible. (See the *Typical Characteristics* section for the *Supply Current vs Logic Input Voltage* transfer characteristic curve).

INPUT SHIFT REGISTER

The input shift register of the DAC8552 is 24 bits wide (see Figure 45) and is made up of 8 control bits (DB16–DB23) and 16 data bits (DB0–DB15). The first two control bits (DB22 and DB23) are reserved and must be '0' for proper operation. LDA (DB20) and LD B (DB21) control the updating of each analog output with the specified 16-bit data value or power-down command. Bit DB19 is a *Don't Care* bit, which does not affect the operation of the DAC8552 and can be '1' or '0'. The following control bit, Buffer Select (DB18), controls the destination of the data (or power-down command) between DAC A and DAC B. The final two control bits, PD0 (DB16) and PD1 (DB17), select the power-down mode of one or both of the DAC channels. The four modes are normal mode or any one of three power-down modes. A more complete description of the operational modes of the DAC8552 can be found in the Power-Down Modes section. The remaining sixteen bits of the 24-bit input word make up the data bits. These are transferred to the specified Data Buffer or DAC Register, depending on the command issued by the control byte, on the 24th falling edge of SCLK. See Table 2 and Table 3 for more information.

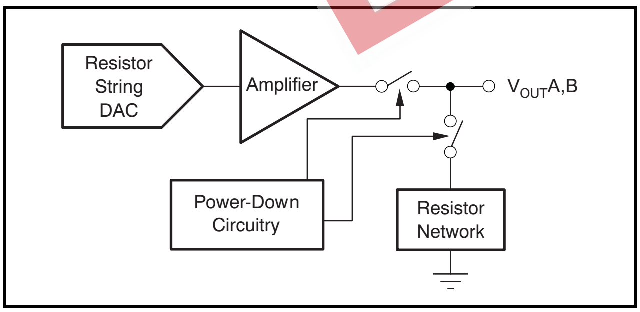


Figure 43. Output Stage During Power-Down (High Impedance)

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the addressed DAC register is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register is reset and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents or a change in the operating mode occurs (see Figure 44).

POWER-ON RESET

The DAC8552 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain there until a valid write sequence and load command is made to the respective DAC channel. This is useful in applications where it is important to know the state of the output of each DAC output while the device is in the process of powering up.

No device pin should be brought high before power is applied to the device.

POWER-DOWN MODES

The DAC8552 utilizes four modes of operation. These modes are accessed by setting two bits (PD1 and PD0) in the control *Load* action to one or both DACs. Table 1 shows how the state of the bits correspond to the register and performing a mode of operation of each channel of the device. (Each DAC channel can be powered down simultaneously or independently of each other. Power-down occurs after proper data is written into PD0 and PD1 and a *Load* command occurs.) See the *Operation Examples* section for additional information.

Table 1. Modes of Operation for the DAC8552

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal Operation
—	—	Power-down modes
0	1	Output typically 1kΩ to GND
1	0	Output typically 100kΩ to GND
1	1	High impedance

When both bits are set to 0, the device works normally with a typical power consumption of 450µA at 5V. For the three power-down modes, however, the supply current falls to 700nA at 5V (400nA at 3V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options for power-down: The output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Impedance). The output stage is illustrated in Figure 43.

All analog circuitry is shut down when the power-down mode is activated. Each DAC will exit power-down when PD0 and PD1 are set to 0, new data is written to the Data Buffer, and the DAC channel receives a *Load* command. The time to exit power-down is typically 2.5µs for V_{DD} = 5V and 5µs for V_{DD} = 3V (see the *Typical Characteristics*).

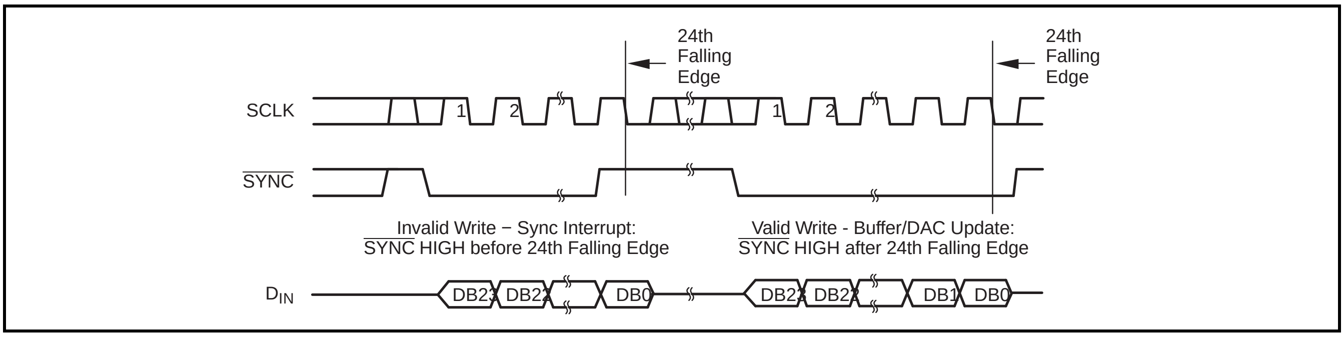


Figure 44. Interrupt and Valid SYNC Timing

DB23 ... **DB12**

0	0	LDB	LDA	X	Buffer Select	PD1	PD0	D15	D14	D13	D12

DB11 ... **DB0**

D11	D10	D9	D8	D7	D6	D5	D5	D3	D2	D1	D0

Figure 45. DAC8552 Data Input Register Format

Table 2. Control Matrix

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13–D0	DESCRIPTION
Reserved	Reserved	Load B	Load A	Don't Care	Buffer Select	PD1	PD0	MSB	MSB-1	MSB-2... LSB	
(Always Write 0)					0 = A, 1 = B						
0	0	0	0	X	#	0	0	Data			WR Buffer # w/Data
0	0	0	0	X	#	See Table 3		X			WR Buffer # w/Power-down Command
0	0	0	1	X	#	0	0	Data			WR Buffer # w/Data and Load DAC A
0	0	0	1	X	0	See Table 3		X			WR Buffer A w/Power-Down Command and LOAD DAC A (DAC A Powered Down)
0	0	0	1	X	1	See Table 3		X			WR Buffer B w/Power-Down Command and LOAD DAC A
0	0	1	0	X	#	0	0	Data			WR Buffer # w/Data and Load DAC B
0	0	1	0	X	0	See Table 3		X			WR Buffer A w/Power-Down Command and LOAD DAC B
0	0	1	0	X	1	See Table 3		X			WR Buffer B w/Power-Down Command and LOAD DAC B (DAC B Powered Down)
0	0	1	1	X	#	0	0	Data			WR Buffer # w/Data and Load DACs A and B
0	0	1	1	X	0	See Table 3		X			WR Buffer A w/Power-Down Command and Load DACs A and B (DAC A Powered Down)
0	0	1	1	X	1	See Table 3		X			WR Buffer B w/Power-Down Command and Load DACs A and B (DAC B Powered Down)

Table 3. Power-Down Commands

D17	D16	OUTPUT IMPEDANCE POWER DOWN COMMANDS
PD1	PD0	
0	1	1kΩ
1	0	100kΩ
1	1	High Impedance

OPERATION EXAMPLES

Example 1: Write to Data Buffer A; Through Buffer B; Load DACA Through DACB Simultaneously

- 1st — Write to DataBuffer A:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	0	0	X	0	0	0	D15	—	D1	D0

- 2nd — Write to Data Buffer B and Load DAC A and DAC B simultaneously:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	1	1	X	1	0	0	D15	—	D1	D0

The DACA and DACB analog outputs simultaneously settle to the specified values upon completion of the 2nd write sequence. (The *Load* command moves the digital data from the data buffer to the DAC register at which time the conversion takes place and the analog output is updated. *Completion* occurs on the 24th falling SCLK edge after $\overline{\text{SYNC}}$ LOW.)

Example 2: Load New Data to DACA and DACB Sequentially

- 1st — Write to Data Buffer A and Load DAC A: DACA output settles to specified value upon completion:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	0	1	X	0	0	0	D15	—	D1	D0

- 2nd — Write to Data Buffer B and Load DAC B: DACB output settles to specified value upon completion:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	1	0	X	1	0	0	D15	—	D1	D0

After completion of the 1st write cycle, the DACA analog output settles to the voltage specified; upon completion of write cycle 2, the DACB analog output settles.

Example 3: Power-Down DACA to 1kΩ and Power-Down DACB to 100kΩ Simultaneously

- 1st — Write power-down command to Data Buffer A:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	0	0	X	0	0	1	Don't Care			

- 2nd — Write power-down command to Data Buffer B and Load DACA and DACB simultaneously:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	1	1	X	1	1	0	Don't Care			

The DACA and DACB analog outputs simultaneously power-down to each respective specified mode upon completion of the 2nd write sequence.

Example 4: Power-Down DACA and DACB to High-Impedance Sequentially:

- 1st — Write power-down command to Data Buffer A and Load DAC A: DAC A output = Hi-Z:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	0	1	X	0	1	1	Don't Care			

- 2nd — Write power-down command to Data Buffer B and Load DAC B: DAC B output = Hi-Z:

Reserved	Reserved	LDB	LDA	DC	Buffer Select	PD1	PD0	DB15	—	DB1	DB0
0	0	1	0	X	1	1	1	Don't Care			

The DACA and DACB analog outputs sequentially power-down to high-impedance upon completion of the 1st and 2nd write sequences, respectively.

MICROPROCESSOR INTERFACING

DAC8552 to 8051 INTERFACE

Figure 46 shows a serial interface between the DAC8552 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8552, while RXD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8552, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second and third write cycle is initiated to transmit the remaining data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which presents the LSB first, while the DAC8552 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed

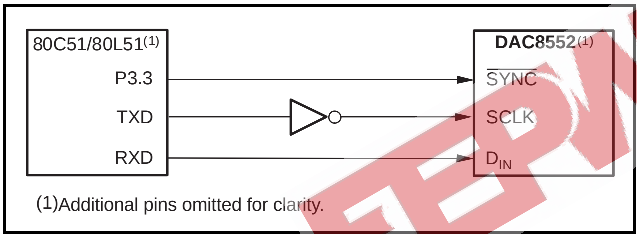


Figure 46. DAC8552 to 80C51/80L51 Interface

DAC8552 to Microwire INTERFACE

Figure 47 shows an interface between the DAC8552 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8552 on the rising edge of the SK signal.

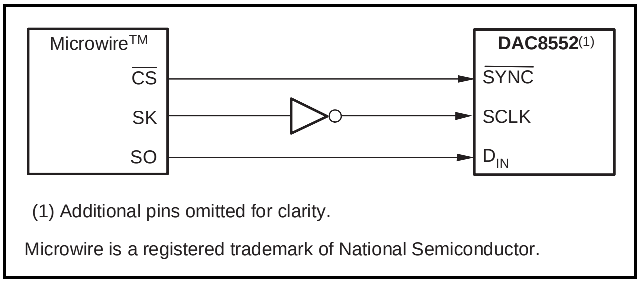


Figure 47. DAC8552 to Microwire Interface

DAC8552 to 68HC11 INTERFACE

Figure 48 shows a serial interface between the DAC8552 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8552, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7), similar to the 8051 diagram.

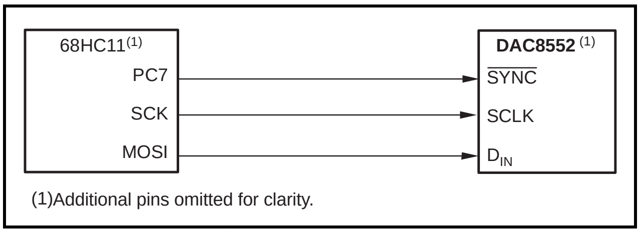


Figure 48. DAC8552 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8552, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.

DAC8552 to TMS320 DSP INTERFACE

Figure 49 shows the connections between the DAC8552 and a TMS320 digital signal processor. By decoding the FSX signal, multiple DAC8552s can be connected to a single serial port of the DSP.

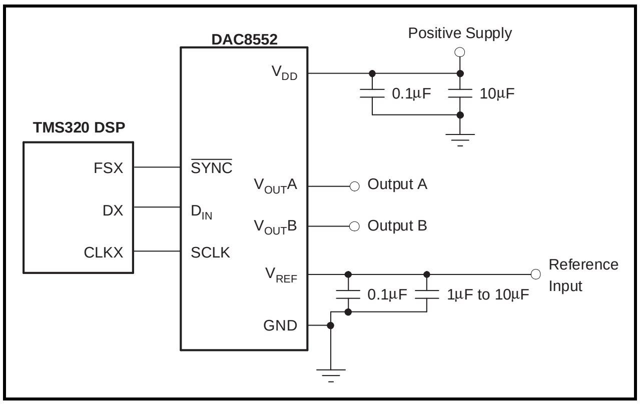


Figure 49. DAC8552 to TMS320 DSP

APPLICATION INFORMATION

CURRENT CONSUMPTION

The DAC8552 typically consumes 170µA at V_{DD} = 5 V and 155µA at V_{DD} = 2.7V for each active channel, excluding reference current consumption. Additional current consumption can occur at the digital inputs if V_{IH}<< V_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital input to the DAC.

In power-down mode, typical current consumption is 700nA. A delay time of 10ms to 20ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10µA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC8552 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC8552 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2kΩ can be driven by the DAC8552 while achieving good load regulation. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 100mV of the DACs output voltage characteristic. Under resistive loading conditions, good linearity is preserved as long as the output voltage is at least 100 mV below the VDD voltage.

CROSSTALK AND AC PERFORMANCE

The DAC8552 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.5 LSBs. The AC crosstalk measured (for a full-scale, 1kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under –100dB.

In addition, the DAC8552 can achieve typical AC performance of 96dB signal-to-noise ratio (SNR) and -85dB total harmonic distortion (THD), making the DAC8552 a solid choice for applications requiring high SNR at output frequencies at or below 10kHz.

OUTPUT VOLTAGE STABILITY

The DAC8552 exhibits excellent temperature stability of 5ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a ±25µV window for a ±1°C ambient temperature change.

Good power-supply rejection ratio (PSRR) performance reduces supply noise present on V_{DD} from appearing at the outputs. Combined with good DC noise performance and true 16-bit differential linearity, the DAC8552 becomes an ideal choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

The DAC8552 settles to ±0.003% of its full-scale range within 10µs, driving a 200pF, 2kΩ load. For good settling performance the outputs should not approach the top and bottom rails. Small signal settling time is under 1µs, enabling data update rates exceeding 1MSPS for small code changes.

Many applications are sensitive to undesired transient signals such as glitch. The DAC8552 has a proprietary, ultra-low glitch architecture addressing such applications. Code-to-code glitches rarely exceed 1mV and they last under 0.3µs. Typical glitch energy is an outstanding 0.15nV-s. Theoretical worst cast glitch should occur during a 256LSB step, but it is so low, it cannot be detected.

DIFFERENTIAL AND INTERGRAL NONLINEARITY

The DAC8552 uses precision, thin-film resistors to achieve monotonicity and good linearity. Typical linearity error is ±4LSBs; ±0.3mV error for a 5V range. Differential linearity is typically ±0.35LSBs, ±27µV error for a consecutive code change.

USING REF02 AS A POWER SUPPLY FOR DAC8552

Due to the extremely low supply current required by the DAC8552, a possible configuration is to use a REF02 +5V precision voltage reference to supply the required voltage to the DAC8552s supply input as well as the reference input, as shown in Figure 50. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC8552. If the REF02 is used, the current it needs to supply to the DAC8552 is 340µA typical and 500µA max for V_{DD} = 5V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The typical current required (with a 5kΩ load on a given DAC output) is:

340µA + (5V/5kΩ) = 1.34mA

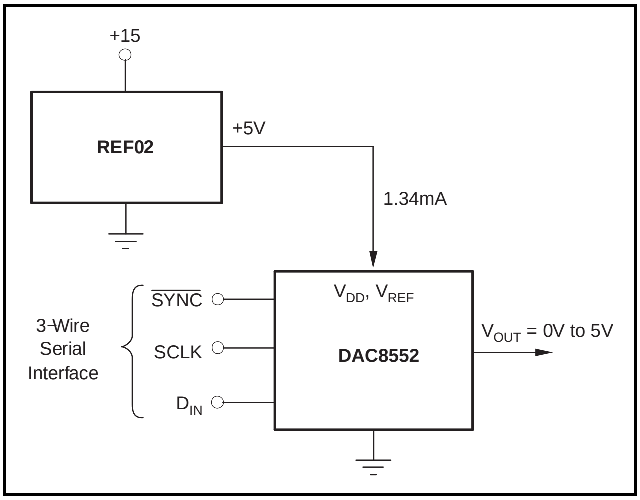


Figure 50. REF02 as a Power Supply to the DAC8552

BIPOLAR OPERATION USING THE DAC8552

The DAC8552 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 51. The circuit shown will give an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an amplifier such as the OPA703, seeFigure 51.

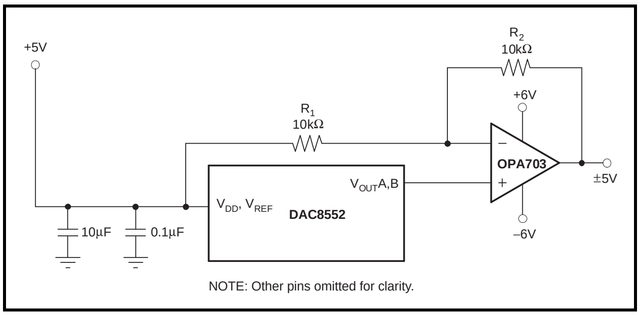


Figure 51. Bipolar Operation with the DAC8552

The output voltage for any input code can be calculated as follows:

$$V_{OUT}A,B = \left[V_{REF} \times \left(\frac{D}{65536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{REF} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0–65535).

With V_{REF} = 5 V, R1 – R2 = 10kΩ.

$$V_{OUT}A,B = \left(\frac{10 \times D}{65536} \right) - 5\ V \quad (3)$$

This is an output voltage range of ±5V with 0000_H corresponding to a –5V output and $FFFF_H$ corresponding to a 5V output. Similarly, using V_{REF} = 2.5V, a ±2.5V output voltage range can be achieved.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8552 offers single-supply operation, and it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8552, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, a 1µF to 10µF capacitor in parallel with a 0.1µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors–all designed to essentially low-pass filter the supply, removing the high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8552IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8552IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8552IDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8552IDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

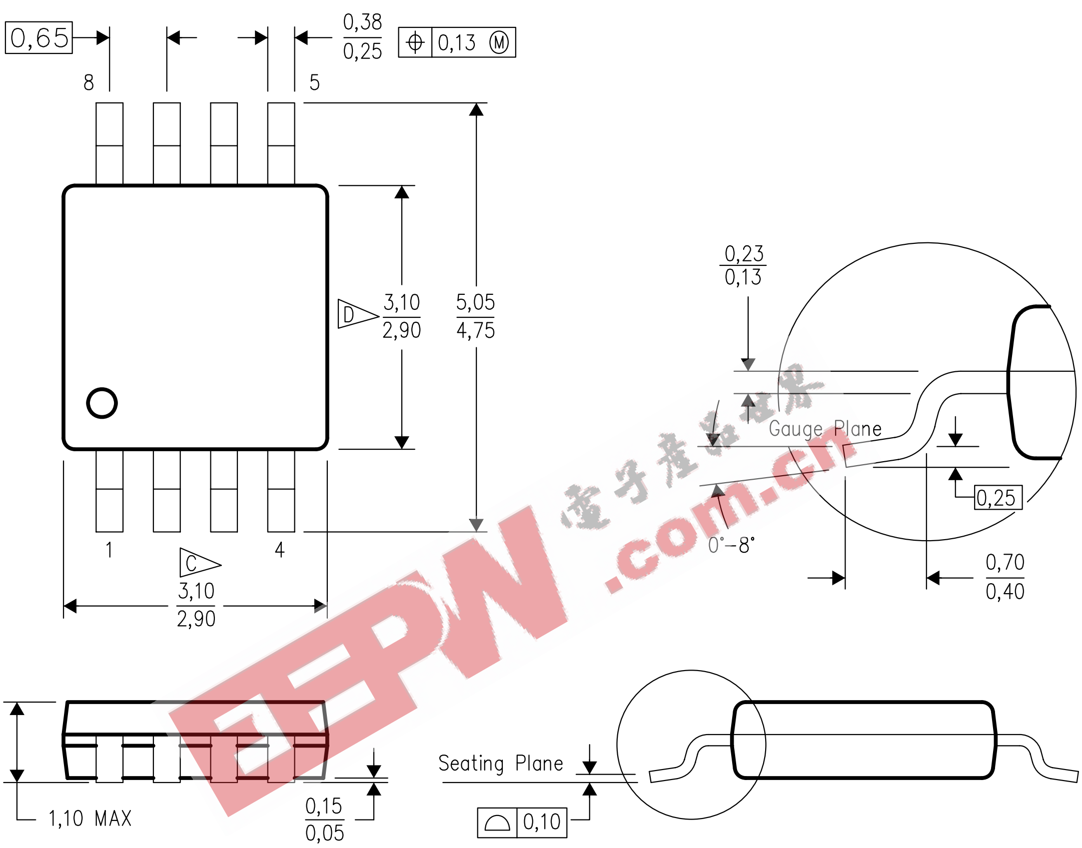
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265