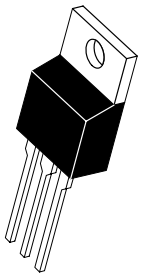
Complementary Silicon Power Transistors

NPN
D44VH
PNP
D45VH

These complementary silicon power transistors are designed for high–speed switching applications, such as switching regulators and high frequency inverters. The devices are also well–suited for drivers for high power switching circuits.

- Fast Switching —
  t_f = 90 ns (Max)
- Key Parameters Specified @ 100°C
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Complementary Pairs Simplify Circuit Designs

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 VOLTS
83 WATTS



CASE 221A–09
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Emitter Voltage	V_{CEV}	100	Vdc
Emitter Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	83 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(2) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

NOTE: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.

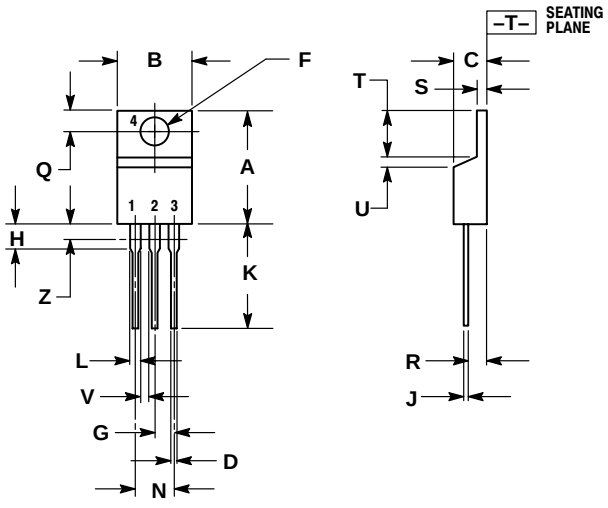
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (2) (I_C = 25 mAdc, I_B = 0)		$V_{CEO(sus)}$	80	—	—	Vdc
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc) (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 10 100	µAdc
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	—	10	µAdc
ON CHARACTERISTICS (2)						
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 35 20	 — —	 — —	—
Collector–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc) (I_C = 8.0 Adc, I_B = 0.8 Adc) (I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)	 D44VH10 D45VH10 D44VH10 D45VH10	$V_{CE(sat)}$	 — — — —	 — — — —	 0.4 1.0 0.8 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc) (I_C = 8.0 Adc, I_B = 0.8 Adc) (I_C = 8.0 Adc, I_B = 0.4 Adc, T_C = 100°C) (I_C = 8.0 Adc, I_B = 0.8 Adc, T_C = 100°C)	 D44VH10 D45VH10 D44VH10 D45VH10	$V_{BE(sat)}$	 — — — —	 — — — —	 1.2 1.0 1.1 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	—	50	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f_{test} = 1.0 MHz)	 D44VH10 D45VH10	C_{ob}	 — —	 120 275	 — —	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 20 Vdc, I_C = 8.0 Adc, I_{B1} = I_{B2} = 0.8 Adc)	t_d	—	—	50	ns
Rise Time		t_r	—	—	250	
Storage Time		t_s	—	—	700	
Fall Time		t_f	—	—	90	

(2) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS

TO–220AB
CASE 221A–09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

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