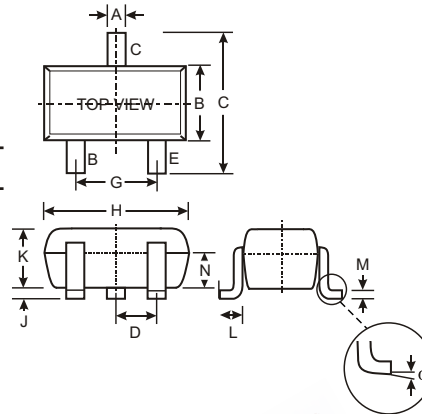


### Features

- Epitaxial Planar Die Construction
- Complementary PNP Types Available (DDTA)
- Built-In Biasing Resistor, R1 only
- Lead Free/RoHS Compliant (Note 2)

### Mechanical Data

- Case: SOT-523
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals: Solderable per MIL-STD-202, Method 208
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe).
- Terminal Connections: See Diagram
- Marking: Date Code and Marking Code (See Diagrams & Page 2)
- Weight: 0.002 grams (approx.)
- Ordering Information (See Page 2)



SOT-523			
Dim	Min	Max	Typ
A	0.15	0.30	0.22
B	0.75	0.85	0.80
C	1.45	1.75	1.60
D			0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
J	0.00	0.10	0.05
K	0.60	0.80	0.75
L	0.10	0.30	0.22
M	0.10	0.20	0.12
N	0.45	0.65	0.50
	0	8	
All Dimensions in mm			



SCHMATIC DIAGRAM

P/N	R1 (NOM)	MARKING
DDTC113TE	1K	N01
DDTC123TE	2.2K	N03
DDTC143TE	4.7K	N07
DDTC114TE	10K	N12
DDTC124TE	22K	N16
DDTC144TE	47K	N19
DDTC115TE	100K	N23
DDTC125TE	200K	N25

### Maximum Ratings @ T<sub>A</sub> = 25 C unless otherwise specified

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	V
Collector-Emitter Voltage	V <sub>CEO</sub>	50	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current	I <sub>C</sub> (Max)	100	mA
Power Dissipation	P <sub>d</sub>	150	mW
Thermal Resistance, Junction to Ambient Air (Note 1)	R <sub>JA</sub>	833	C/W
Operating and Storage and Temperature Range	T <sub>j</sub> , T <sub>STG</sub>	-55 to +150	C

- Note:
- Mounted on FR4 PC Board with recommended pad layout at <http://www.diodes.com/datasheets/ap02001.pdf>.
  - No purposefully added lead

**Electrical Characteristics** @ T<sub>A</sub> = 25 C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV <sub>CBO</sub>	50			V	I <sub>C</sub> = 50 A
Collector-Emitter Breakdown Voltage	BV <sub>CEO</sub>	50			V	I <sub>C</sub> = 1mA
Emitter-Base Breakdown Voltage	BV <sub>EBO</sub>	5			V	I <sub>E</sub> = 50 A
Collector Cutoff Current	I <sub>CBO</sub>			0.5	A	V <sub>CB</sub> = 50V
Emitter Cutoff Current	I <sub>EBO</sub>			0.5	A	V <sub>EB</sub> = 4V
Collector-Emitter Saturation Voltage	V <sub>CE(sat)</sub>			0.3	V	I <sub>C</sub> /I <sub>B</sub> = 10mA/1mA DDTC113TE I <sub>C</sub> /I <sub>B</sub> = 5mA/0.5mA DDTC123TE I <sub>C</sub> /I <sub>B</sub> = 2.5mA/.25mA DDTC143TE I <sub>C</sub> /I <sub>B</sub> = 1mA/.1mA DDTC114TE I <sub>C</sub> /I <sub>B</sub> = 5mA/0.5mA DDTC124TE I <sub>C</sub> /I <sub>B</sub> = 2.5mA/.25mA DDTC144TE I <sub>C</sub> /I <sub>B</sub> = 1mA/0.1mA DDTC115TE I <sub>C</sub> /I <sub>B</sub> = .5mA/.05mA DDTC125TE
DC Current Transfer Ratio	h <sub>FE</sub>	100	250	600		I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V
Input Resistor (R <sub>1</sub> ) Tolerance	R <sub>1</sub>	-30		+30	%	
Gain-Bandwidth Product*	f <sub>T</sub>		250		MHz	V <sub>CE</sub> = 10V, I <sub>E</sub> = -5mA, f = 100MHz

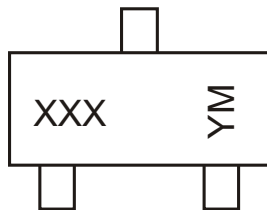
\* Transistor - For Reference Only

**Ordering Information** (Note 3)

Device	Packaging	Shipping
DDTC113TE-7-F	SOT-523	3000/Tape & Reel
DDTC123TE-7-F	SOT-523	3000/Tape & Reel
DDTC143TE-7-F	SOT-523	3000/Tape & Reel
DDTC114TE-7-F	SOT-523	3000/Tape & Reel
DDTC124TE-7-F	SOT-523	3000/Tape & Reel
DDTC144TE-7-F	SOT-523	3000/Tape & Reel
DDTC115TE-7-F	SOT-523	3000/Tape & Reel
DDTC125TE-7-F	SOT-523	3000/Tape & Reel

Notes: 3. For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

**Marking Information**



XXX = Product Type Marking Code  
See Sheet 1 Diagrams  
YM = Date Code Marking  
Y = Year ex: N = 2002  
M = Month ex: 9 = September

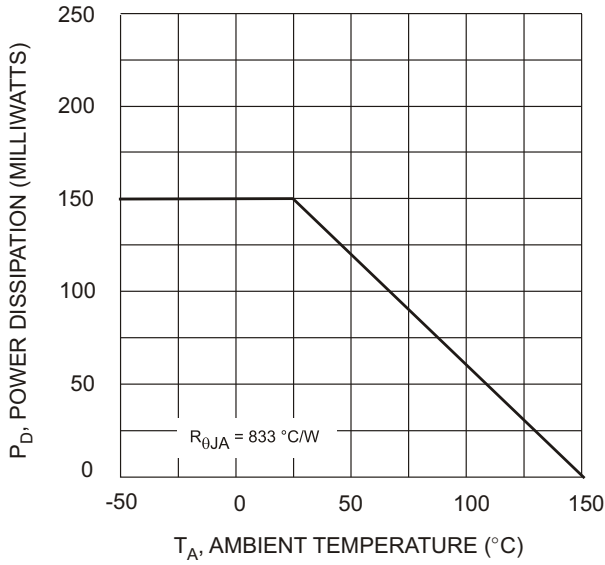
Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

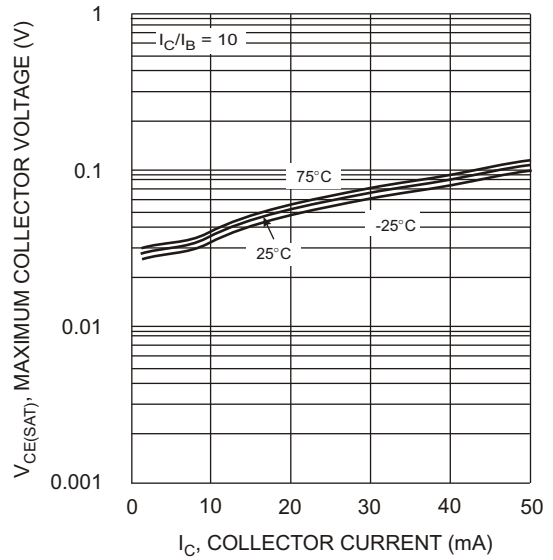
Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

TYPICAL CURVES - DDTC114TE

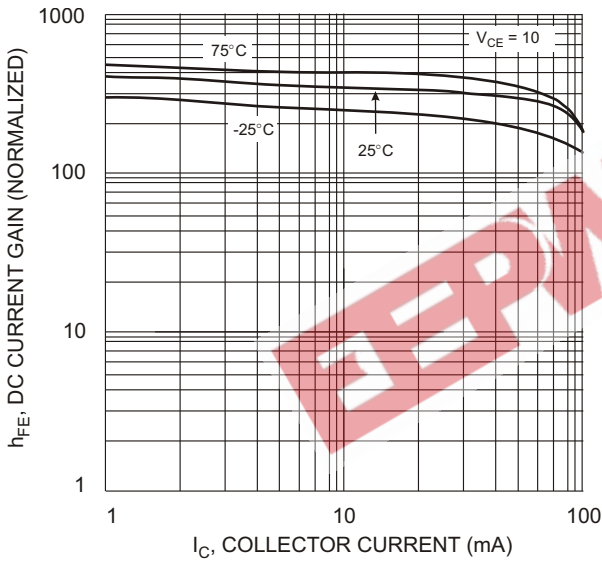
NEW PRODUCT



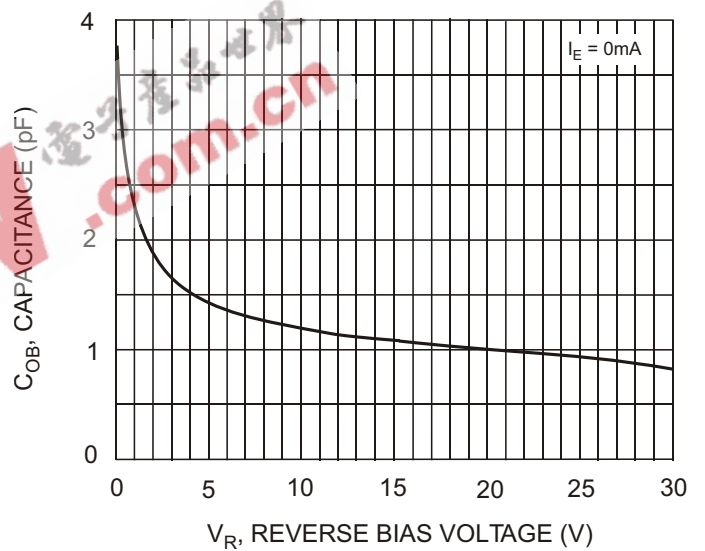
$T_A$ , AMBIENT TEMPERATURE ( $^\circ\text{C}$ )  
Fig. 1 Derating Curve



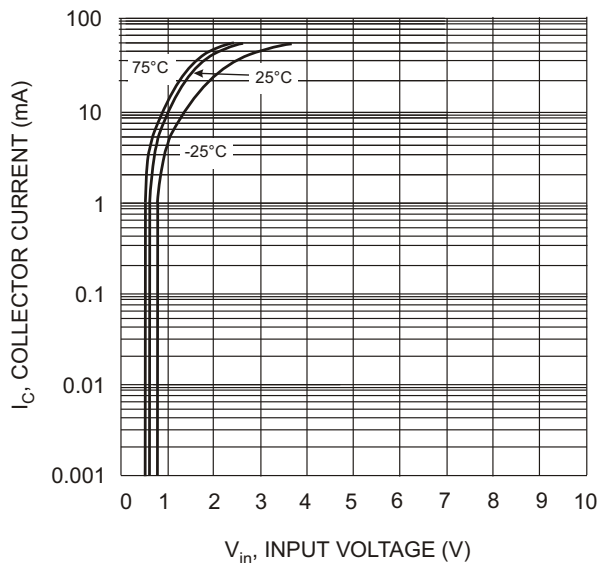
$I_C$ , COLLECTOR CURRENT (mA)  
Fig. 2  $V_{CE(SAT)}$  vs.  $I_C$



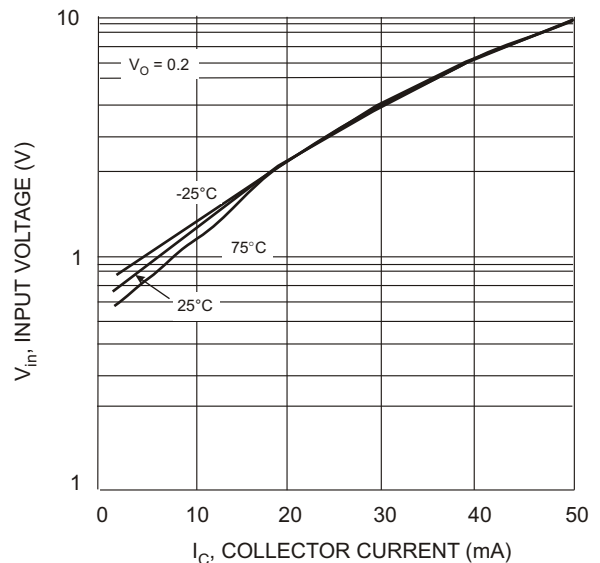
$I_C$ , COLLECTOR CURRENT (mA)  
Fig. 3 DC Current Gain



$V_R$ , REVERSE BIAS VOLTAGE (V)  
Fig. 4 Output Capacitance



$V_{in}$ , INPUT VOLTAGE (V)  
Fig. 5 Collector Current Vs. Input Voltage



$I_C$ , COLLECTOR CURRENT (mA)  
Fig. 6 Input Voltage vs. Collector Current

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