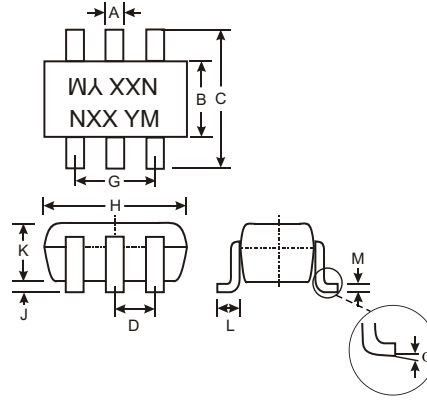


Features

- Epitaxial Planar Die Construction
- Complementary PNP Types Available (DDA)
- Built-In Biasing Resistors

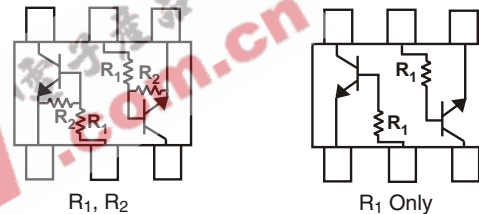
Mechanical Data

- Case: SOT-26, Molded Plastic
- Case material - UL Flammability Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020A
- Terminals: Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Marking: Date Code and Marking Code (See Diagrams & Page 3)
- Weight: 0.015 grams (approx.)
- Ordering Information (See Page 3)



SOT-26			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	0.95		
G	1.90		
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
α	0°	8°	—
All Dimensions in mm			

P/N	R1	R2	MARKING
DDC124EK	22K Ω	22K Ω	N17
DDC144EK	47K Ω	47K Ω	N20
DDC114YK	10K Ω	47K Ω	N14
DDC123JK	2.2K Ω	47K Ω	N06
DDC114EK	10K Ω	10K Ω	N13
DDC143TK	4.7K Ω	-	N07
DDC114TK	10K Ω	-	N12



SCHEMATIC DIAGRAM

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage, (3) to (1)	V_{CC}	50	V
Input Voltage, (2) to (1)	V_{IN}	-10 to +40 -10 to +40 -6 to +40 -5 to +12 -10 to +40 -5 V_{max} -5 V_{max}	V
Output Current	I_O	30 30 70 100 50 100 100	mA
Output Current	I_C (Max)	100	mA
Power Dissipation (Total)	P_d	300	mW
Thermal Resistance, Junction to Ambient Air (Note 1)	$R_{\theta JA}$	416.7	$^\circ\text{C/W}$
Operating and Storage and Temperature Range	T_j, T_{STG}	-55 to +150	$^\circ\text{C}$

- Note: 1. Mounted on FR4 PC Board with recommended pad layout at <http://www.diodes.com/datasheets/ap02001.pdf>.
2. 200mW per element must not be exceeded.

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic (DDC143TK & DDC114TK only)	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV_{CBO}	50	—	—	V	$I_C = 50\mu\text{A}$
Collector-Emitter Breakdown Voltage	BV_{CEO}	50	—	—	V	$I_C = 1\text{mA}$
Emitter-Base Breakdown Voltage	BV_{EBO}	5	—	—	V	$I_E = 50\mu\text{A}$
Collector Cutoff Current	I_{CBO}	—	—	0.5	μA	$V_{CB} = 50\text{V}$
Emitter Cutoff Current	I_{EBO}	—	—	0.5	μA	$V_{EB} = 4\text{V}$
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	—	—	0.3	V	$I_C/I_B = 2.5\text{mA} / 0.25\text{mA}$ DDC143TK $I_C/I_B = 1\text{mA} / 0.1\text{mA}$ DDC114TK
DC Current Transfer Ratio	h_{FE}	100	250	600	—	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$
Input Resistor (R_1) Tolerance	ΔR_1	-30	—	+30	%	—
Gain-Bandwidth Product*	f_T	—	250	—	MHZ	$V_{CE} = 10\text{V}, I_E = -5\text{mA}, f = 100\text{MHZ}$

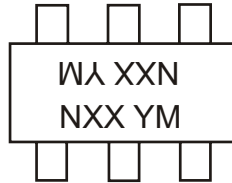
Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
Input Voltage	DDC124EK DDC144EK DDC114YK DDC123JK DDC114EK	$V_{I(off)}$	0.5	1.1	—	V	$V_{CC} = 5\text{V}, I_O = 100\mu\text{A}$
	DDC124EK DDC144EK DDC114YK DDC123JK DDC114EK		$V_{I(on)}$	—	1.9		
Output Voltage	DDC124EK DDC144EK DDC114YK DDC123JK DDC114EK	$V_{O(on)}$		—	0.1	0.3	V
	DDC124EK DDC144EK DDC114YK DDC123JK DDC114EK		I_I	—	—	0.36	
Input Current	DDC124EK DDC144EK DDC114YK DDC123JK DDC114EK	I_I		—	—	0.18	mA
Output Current	DDC124EK DDC144EK DDC114YK DDC123JK DDC114EK		$I_O(off)$	—	—	0.88	
DC Current Gain	DDC124EK DDC144EK DDC114YK DDC123JK DDC114EK	G_I		—	—	3.6	—
Input Resistor (R_1) Tolerance	ΔR_1		-30	—	+30	%	
Resistance Ratio Tolerance	R_2/R_1	-20	—	+20	%	—	
Gain-Bandwidth Product*	f_T	—	250	—	MHZ	$V_{CE} = 10\text{V}, I_E = 5\text{mA}, f = 100\text{MHZ}$	

* Transistor - For Reference Only

Ordering Information (Note 3)

Device	Packaging	Shipping
DDC124EK-7	SOT-26	3000/Tape & Reel
DDC144EK-7	SOT-26	3000/Tape & Reel
DDC114YK-7	SOT-26	3000/Tape & Reel
DDC123JK-7	SOT-26	3000/Tape & Reel
DDC114EK-7	SOT-26	3000/Tape & Reel
DDC143TK-7	SOT-26	3000/Tape & Reel
DDC114TK-7	SOT-26	3000/Tape & Reel

Notes: 3. For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

Marking Information

NXX = Product Type Marking Code
See Sheet 1 Diagrams
YM = Date Code Marking
Y = Year ex: N = 2002
M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

TYPICAL CURVES - DDC123JK
ONE SECTION

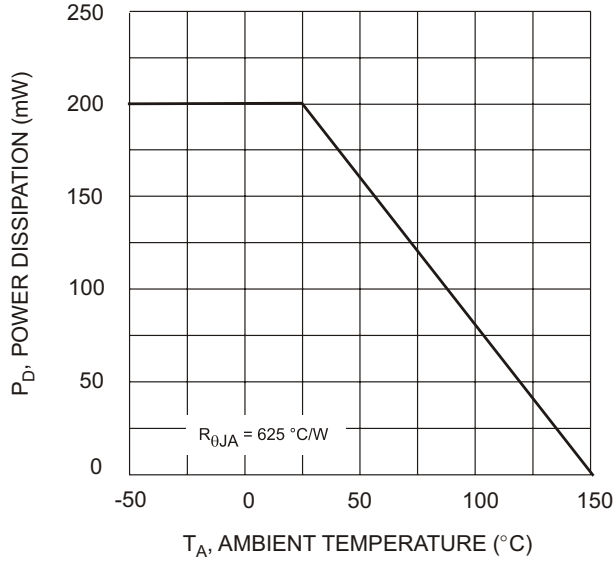


Fig. 1 Derating Curve

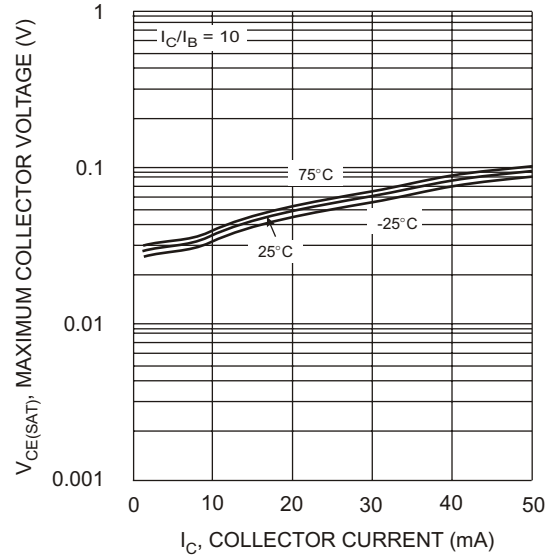


Fig. 2 $V_{CE(SAT)}$ vs. I_C

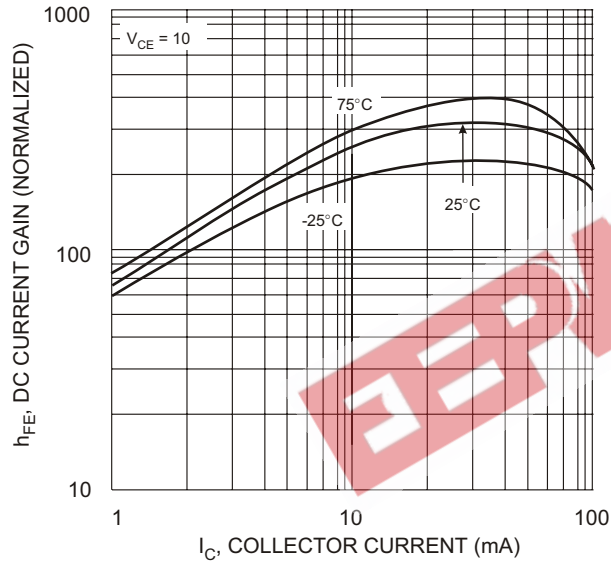


Fig. 3 DC Current Gain

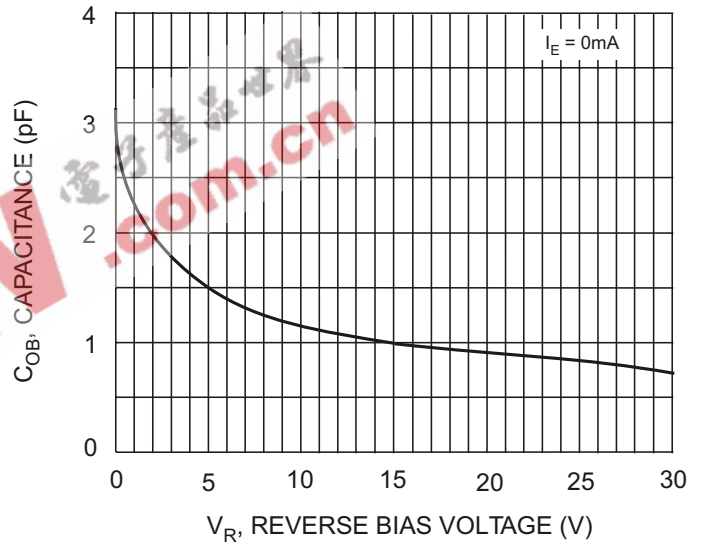


Fig. 4 Output Capacitance

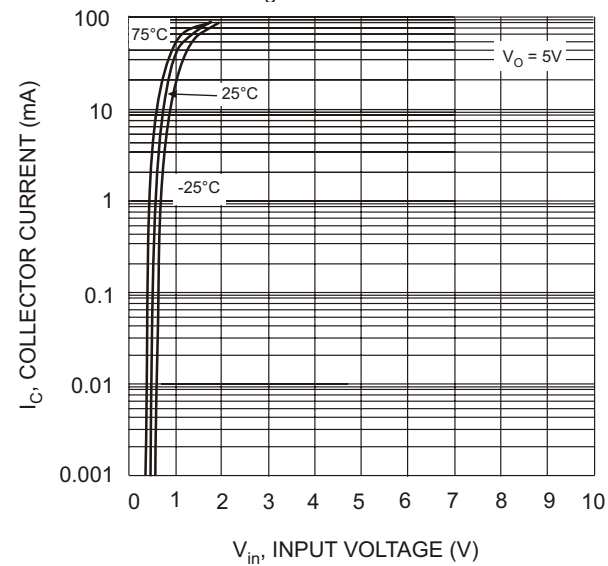


Fig. 5 Collector Current Vs. Input Voltage

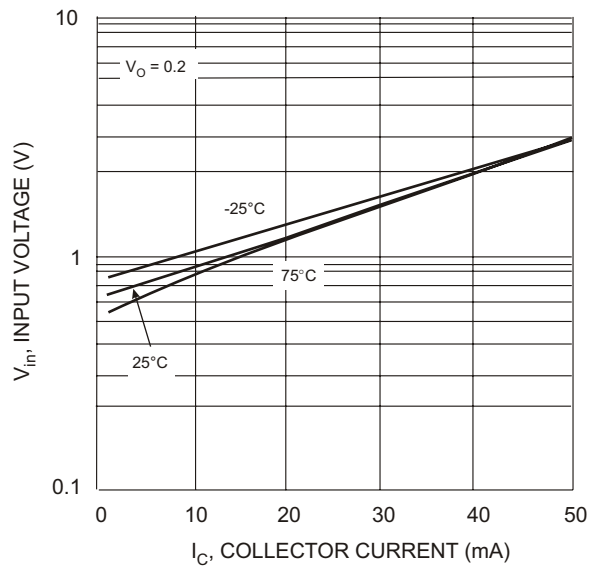


Fig. 6 Input Voltage vs. Collector Current

TYPICAL CURVES - DDC114TK

ONE SECTION

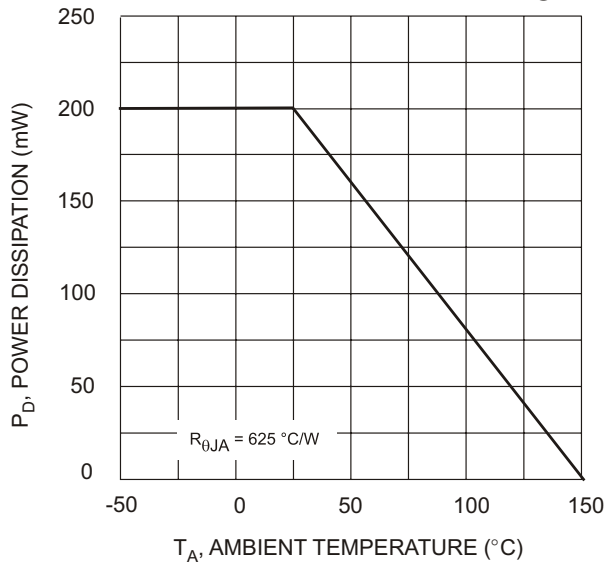


Fig. 1 Derating Curve

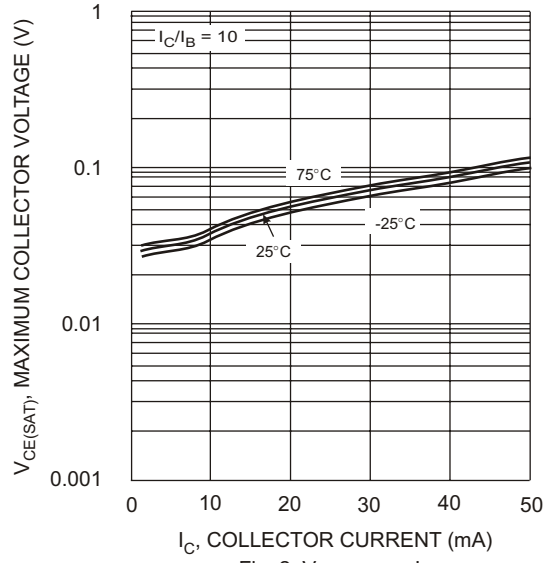


Fig. 2 $V_{CE(SAT)}$ vs. I_C

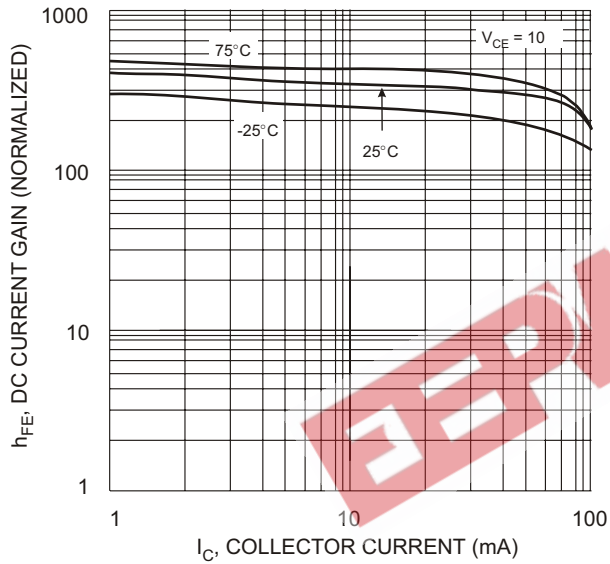


Fig. 3 DC Current Gain

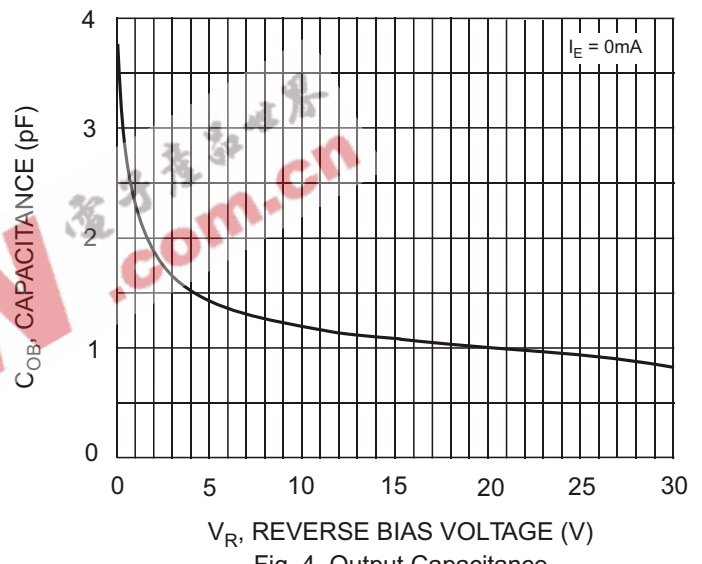


Fig. 4 Output Capacitance

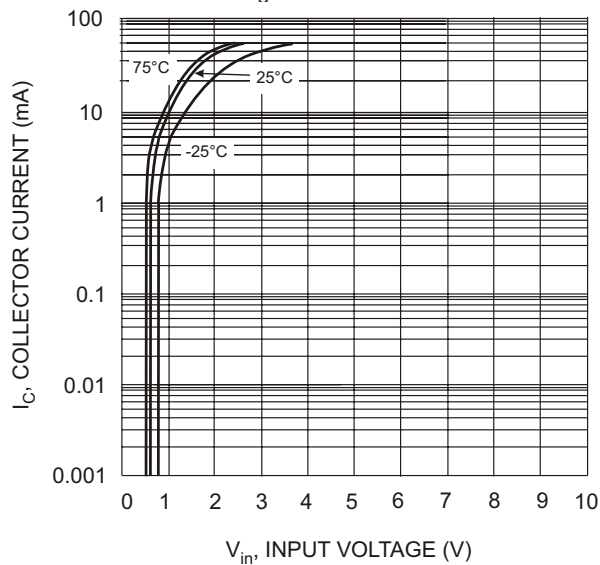


Fig. 5 Collector Current Vs. Input Voltage

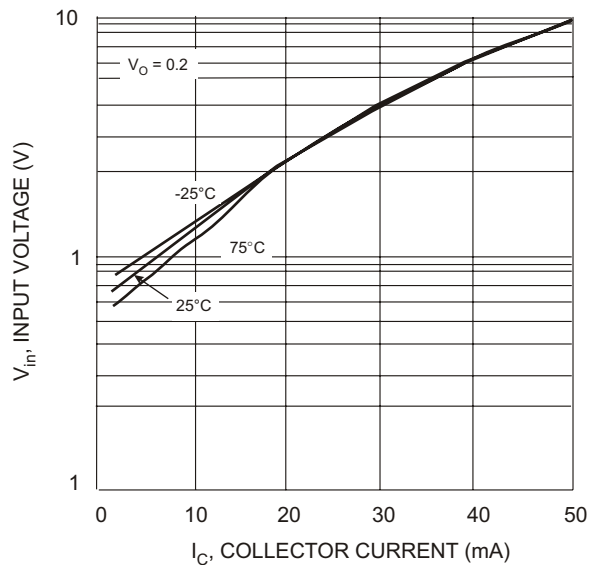


Fig. 6 Input Voltage vs. Collector Current