16-Bit, Single-Channel, ±18V Output (Unbuffered), Ultra-Low Power, Serial Interface DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **16-Bit Resolution**
- **Output: ±18V for ±18V Reference Input**
- **±18V Supply Operation**
- **Very Low Power**
- **High Accuracy INL: 1LSB**
- **Low Noise: 10nV/√Hz**
- **Fast Settling: 1μs to 1LSB**
- **Fast SPI™ Interface: Up To 50MHz**
- **16-Pin TSSOP Package**
- **Selectable Reset to Zero or Midscale**

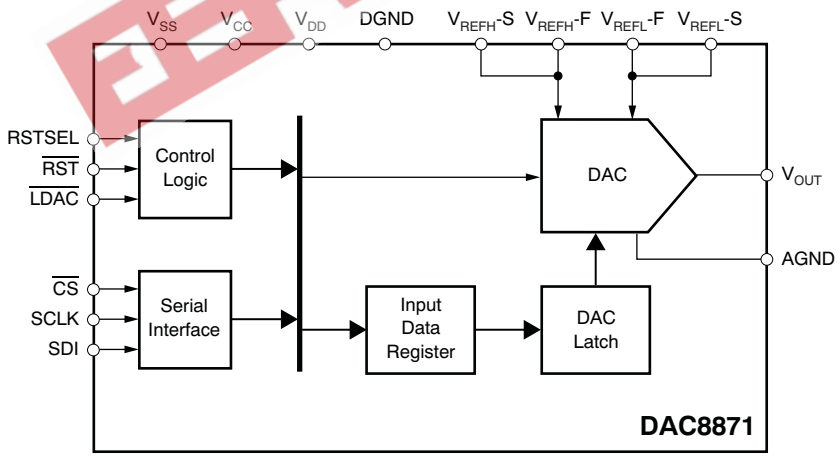
APPLICATIONS

- **Portable Equipment**
- **Automatic Test Equipment**
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Optical Networking**

DESCRIPTION

The DAC8871 is a 16-bit, single-channel, serial input, voltage output digital-to-analog converter (DAC). The output range is determined by the reference voltage, V_{REFH} and V_{REFL}. By properly selecting the reference, the output can be unipolar or bipolar, and up to ±18V. These converters provide excellent linearity (1LSB INL), low noise, and fast settling (1μs to 1LSB of full scale output) over the specified temperature range of –40°C to +105°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer. The device features a standard high-speed clock (up to 50MHz), and a 3V or 5V SPI serial interface to communicate with the DSP or microprocessors.

For optimum performance, a set of Kelvin connections to external reference are provided. The DAC8871 is available in a TSSOP-16 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE-LEAD	PACKAGE DESIGNATOR
DAC8871B	±1	±1	–40°C to +105°C	8871	TSSOP-16	PW
DAC8871	±3	±1	–40°C to +105°C	8871	TSSOP-16	PW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted).

		DAC8871	UNIT
V_{DD} to GND		–0.3 to +7	V
Digital input voltage to GND		–0.3 to (V_{DD} + 0.3)	V
AGND to DGND		–0.3 to +0.3	V
V_{CC} to V_{SS}		–0.3 to +39.6	V
V_{CC} to AGND		–0.3 to +19.8	V
V_{SS} to AGND		+0.3 to –19.8	V
V_{REFH} to VREFL		–0.3 to +39.6	V
V_{REFH} to AGND		–0.3 to +19.8	V
V_{REFL} to AGND		–19.8 to +17.5	V
Operating temperature range		–40 to +105	°C
Storage temperature range		–65 to +150	°C
Maximum junction temperature (T_J max)		+150	°C
Power dissipation		(T_J max - T_A)/θ_{JA}	W
Thermal impedance, θ_{JA}	TSSOP-16	161.4	°C/W

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, and V_{DD} = +5V, unless otherwise noted; specifications subject to change without notice.

PARAMETER			CONDITIONS	DAC8871 MIN	DAC8871 TYP	DAC8871 MAX	UNIT
STATIC PERFORMANCE							
	Resolution			16			Bits
	Linearity error	DAC8871B	V_{REFH} = 10V, V_{REFL} = –5V		±0.75	±1	LSB
			V_{REFH} = 10V, V_{REFL} = –10V		±1	±1.5	LSB
		DAC8871			±1	±3	LSB
	Differential linearity error				±0.25	±1	LSB
	Gain error		T_A = +25°C		±0.5	±2	LSB
	Gain drift				±0.1		ppm/°C
	Bipolar zero error		T_A = +25°C		±1	±4	LSB
	Bipolar drift				±0.1		ppm/°C
	Zero code error		T_A = +25°C		±0.5	±2	LSB
	Zero code drift				±0.05		ppm/°C
OUTPUT CHARACTERISTICS							
	Voltage output			V_{REFL}		V_{REFH}	V
	Output impedance				6.25		kΩ
	Settling time		To 1LSB of FS, C_L = 15 pF		1		µs
	Slew rate(1)		C_L = 15pF		40		V/µs
	Digital feedthrough(2)				0.2		nV-s
	Output noise		T_A = +25°C		10		nV/√Hz
	Power supply rejection		Supplies vary ±10%			±1	LSB
REFERENCE INPUT							
V_{REFH}	Ref high input voltage range			0		+18	V
V_{REFL}	Ref low input voltage range			–18		V_{REFH} – 1.25	V
	Ref high input current				1.3		mA
	Ref low input current				–1.3		mA
	Reference input impedance(3)			7.5			kΩ
	Reference input capacitance		Code = 0000h		75		pF
			Code = FFFFh		120		pF
DIGITAL INPUTS							
V_{IL}	Input low voltage		V_{DD} = +5V	DGND		0.8	V
			V_{DD} = +3V	DGND		0.6	V
V_{IH}	Input high voltage		V_{DD} = +5V	2.6		V_{DD}	V
			V_{DD} = +3V	2.1		V_{DD}	V
	Input current					±1	µA
	Input capacitance					10	pF

(1) Slew Rate is measure from 10% to 90% of transition when the output changes from 0 to full scale.
(2) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change; $\overline{CS}$ is held high, while SCLK and DIN signals are toggled. It is specified with a full-scale code change on the SDI bus (that is, from all 0s to all 1s and vise versa).
(3) Reference input resistance is code-dependent, with a minimum at 8555h

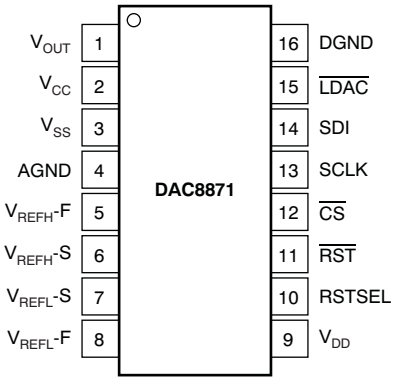
ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, and V_{DD} = +5V, unless otherwise noted; specifications subject to change without notice.

PARAMETER	CONDITIONS	DAC8871			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
V_{CC}		+13.5	+15	+19.8	V
V_{SS}		–19.8	–15	–13.5	V
V_{DD}		+2.7		+5.5	V
I_{CC}			0.01	2	µA
I_{SS}			–0.01	–2	µA
I_{DD}			3	10	µA
Power			15	30	µW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

PIN CONFIGURATION (NOT TO SCALE)

PW PACKAGE
TSSOP-16
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	V_{OUT}	Analog output of the DAC
2	V_{CC}	Positive analog power supply: +15V
3	V_{SS}	Negative analog power supply: –15V
4	AGND	Analog ground
5	V_{REFH}-F	V_{REFH} reference input (Force). Connect to external V_{REFH}.
6	V_{REFH}-S	V_{REFH} reference input (Sense). Connect to external V_{REFH}.
7	V_{REFL}-S	V_{REFL} reference input (Sense). Connect to external V_{REFL}.
8	V_{REFL}-F	V_{REFL} reference input (Force). Connect to external V_{REFL}.
9	V_{DD}	Digital power. +5V for 5V interface logic; +3V for 3V logic.
10	RSTSEL	Power-On-Reset select. Determines V_{OUT} after power-on reset. If tied to V_{DD}, the DAC latch is set to mid-scale after power-on, and V_{OUT} is (V_{REFH}– V_{REFL})/2. If tied to DGND, the DAC latch is cleared ('0'), and V_{OUT} is V_{REFL}.
11	$\overline{RST}$	Reset (active low)
12	$\overline{CS}$	Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low.
13	SCLK	Serial clock input
14	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
15	$\overline{LDAC}$	Load DAC control input (active low). When $\overline{LDAC}$ is low, the DAC latch is simultaneously updated with the content of the input register.
16	DGND	Digital ground

TIMING DIAGRAMS

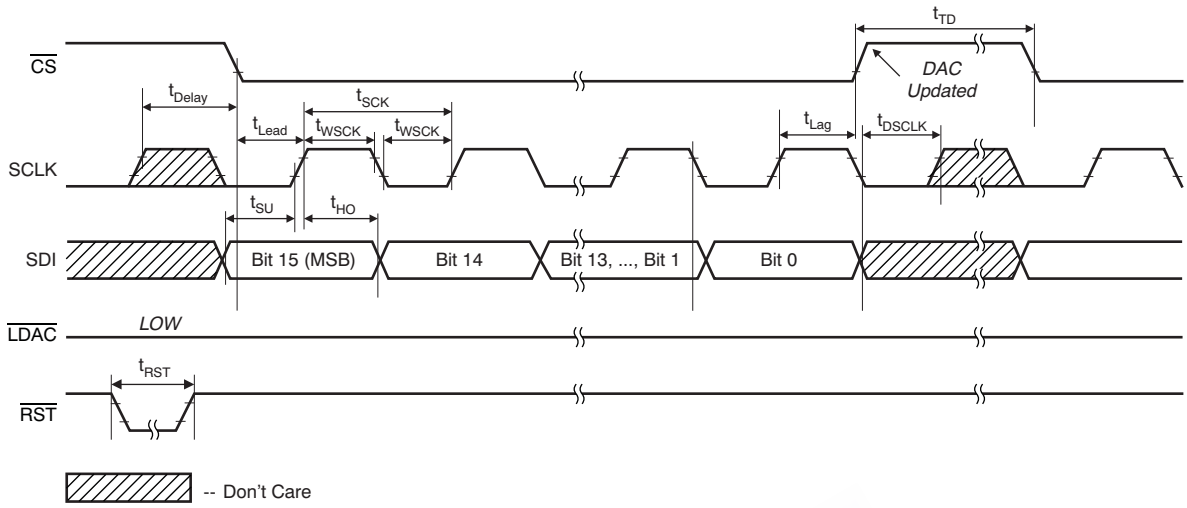


Figure 1. Case 1—$\overline{\text{LDAC}}$ Tied Low

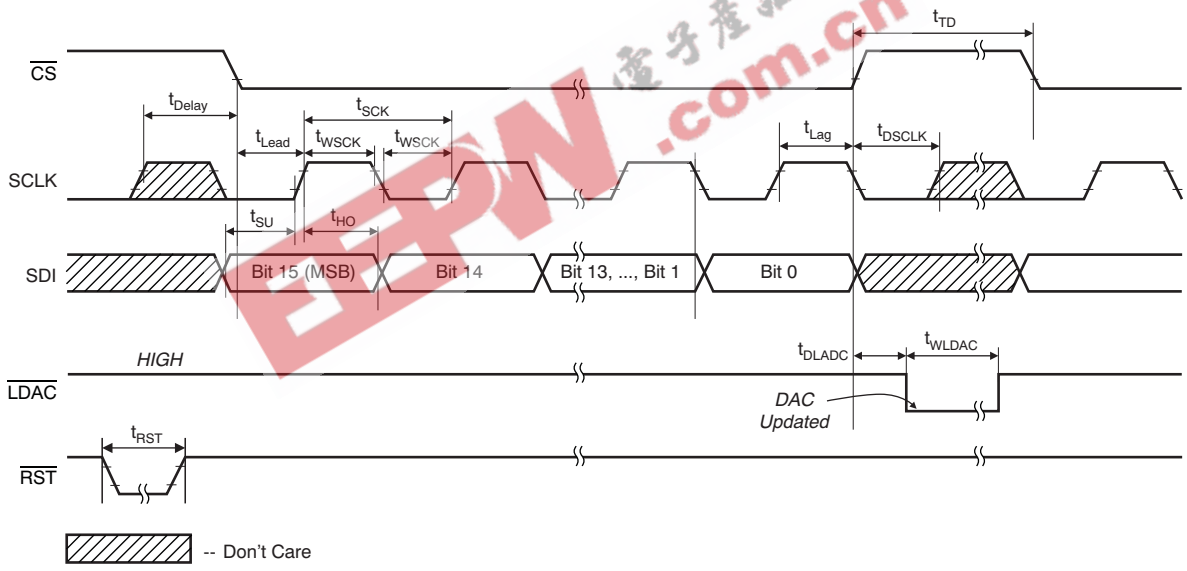


Figure 2. Case 2—$\overline{\text{LDAC}}$ Active

TIMING CHARACTERISTICS: V_{DD} = +5V(1)(2)

At –40°C to +105°C, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{SCK}	SCLK period	20		ns
t_{WSCK}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{CS}$ low	10		ns
t_{Lead}	$\overline{CS}$ enable lead time	10		ns
t_{Lag}	$\overline{CS}$ enable lag time	10		ns
t_{DSCLK}	Delay from $\overline{CS}$ high to SCLK high	10		ns
t_{TD}	$\overline{CS}$ high between active period	30		ns
t_{SU}	Data setup time (input)	10		ns
t_{HO}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{LDAC}$ width	30		ns
t_{DLDAC}	Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	30		ns
t_{RST}	Reset ($\overline{RST}$) low	10		ns
	V_{DD} high to $\overline{CS}$ low (power-up delay)	10		µs

(1) Assured by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, and V_{REFL} =–10V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

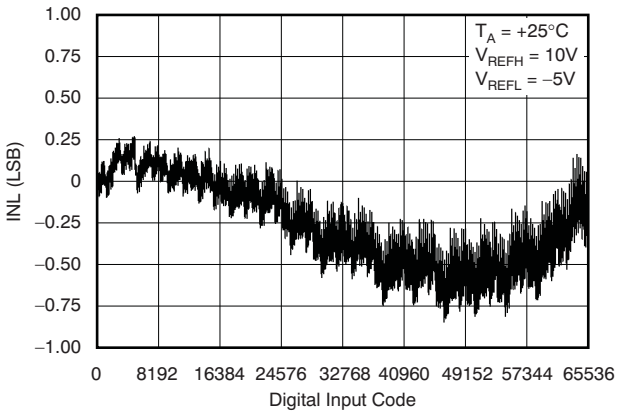


Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

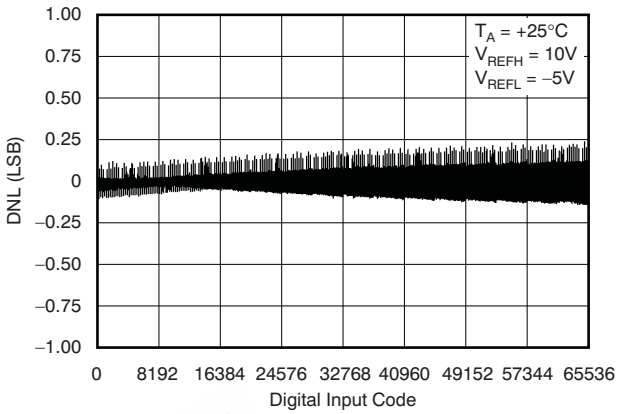


Figure 4.

LINEARITY ERROR vs DIGITAL INPUT CODE

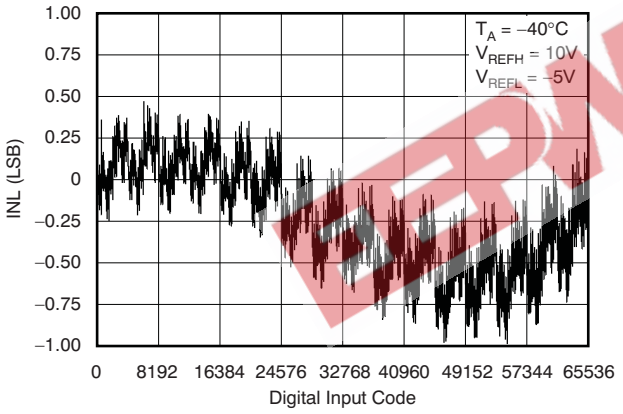


Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

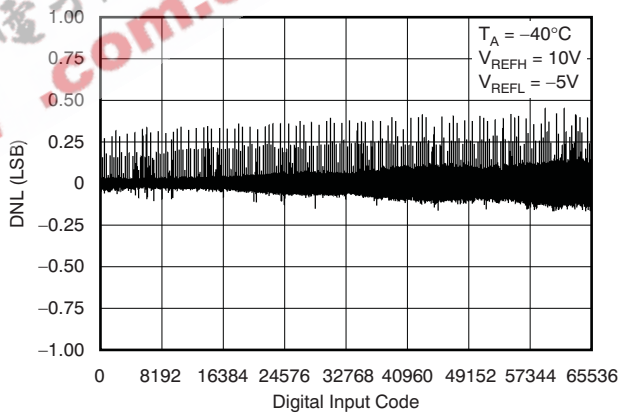


Figure 6.

LINEARITY ERROR vs DIGITAL INPUT CODE

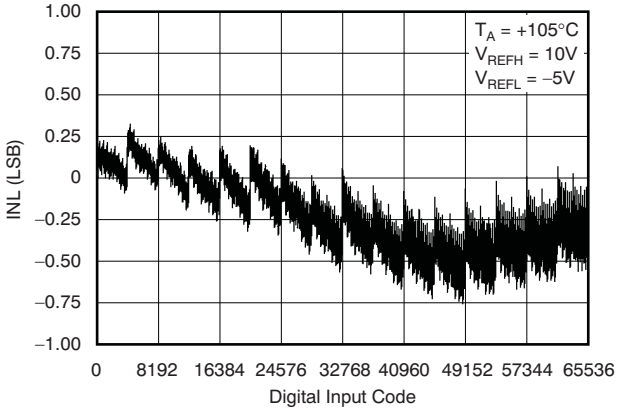


Figure 7.

DIFFERENTIAL LINEARY ERROR vs DIGITAL INPUT CODE

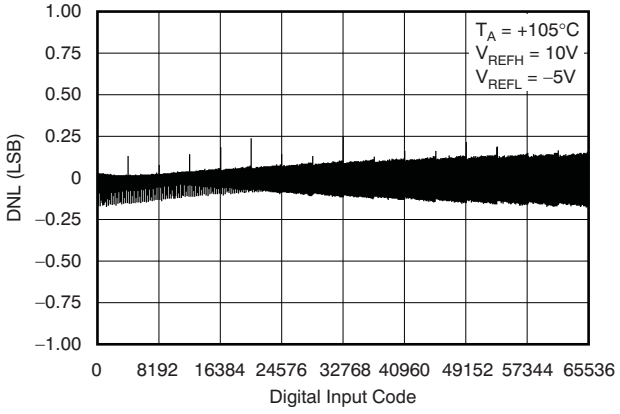


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, and V_{REFL} =–10V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

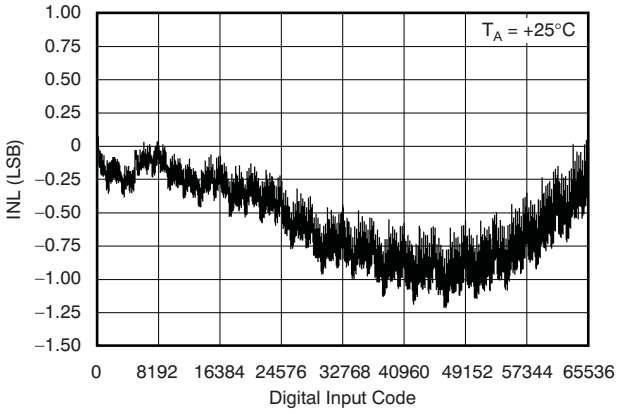


Figure 9.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

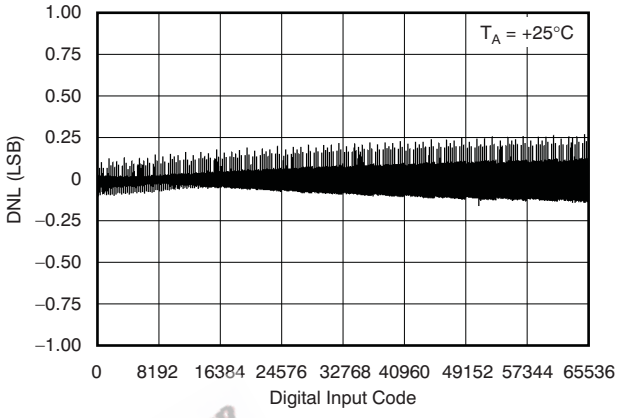


Figure 10.

LINEARITY ERROR vs DIGITAL INPUT CODE

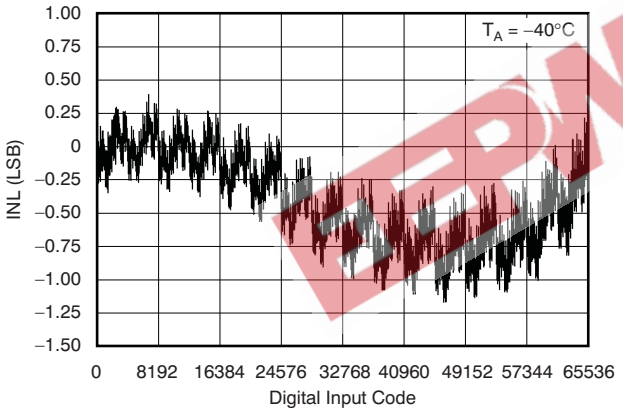


Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

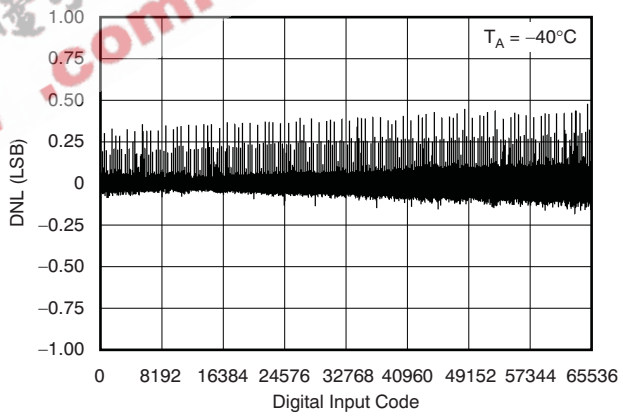


Figure 12.

LINEARITY ERROR vs DIGITAL INPUT CODE

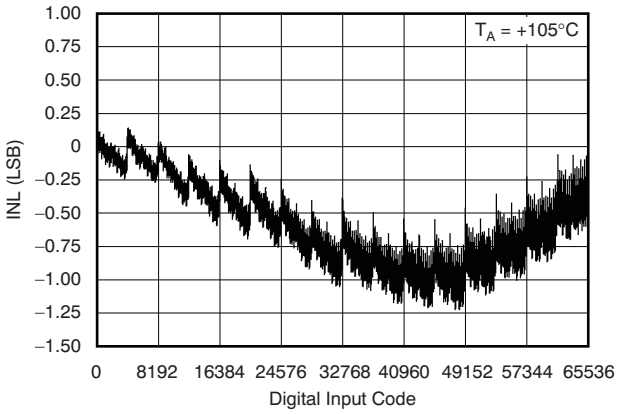


Figure 13.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

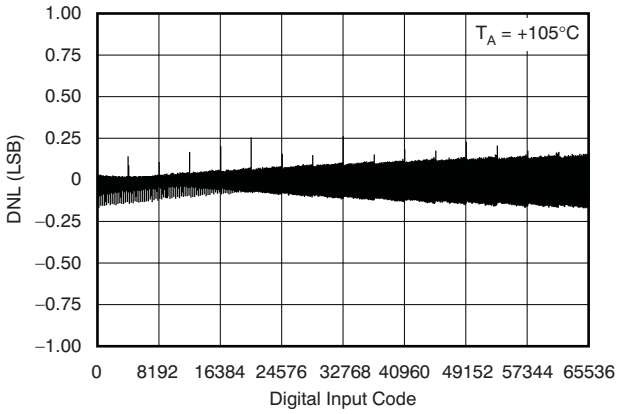


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, and V_{REFL} =–10V, unless otherwise noted.

LINEARITY ERROR
vs DIGITAL INPUT CODE

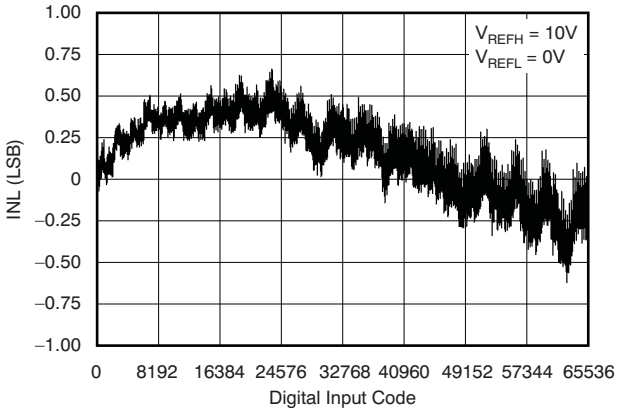


Figure 15.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

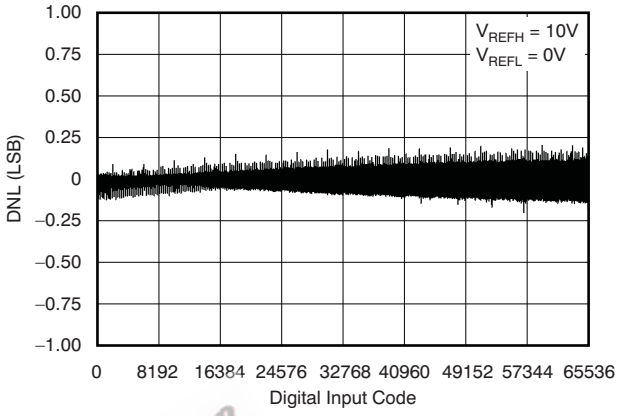


Figure 16.

LINEARITY ERROR
vs DIGITAL INPUT CODE

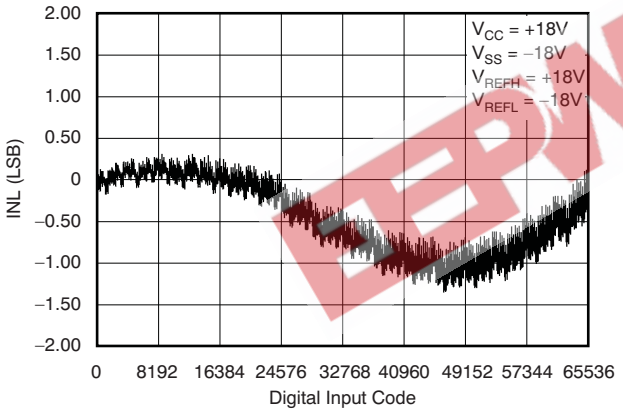


Figure 17.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

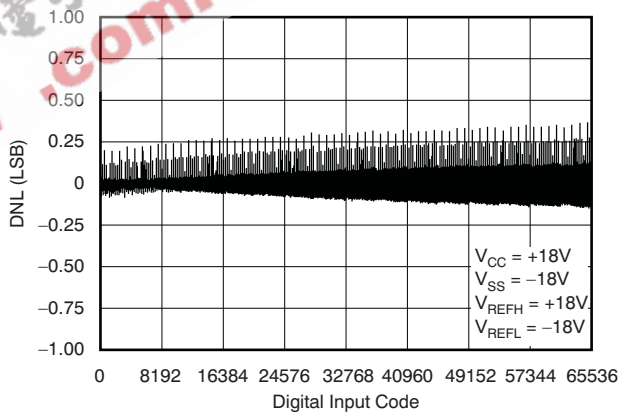


Figure 18.

INTEGRAL NONLINEARITY ERROR
vs REFERENCE VOLTAGE

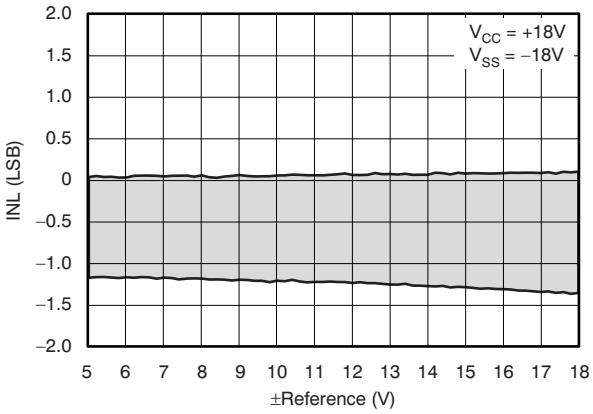


Figure 19.

DIFFERENTIAL NONLINEARITY ERROR
vs REFERENCE VOLTAGE

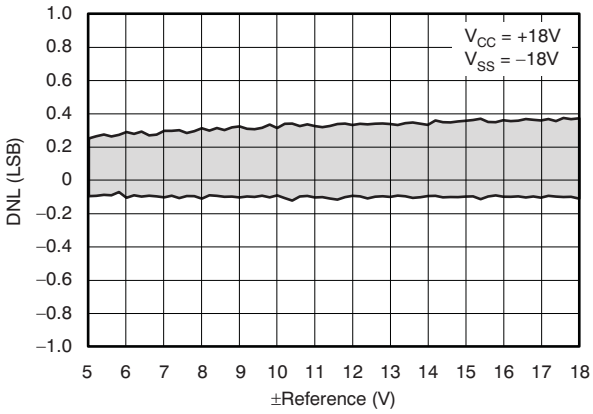


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, and V_{REFL} =–10V, unless otherwise noted.

INTEGRAL NONLINEARITY ERROR vs ANALOG SUPPLY VOLTAGE

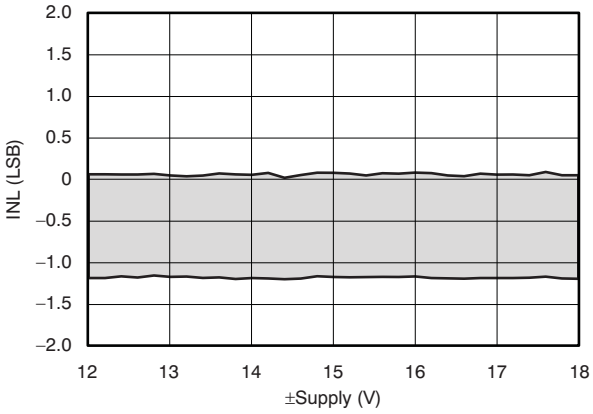


Figure 21.

DIFFERENTIAL NONLINEARITY ERROR vs ANALOG SUPPLY VOLTAGE

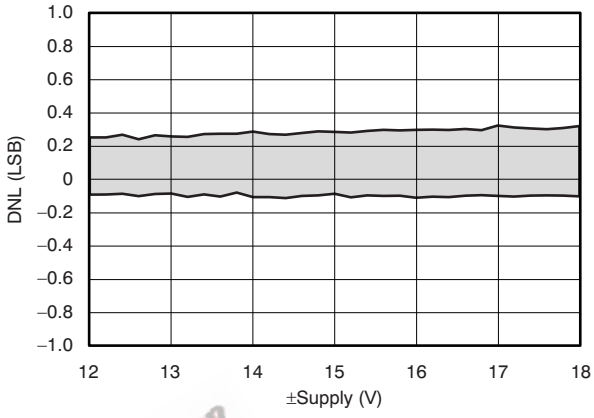


Figure 22.

GAIN ERROR vs TEMPERATURE

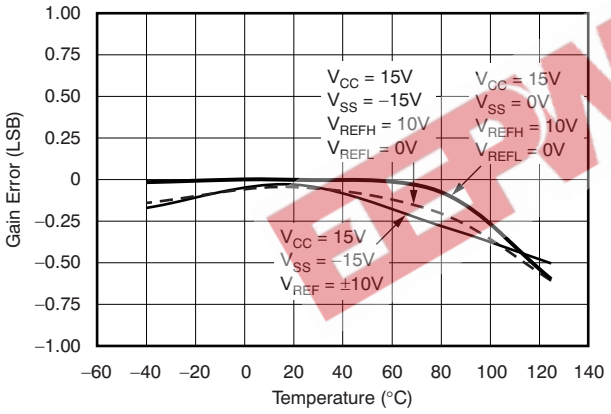


Figure 23.

ZERO-CODE ERROR vs TEMPERATURE

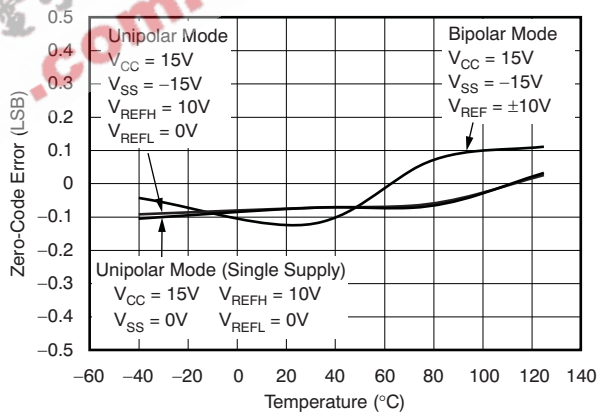


Figure 24.

BIPOLAR ZERO ERROR vs TEMPERATURE

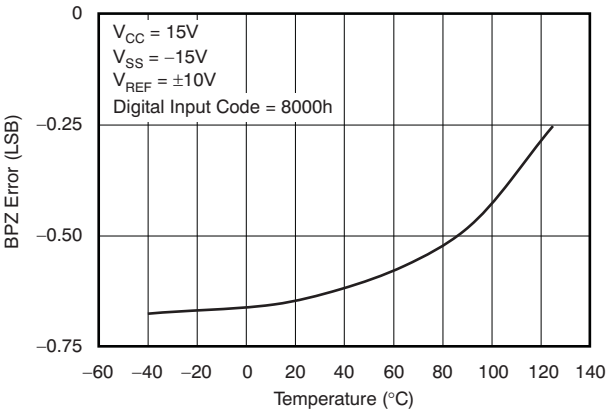


Figure 25.

SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE

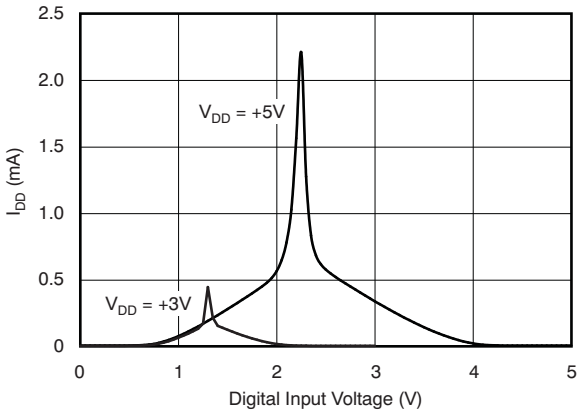


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, and V_{REFL} =–10V, unless otherwise noted.

DUAL REFERENCE CURRENT vs CODE

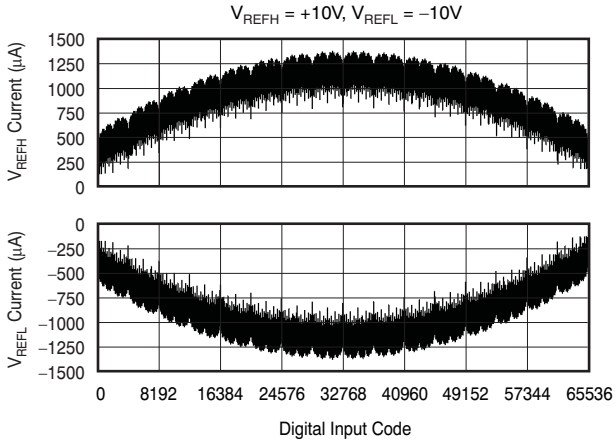


Figure 27.

SINGLE REFERENCE CURRENT vs CODE

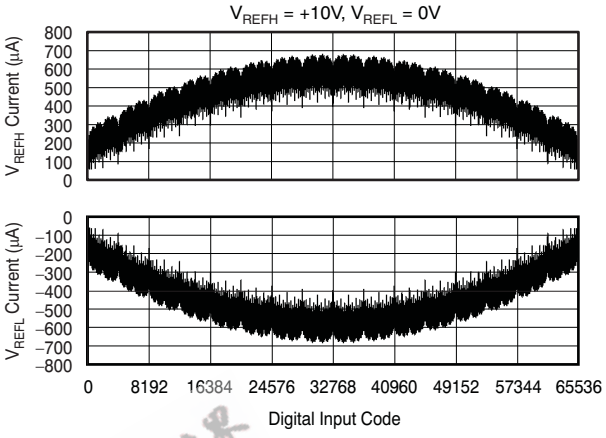


Figure 28.

SUPPLY CURRENTS vs TEMPERATURE

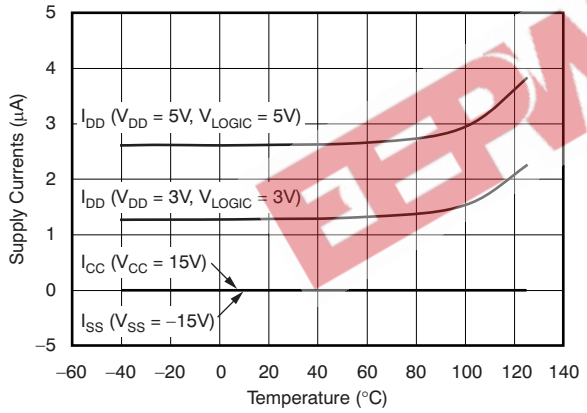


Figure 29.

DIGITAL SUPPLY CURRENT vs DIGITAL SUPPLY VOLTAGE

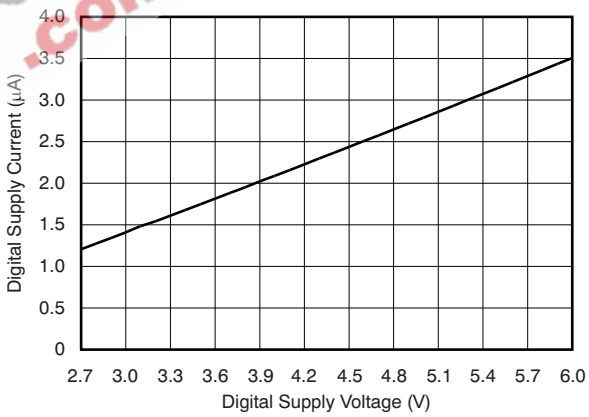


Figure 30.

ANALOG SUPPLY CURRENT vs ANALOG SUPPLY VOLTAGE

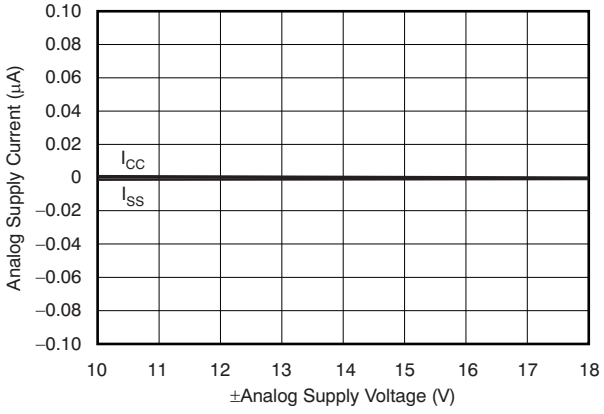


Figure 31.

SUPPLY CURRENTS vs REFERENCE VOLTAGES

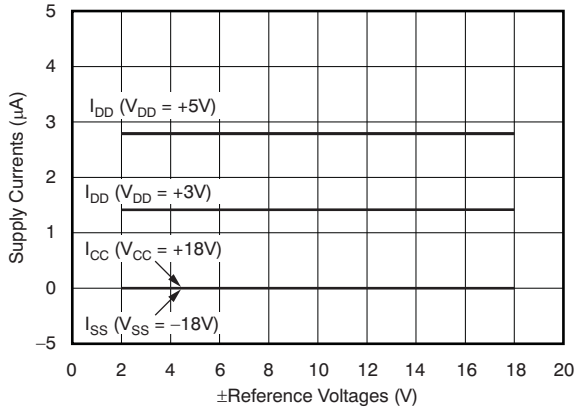


Figure 32.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, V_{REFH} = +10V, and V_{REFL} =–10V, unless otherwise noted.

MAJOR CARRY GLITCH (FALLING)

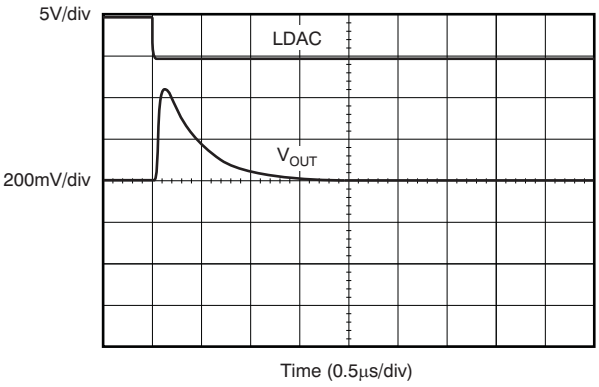


Figure 33.

MAJOR CARRY GLITCH (RISING)

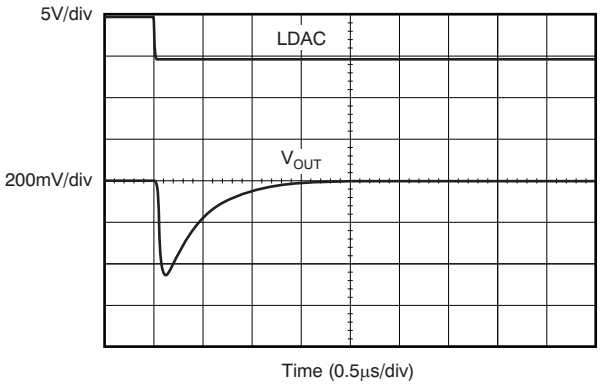


Figure 34.

DAC SETTLING TIME (FALLING)

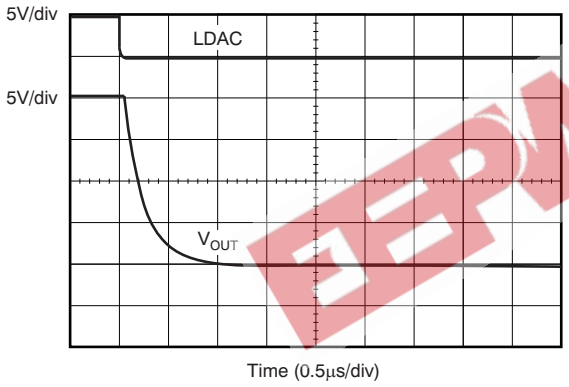


Figure 35.

DAC SETTLING TIME (RISING)

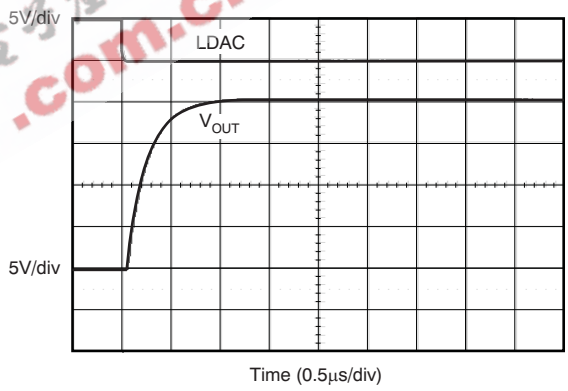


Figure 36.

BROADBAND NOISE

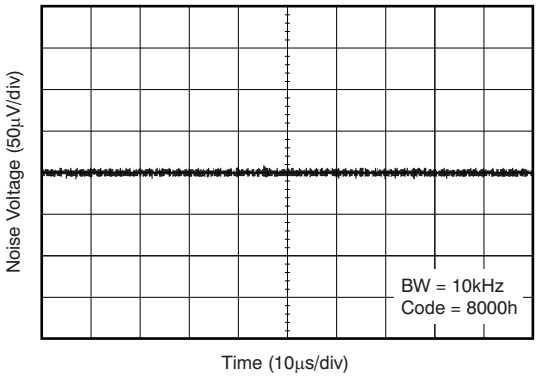


Figure 37.

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8871 is a 16-bit, single-channel, serial-input, voltage-output DAC. It operates from a dual power supply ranging from ±13.5V to ±19.8V, and typically consumes 10µA. The output range is from V_{REFL} to V_{REFH}. Data are written to this device in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, the DAC8871 is designed with a power-on reset function. After power on, the state of the RSTSEL pin sets the value of the input register and DAC latch, which sets the output state of the V_{OUT} pin. Refer to the Power-On Reset and Hardware Reset section for more details.

Kelvin sense connections for the reference and analog ground are also included.

DIGITAL-TO-ANALOG SECTIONS

The DAC architecture consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 38. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

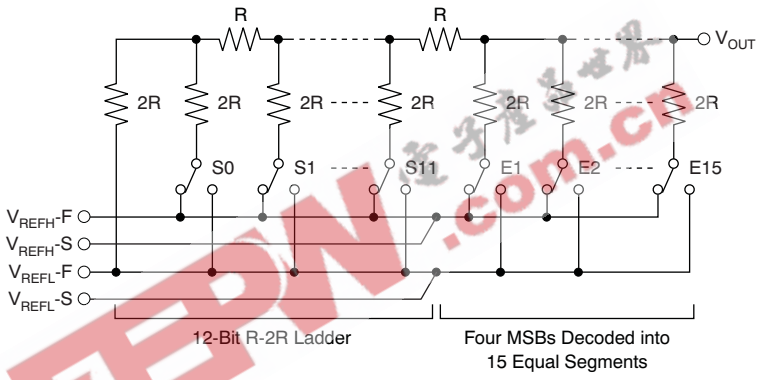


Figure 38. DAC Architecture

OUTPUT RANGE

The output of the DAC is:

$$V_{OUT} = \frac{(V_{REFH} - V_{REFL}) \times Code}{65536 + V_{REFL}} \quad (1)$$

Where *Code* is the decimal data word loaded to the DAC latch.

For example, if V_{REFH} is +10V, and V_{REFL} is –10V, the range of V_{OUT} is from –10V (code = 0000h) to +10V (code = FFFFh).

The range of V_{REFL} is from –18V to (V_{REFH} – 1.25V), and the range of V_{REFH} is 0V to +18V. The output from the DAC8871 can be unipolar (from 0V to +18V) or bipolar by setting the proper V_{REFL} and V_{REFH} values.

THEORY OF OPERATION (continued)

POWER-ON RESET AND HARDWARE RESET

The DAC8871 has a power-on reset function. When the RSTSEL pin is low (tied to DGND), and after power-on or a hardware reset signal is applied to the $\overline{RST}$ pin, the DAC latch is cleared ('0') and the V_{OUT} pin is set to negative full-scale. When RSTSEL is high, the DAC latch and V_{OUT} are set to mid-scale.

SERIAL INTERFACE

The DAC8871 digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™ and TI DSP™ interfaces, which can operate at speeds up to 50 Mbits/second. The data transfer is framed by the chip select ($\overline{CS}$) signal. The DAC works as a bus slave. The bus master generates the synchronize clock (SCLK) and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and SCLK and SDI are ignored. The bus master accesses the DAC by driving $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on the SDI pin are shifted out from the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the content of the input shift register to the input register.

All data registers are 16 bits. It takes 16 SCLK cycles to transfer one data word to the device. To complete a whole data word, $\overline{CS}$ must be taken high immediately after the 16th SCLK is clocked in. If more than 16 SCLK cycles are applied while $\overline{CS}$ is low, the last 16 bits are transferred into the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, the data are corrupted. In this case, reload the DAC latch with a new 16-bit word.

The DAC8871 has an $\overline{LDAC}$ pin that allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. In this case, $\overline{LDAC}$ must be kept high while $\overline{CS}$ is low. If $\overline{LDAC}$ is permanently tied low, the DAC latch will be updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{CS}$).

EXTERNAL AMPLIFIER SELECTION

The output of the DAC8871 is unbuffered. The output impedance is approximately 6.2kΩ. If the applications require an external buffer amplifier, the selected amplifier must have a low-offset voltage (1LSB = 305µV for ±10V output range), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25kΩ) adds to the zero-code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. The output impedance of the DAC is constant and code-independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3dB bandwidth of 1MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3dB amplifier bandwidth results in a shorter effective settling time of the DAC and amplifier combination.

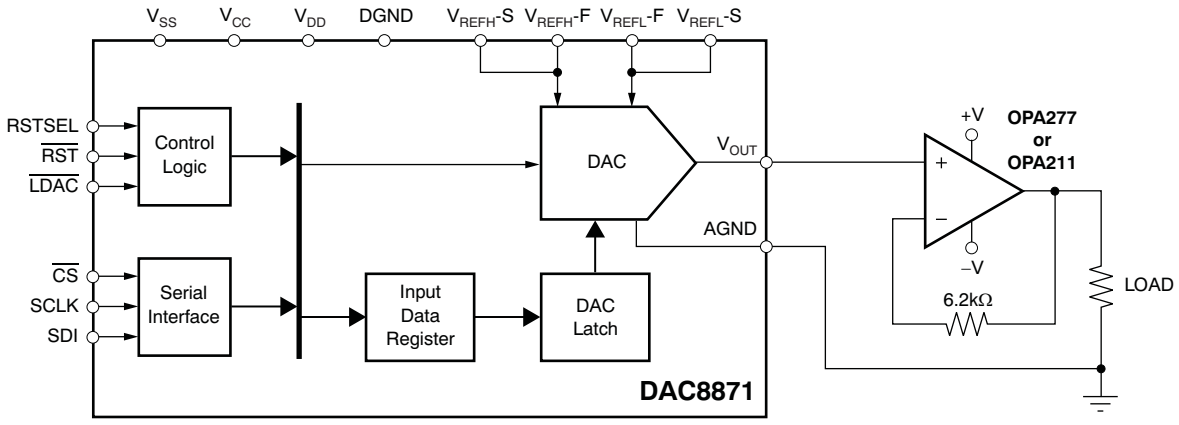


Figure 39. DAC8871 with External Amplifier

APPLICATION INFORMATION

REFERENCE INPUT

The DAC full-scale output voltage is determined by the reference voltage, as shown in the *Output Range* section.

Reference input V_{REFH} can be any voltage from 0V to +18V. Reference input V_{REFL} can be any voltage from –18V to 0V. The current into the V_{REFH} input and out of V_{REFL} depends on the DAC output voltages. Refer to Figure 27 and Figure 28 for details. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC8871 features a reference drive (force) and sense connection that minimizes the internal errors caused by the changing reference current and the circuit impedances. Figure 40 shows a typical reference configuration.

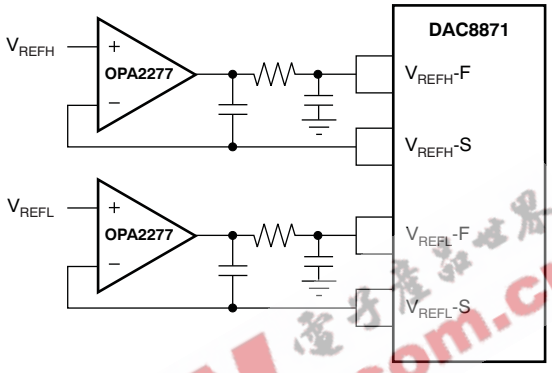


Figure 40. Buffered Reference Connection

POWER SUPPLY BYPASSING

For accurate, high-resolution performance, bypassing the supply pins with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor is recommended.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8871SBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
DAC8871SBPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
DAC8871SBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
DAC8871SBPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
DAC8871SPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
DAC8871SPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
DAC8871SPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
DAC8871SPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR

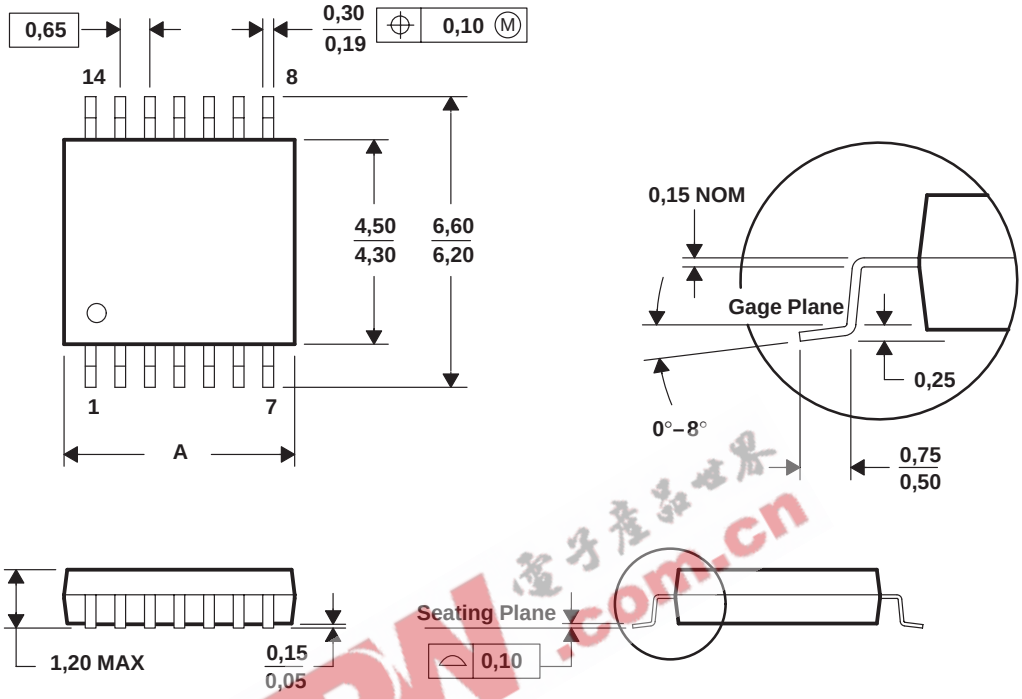
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265