

DDTC (R1 = R2 SERIES) KA

**NPN PRE-BIASED SMALL SIGNAL SC-59
SURFACE MOUNT TRANSISTOR**

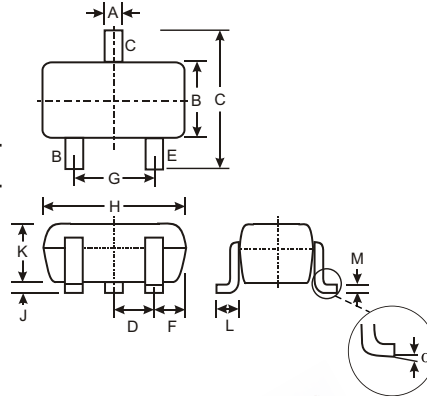
NEW PRODUCT

Features

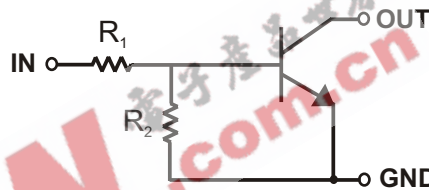
- Epitaxial Planar Die Construction
- Complementary PNP Types Available (DDTA)
- Built-In Biasing Resistors, R1 = R2

Mechanical Data

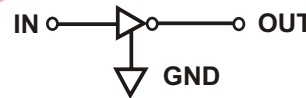
- Case: SC-59, Molded Plastic
- Case material - UL Flammability Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020A
- Terminals: Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Marking: Date Code and Marking Code (See Diagrams & Page 2)
- Weight: 0.008 grams (approx.)
- Ordering Information (See Page 2)



SC-59		
Dim	Min	Max
A	0.35	0.50
B	1.50	1.70
C	2.70	3.00
D	0.95	
G	1.90	
H	2.90	3.10
J	0.013	0.10
K	1.00	1.30
L	0.35	0.55
M	0.10	0.20
α	0°	8°
All Dimensions in mm		



P/N	R1, R2 (NOM)	MARKING
DDTC123EKA	2.2K Ω	N04
DDTC143EKA	4.7K Ω	N08
DDTC114EKA	10K Ω	N13
DDTC124EKA	22K Ω	N17
DDTC144EKA	47K Ω	N20
DDTC115EKA	100K Ω	N24



SCHEMATIC DIAGRAM

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage, (3) to (1)	V _{CC}	50	V
Input Voltage, (2) to (1)	V _{IN}	-10 to +12 -10 to +30 -10 to +40 -10 to +40 -10 to +40 -10 to +40 -10 to +40	V
Output Current	I _O	100 100 50 30 100 20	mA
Output Current	I _C (Max)	100	mA
Power Dissipation	P _d	200	mW
Thermal Resistance, Junction to Ambient Air (Note 1)	R _{θJA}	625	°C/W
Operating and Storage and Temperature Range	T _j , T _{STG}	-55 to +150	°C

Note: 1. Mounted on FR4 PC Board with recommended pad layout at <http://www.diodes.com/datasheets/ap02001.pdf>.

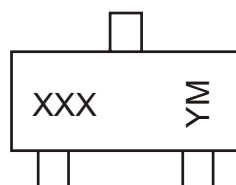
Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
Input Voltage		$V_{I(off)}$	0.5	1.1	—	V	$V_{CC} = 5V, I_O = 100\mu\text{A}$
		$V_{I(on)}$	—	1.9	3		$V_O = 0.3V, I_O = 20\text{mA}, \text{DDTC123EKA}$ $V_O = 0.3V, I_O = 20\text{mA}, \text{DDTC143EKA}$ $V_O = 0.3V, I_O = 10\text{mA}, \text{DDTC114EKA}$ $V_O = 0.3V, I_O = 5\text{mA}, \text{DDTC124EKA}$ $V_O = 0.3V, I_O = 2\text{mA}, \text{DDTC144EKA}$ $V_O = 0.3V, I_O = 1\text{mA}, \text{DDTC115EKA}$
Output Voltage		$V_{O(on)}$	—	0.1	0.3	V	$I_O/I_I = 10\text{mA}/0.5\text{mA}, \text{DDTC123EKA}$ $I_O/I_I = 10\text{mA}/0.5\text{mA}, \text{DDTC143EKA}$ $I_O/I_I = 10\text{mA}/0.5\text{mA}, \text{DDTC114EKA}$ $I_O/I_I = 10\text{mA}/0.5\text{mA}, \text{DDTC124EKA}$ $I_O/I_I = 10\text{mA}/0.5\text{mA}, \text{DDTC144EKA}$ $I_O/I_I = 5\text{mA}/0.25\text{mA}, \text{DDTC115EKA}$
Input Current	DDTC123EKA DDTC143EKA DDTC114EKA DDTC124EKA DDTC144EKA DDTC115EKA	I_I	—	—	3.8 1.8 0.88 0.36 0.18 0.15	mA	$V_I = 5V$
Output Current		$I_{O(off)}$	—	—	0.5	μA	$V_{CC} = 50V, V_I = 0V$
DC Current Gain	DDTC123EKA DDTC143EKA DDTC114EKA DDTC124EKA DDTC144EKA DDTC115EKA	G_I	20 20 30 56 68 82	—	—	—	$V_O = 5V, I_O = 20\text{mA}$ $V_O = 5V, I_O = 10\text{mA}$ $V_O = 5V, I_O = 5\text{mA}$ $V_O = 5V, I_O = 5\text{mA}$ $V_O = 5V, I_O = 5\text{mA}$ $V_O = 5V, I_O = 5\text{mA}$
Input Resistor (R_1) Tolerance		DR_1	-30	—	+30	%	—
Resistance Ratio		R_2/R_1	0.8	1	1.2	—	—
Gain-Bandwidth Product*		f_T	—	250	—	MHz	$V_{CE} = 10V, I_E = 5\text{mA},$ $f = 100\text{MHz}$

* Transistor - For Reference Only

Ordering Information (Note 2)

Device	Packaging	Shipping
DDTC123EKA-7	SC-59	3000/Tape & Reel
DDTC143EKA-7	SC-59	3000/Tape & Reel
DDTC114EKA-7	SC-59	3000/Tape & Reel
DDTC124EKA-7	SC-59	3000/Tape & Reel
DDTC144EKA-7	SC-59	3000/Tape & Reel
DDTC115EKA-7	SC-59	3000/Tape & Reel

Notes: 2. For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.**Marking Information**

XXX = Product Type Marking Code
See Sheet 1 Diagrams
YM = Date Code Marking
Y = Year ex: N = 2002
M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

TYPICAL CURVES - DDTC143EKA

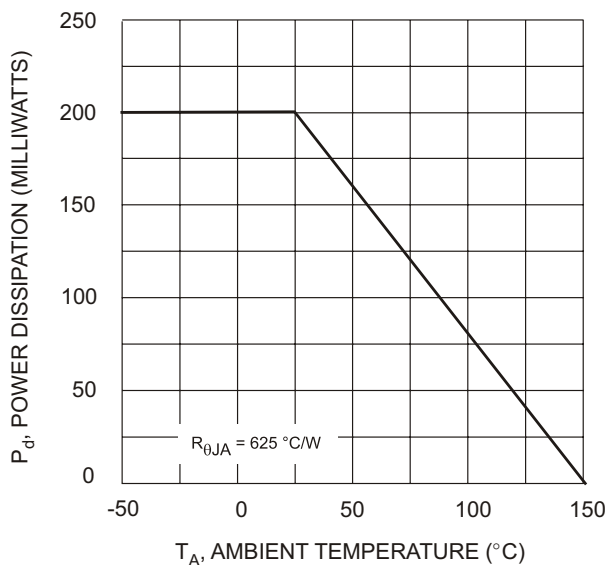


Fig. 1 Derating Curve

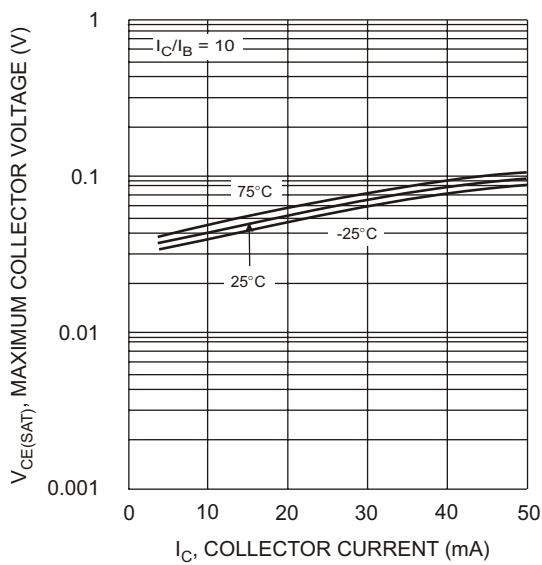


Fig. 2 $V_{CE(SAT)}$ vs. I_C

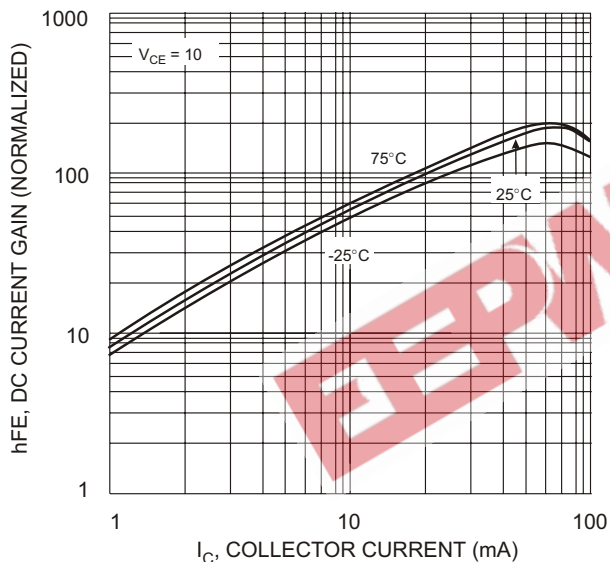


Fig. 3 DC CURRENT GAIN

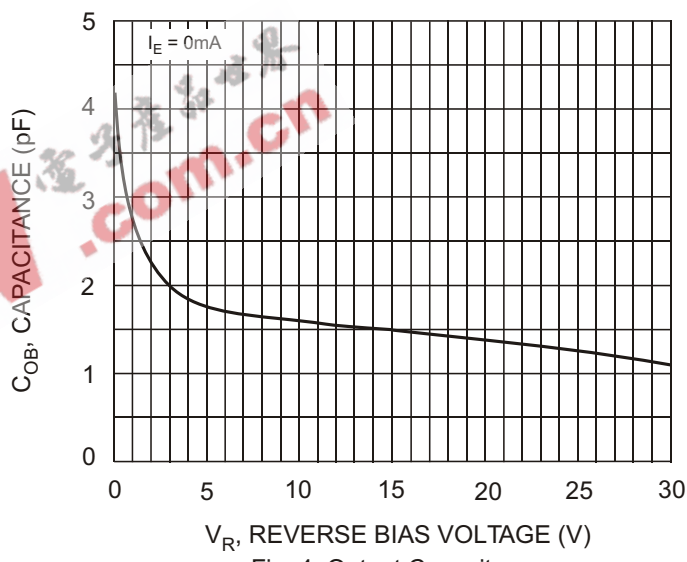


Fig. 4 Output Capacitance

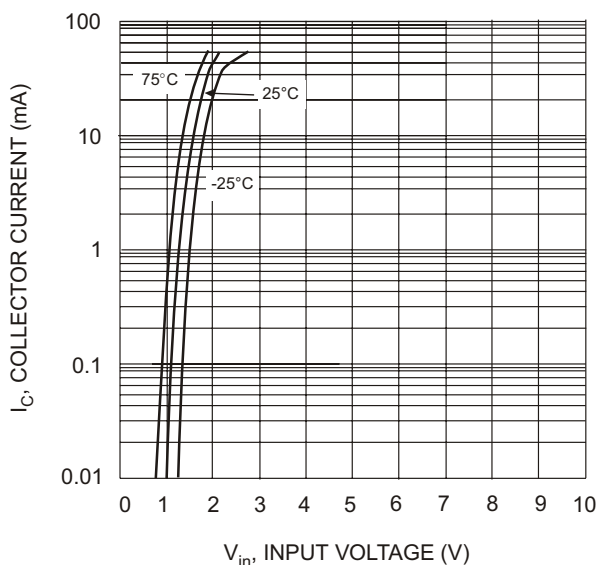


Fig. 5 Collector Current Vs. Input Voltage

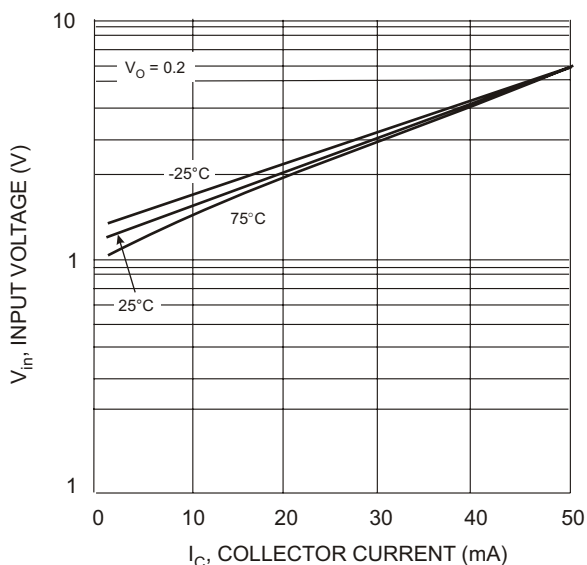


Fig. 6 Input Voltage vs. Collector Current