18-Bit, Single-Channel, Low-Noise, Voltage-Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy: ±2 LSB**
- **18-Bit Monotonic Over Temperature Range**
- **Low-Noise: 24nV/√Hz**
- **Fast Settling: 5μs**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Single Power Supply: +4.75V to +5.5V**
- **DAC Loading Control**
- **Selectable Power-On Reset to Zero-Scale or Midscale**
- **Power-Down Mode**
- **Unipolar Straight Binary or 2s Complement Input Mode**
- **Fast SPI™ Interface with Schmitt-Triggered Inputs: Up To 50MHz, 1.8V/3V/5V Logic**
- **Small Package: QFN-24, 4mm × 4mm**

APPLICATIONS

- **Industrial Process Control**
- **Data Acquisition Systems**
- **Automatic Test Equipment**
- **Communications**
- **Optical Networking**

DESCRIPTION

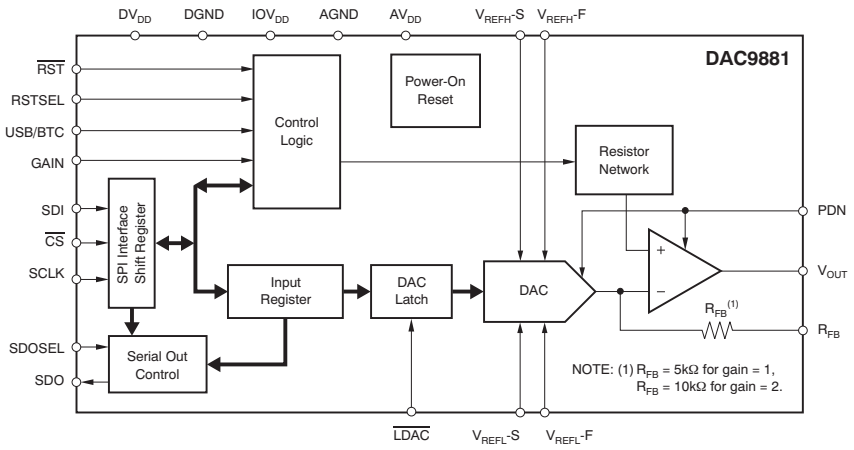
The DAC9881 is an 18-bit, single-channel, voltage-output digital-to-analog converter (DAC) that offers low-power operation and a flexible SPI serial interface. It also features 18-bit monotonicity, excellent linearity, and fast settling time. The on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the full supply range of 4.75V to 5.5V.

The device supports a standard SPI serial interface capable of operating with input data clock frequencies up to 50MHz. The DAC9881 requires an external reference voltage to set the output range of the DAC channel. A programmable power-on reset circuit is also incorporated into the device to ensure that the DAC output powers up at zero-scale or midscale, and remains there until a valid write command.

Additionally, the device has the capability to function in either unipolar straight binary or 2s complement mode. The DAC9881 provides a power-down feature, accessed over the PDN pin, that reduces the current consumption to 25μA at 5V. Power consumption is 6mW at 5V, reducing to 125μW in power-down mode.

The DAC9881 is available in a 4mm × 4mm QFN-24 package with a specified operating temperature range of –40°C to +85°C.

PRODUCT PREVIEW



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC9881	QFN-24	RGE	–40°C to +85°C	DAC9881

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		DAC9881	UNIT
AV_{DD} to AGND		–0.3 to 6	V
DV_{DD} to DGND		–0.3 to 6	V
IOV_{DD} to DGND		–0.3 to 6	V
Digital input voltage to DGND		–0.3 to IOV_{DD} + 0.3	V
V_{OUT} to AGND		–0.3 to AV_{DD} + 0.3	V
Operating temperature range		–40 to +85	°C
Storage temperature range		–65 to +150	°C
Maximum junction temperature (T_J max)		+150	°C
ESD ratings	Human body model (HBM)	3000	V
	Charged device model (CDM)	1000	V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD} = +4.75V$ to $+5.5V$, $IOV_{DD} = +1.8V$ to $+5.5V$, and gain = 1X mode, unless otherwise noted.

PARAMETER	CONDITIONS		DAC9881 MIN	DAC9881 TYP	DAC9881 MAX	UNIT
ACCURACY						
Linearity error	Measured by line passing through codes 2048 and 260096			±1	±2	LSB
Differential linearity error	Measured by line passing through codes 2048 and 260096			±0.5	±1	LSB
Monotonicity			18			Bits
Zero-scale error	T_A = +25°C, code = 2048				±16	LSB
	T_{MIN} to T_{MAX}, code = 2048				±32	LSB
Zero-scale drift	Code = 2048			±0.5	±1	ppm/°C of FSR
Gain error	T_A = +25°C, measured by line passing through codes 2048 and 260096			±16	±32	LSB
Gain temperature drift	Measured by line passing through codes 2048 and 260096			±0.5	±1	ppm/°C
PSRR	V_{OUT} = full-scale, AV_{DD} = +5V ±10%				32	LSB/V
ANALOG OUTPUT(1)						
Voltage output(2)			0		AV_{DD}	V
Output voltage drift vs time	Device operating for 500 hours			5		ppm of FSR
	Device operating for 1000 hours			8		ppm of FSR
Output current				2.5		mA
Maximum load capacitance				200		pF
Short-circuit current				+31, –50		mA
REFERENCE INPUT(1)						
V_{REFH} input voltage range	AV_{DD} = +5.5V		1.25	5.0	AV_{DD}	V
V_{REFH} input capacitance				5		pF
V_{REFH} input impedance				4.5		kΩ
V_{REFL} input voltage range			–0.2	0	+0.2	V
V_{REFL} input capacitance				4.5		pF
V_{REFL} input impedance				5		kΩ
DYNAMIC PERFORMANCE(1)						
Settling time	To ±0.003% FS, R_L = 10kΩ, C_L = 50pF, code 04000h to 3C000h			5		µs
Slew rate	From 10% to 90% of 0V to +5V			2.5		V/µs
Code change glitch	Code = 1FFFFh to 20000h to 1FFFFh	V_{REFH} = 5V, gain = 1X mode		37		nV-s
		V_{REFH} = 2.5V, gain = 1X mode		18		nV-s
		V_{REFH} = 1.25V, gain = 1X mode		9		nV-s
		V_{REFH} = 2.5V, gain = 2X mode		21		nV-s
		V_{REFH} = 1.25V, gain = 2X mode		10		nV-s
Digital feedthrough				1		nV-s
Output noise voltage density	f = 1kHz to 100kHz, full-scale output	Gain = 1		24	30	nV/√Hz
		Gain = 2		40	48	nV/√Hz
Output noise voltage	f = 0.1Hz to 10Hz, full-scale output			2		μV_{PP}

(1) Ensured by design. Not production tested.
(2) The output from the V_{OUT} pin = $[(V_{REFH} - V_{REFL})/262144] \times CODE \times$ Buffer GAIN + V_{REFL}. The maximum range of V_{OUT} is 0V to AV_{DD}. The full-scale of the output must be less than AV_{DD}; otherwise, output saturation occurs.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD}$ = +4.75V to +5.5V, IOV_{DD} = +1.8V to +5.5V, and gain = 1X mode, unless otherwise noted.

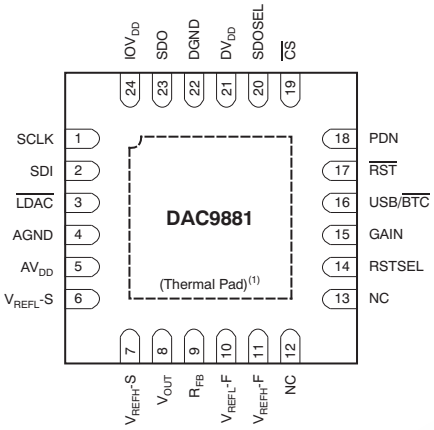
PARAMETER	CONDITIONS	DAC9881			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS(3)					
High-level input voltage, V_{IH}	IOV_{DD} = 4.5V to 5.5V	3.8		IOV_{DD} + 0.3	V
	IOV_{DD} = 2.7V to 3.3V	2.1		IOV_{DD} + 0.3	V
	IOV_{DD} = 1.7V to 2.0V	1.5		IOV_{DD} + 0.3	V
Low-level input voltage, V_{IL}	IOV_{DD} = 4.5V to 5.5V	–0.3		0.8	V
	IOV_{DD} = 2.7V to 3.3V	–0.3		0.6	V
	IOV_{DD} = 1.7V to 2.0V	–0.3		0.3	V
Digital input current (I_{IN})			±1	±10	µA
Digital input capacitance			5		pF
DIGITAL OUTPUT(3)					
High-level output voltage, V_{OH}	IOV_{DD} = 2.7V to 5.5V, I_{OH} = –1mA	IOV_{DD} – 0.2			V
	IOV_{DD} = 1.7V to 2.0V, I_{OH} = –500µA	IOV_{DD} – 0.2			V
Low-level output voltage, V_{OL}	IOV_{DD} = 2.7V to 5.5V, I_{OL} = 1mA			0.2	V
	IOV_{DD} = 1.7 to 2.0V, I_{OL} = 500µA			0.2	V
POWER SUPPLY					
AV_{DD}		+4.75		+5.5	V
DV_{DD}		+4.75		+5.5	V
IOV_{DD}		+1.7		DV_{DD}	V
AI_{DD}	V_{IH} = IOV_{DD}, V_{IL} = DGND			1.5	mA
DI_{DD}	V_{IH} = IOV_{DD}, V_{IL} = DGND		1	10	µA
IOI_{DD}	V_{IH} = IOV_{DD}, V_{IL} = DGND		1	10	µA
AI_{DD} power-down	PDN = IOV_{DD}		25	50	µA
Power dissipation	AV_{DD} = DV_{DD} = 5.0V		6	7.5	mW
TEMPERATURE RANGE					
Specified performance		–40		+85	°C

(3) Ensured by design. Not production tested.

PRODUCT PREVIEW

PIN CONFIGURATION

RGE PACKAGE[1]
QFN-24
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

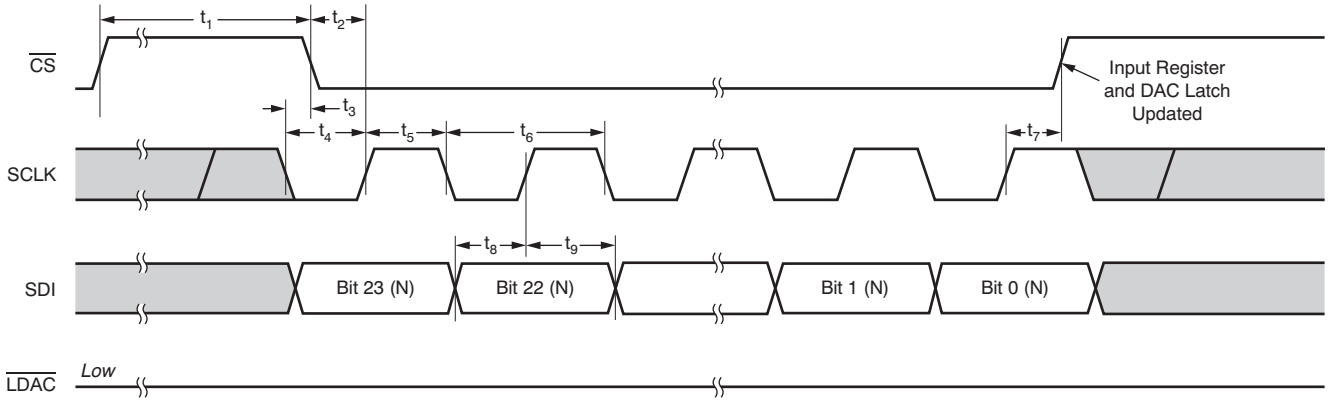
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1	SCLK	I	SPI bus serial clock input
2	SDI	I	SPI bus serial data input
3	$\overline{\text{LDAC}}$	I	Load DAC latch control input (active low). When $\overline{\text{LDAC}}$ is low, the DAC latch is transparent, and the contents of the input register are transferred to the DAC latch. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated.
4	AGND	I	Analog ground
5	AV_{DD}	I	Analog power supply
6	V_{REFL}-S	I	Reference low input sense
7	V_{REFH}-S	I	Reference high input sense
8	V_{OUT}	O	Output of output buffer
9	R_{FB}	I	Feedback resistor connected to the inverting input of the output buffer.
10	V_{REFL}-F	I	Reference low input force
11	V_{REFH}-F	I	Reference high input force
12	NC	—	Do not connect.
13	NC	—	Do not connect.
14	RSTSEL	I	Selects the value of the output from the V_{OUT} pin after power-on or hardware reset. If RSTSEL = IOV_{DD}, then register data = 20000h. If RSTSEL = DGND, then register data = 00000h.
15	GAIN	I	Buffer gain setting. Gain = 1 when the pin is connected to DGND; Gain = 2 when the pin is connected to IOV_{DD}.
16	USB/$\overline{\text{BTC}}$	I	Input data format selection. Input data are straight binary format when the pin is connected to IOV_{DD}, and in twos complement format when the pin is connected to DGND.
17	$\overline{\text{RST}}$	I	Reset input (active low). Logic low on this pin causes the device to perform a reset.
18	PDN	I	Power-down input (active high). Logic high on this pin forces the device into power-down status. In power-down, the V_{OUT} pin connects to AGND through a 10kΩ resistor.
19	$\overline{\text{CS}}$	I	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, SDO is in a high-impedance state.
20	SDOSEL	I	SPI serial data output selection. When SDOSEL is tied to IOV_{DD}, the contents of the existing input register are shifted out from the SDO pin; this is Stand-Alone mode. When SDOSEL is tied to DGND, the contents in the SPI input shift register are shifted out from the SDO pin; this is Daisy-Chain mode for daisy-chained communication.
21	DV_{DD}	I	Digital power supply (connect to AV_{DD}, pin 5)
22	DGND	I	Digital ground
23	SDO	O	SPI bus serial data output. Refer to the *Timing Diagrams* for further detail.
24	IOV_{DD}	I	Interface power. Connect to +1.8V for 1.8V logic, +3V for 3V logic, and to +5V for 5V logic.

PRODUCT PREVIEW

TIMING DIAGRAMS

Case 1: Standalone operation without SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation without SDO, $\overline{\text{LDAC}}$ active.

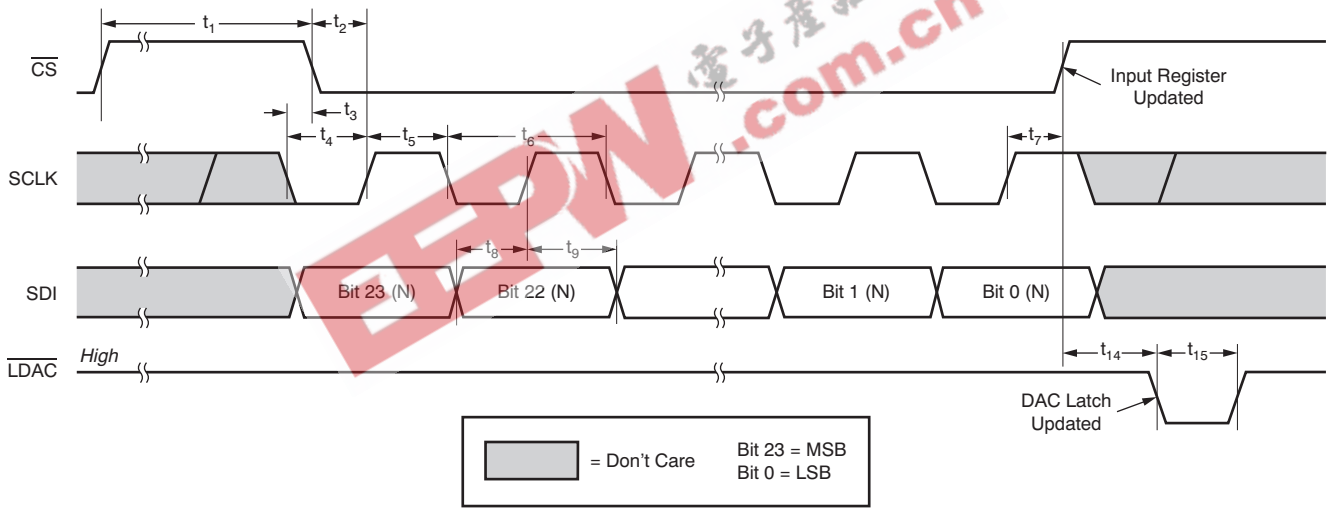


Figure 1. Timing Diagram for Standalone Operation without SDO

PRODUCT PREVIEW

TIMING CHARACTERISTICS for Figure 1(1)(2)(3)

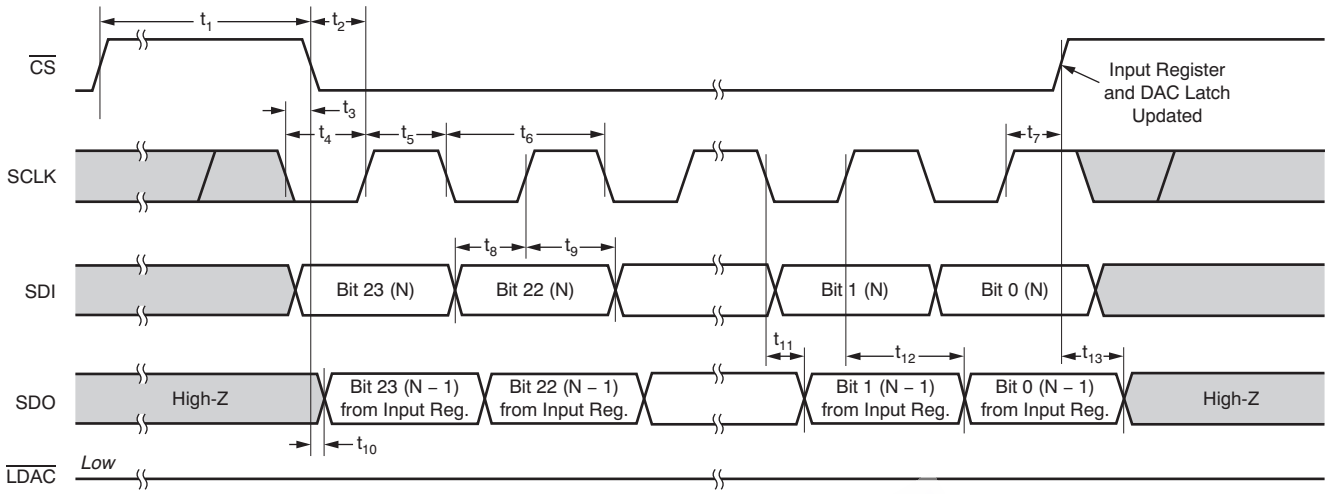
At –40°C to +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		40	MHz
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		50	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	30		ns
t_2	$\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
t_3	SCLK falling edge to $\overline{CS}$ falling edge setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_4	SCLK low time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_5	SCLK high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_6	SCLK cycle time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_7	SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{14}	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse width	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F = 2ns$ (10% to 90% of IOV_{DD}) and timed from a voltage level of $IOV_{DD}/2$.
(2) Ensured by design. Not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

PRODUCT PREVIEW

Case 1: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ active.

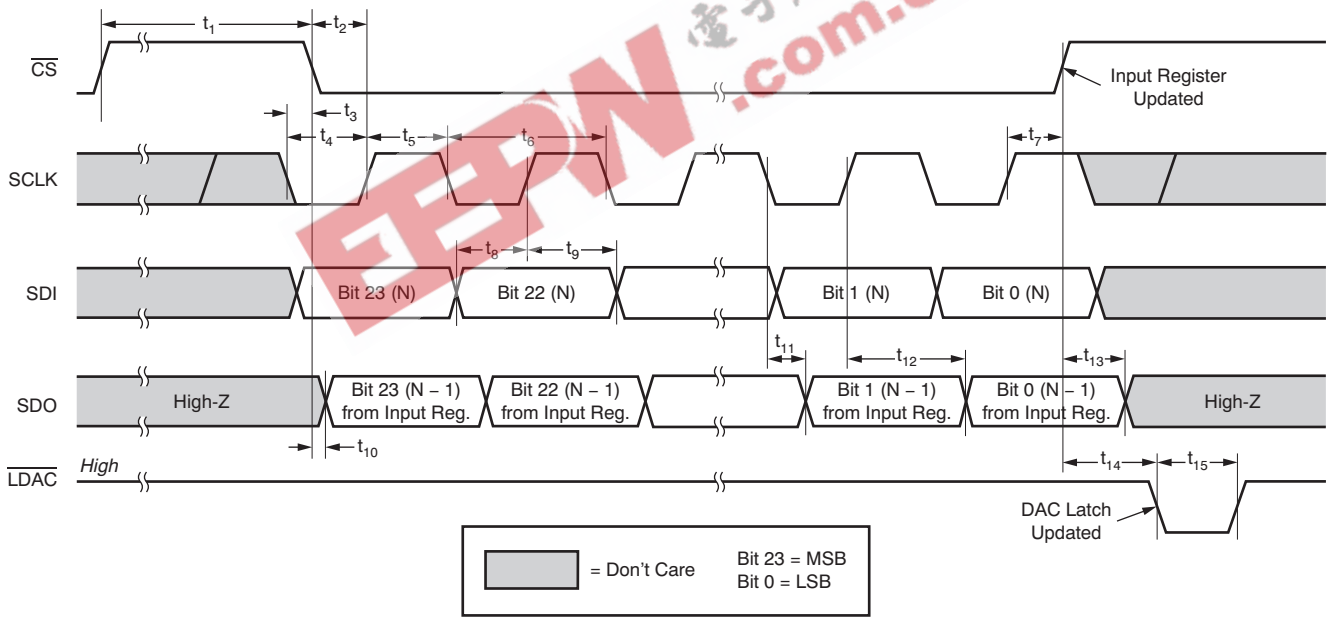
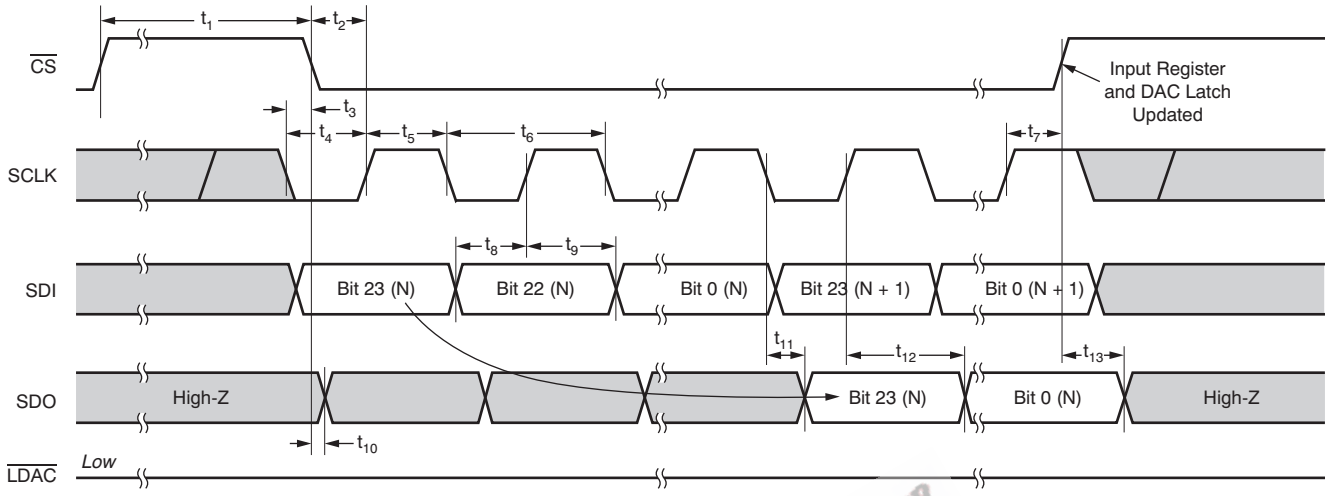


Figure 2. Timing Diagram for Standalone Operation with SDO

PRODUCT PREVIEW

Case 1: Daisy Chain, $\overline{\text{LDAC}}$ tied low.



Case 2: Daisy Chain, $\overline{\text{LDAC}}$ active.

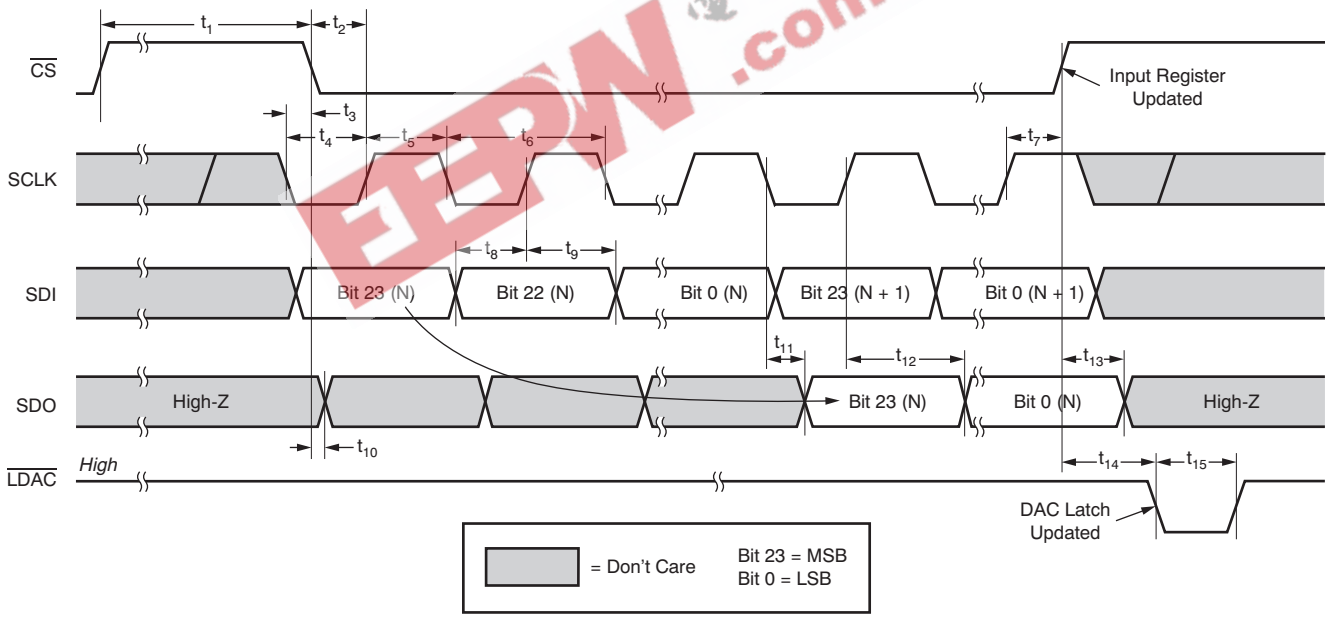


Figure 3. Timing Diagram for Daisy Chain Mode, Two Cascaded Devices

PRODUCT PREVIEW

TIMING CHARACTERISTICS for Figure 2 and Figure 3(1)(2)(3)

At –40°C to +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		20	MHz
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		25	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	30		ns
t_2	$\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
t_3	SCLK falling edge to $\overline{CS}$ falling edge setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_4	SCLK low time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_5	SCLK high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_6	SCLK cycle time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	40		ns
t_7	SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{10}	SDO active from $\overline{CS}$ falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		15	ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		10	ns
t_{11}	SDO data valid from SCLK falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		20	ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		15	ns
t_{12}	SDO data hold from SCLK rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_{13}	SDO High-Z from $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		8	ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		5	ns
t_{14}	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse width	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F$ = 2ns (10% to 90% of IOV_{DD}) and timed from a voltage level of $IOV_{DD}/2$.
(2) Ensured by design. Not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

PRODUCT PREVIEW

PACKAGING INFORMATION

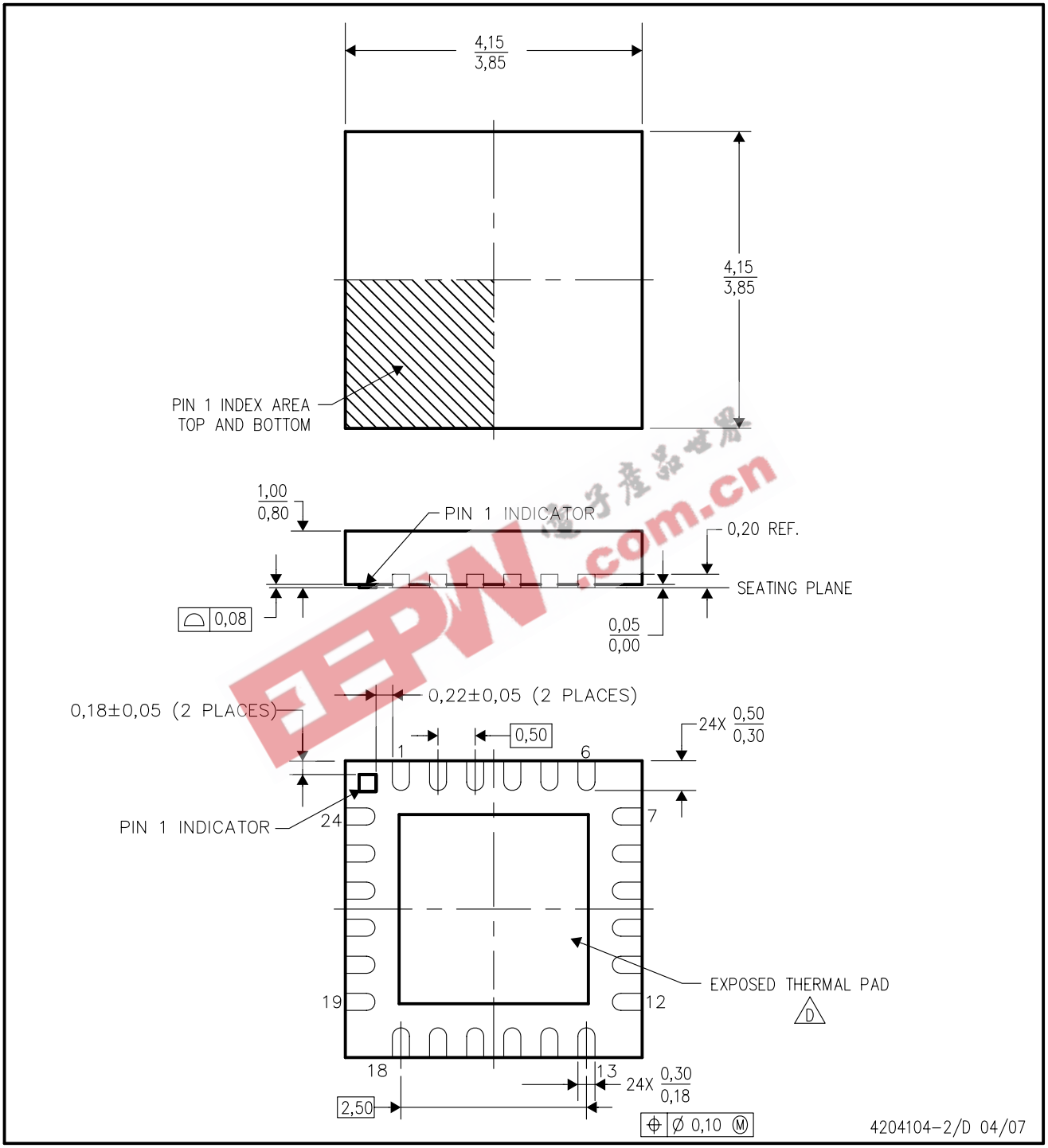
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC9881IRGER	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI
DAC9881IRGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGE (S–PQFP–N24) PIN 1 BUMP OPTION PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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