# DBB03
# Baseband ASIC for Dolphin Chipset

SWRS027B – DECEMBER 2004 – REVISED MARCH 2005

## FEATURES

- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 160 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.9 µA**
  - **Off Mode (RAM Retention) : 0.1 µA**
- **Contains Frequency-Hopping Firmware for Dolphin Reference Design**
- **Firmware Resides in ROM-Based Program Memory and is Fixed**
- **Simple UART Interface to an External Host/System Microcontroller**
- **Pre-Defined Protocol for Communication with an External Host/System Microcontroller**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in less than 6 µs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **Serial Communication Interface (USART), Software Selects Asynchronous UART or Synchronous SPI**
- **Available in 64-Pin Quad Flat Pack (QFP)**
- **For Complete Dolphin Product Description, See the *Dolphin Frequency Hopping Spread Spectrum Evaluation Kit Hardware and Software User's Guide* (SLLU090)**

## DESCRIPTION

The DBB03 is a baseband ASIC for the "Dolphin" reference design. The firmware for the Dolphin reference design resides in the ROM-based program memory of the DBB03, and thus can be readily interfaced with a TRF6903 single-chip RF Transceiver to generate a frequency hopping wireless UART "Dolphin" reference design chipset. This is illustrated in Figure 1.

The DBB03 baseband ASIC in addition to being a RF baseband processor is also responsible for communications with an external host/system micrcontroller. In a typical end user application, the Dolphin chipset will be connected up to an external host/system microcontroller that will send configuration messages, RF transmission messages into the Dolphin chipset, or receive status, RF messages received from the Dolphin chipset.

Any catalog low-cost host/system microcontroller can be interfaced to the Dolphin chipset as long as the Dolphin host interface protocol for communication is adhered to. (See Application Note Dolphin - Frequency Hopping Spread Spectrum Chipset Host Interface Protocol TI Literature SWRA043) Texas Instruments recommends its ultra-low power MSP430 series of microcontrollers to interface with Dolphin.

The interface between the DBB03 baseband ASIC and an external host/system microcontroller is a simple UART consisting of RX and TX data lines. (See Application Note *Interfacing Dolphin to an External System Microcontroller*, TI Literature SWRA045).

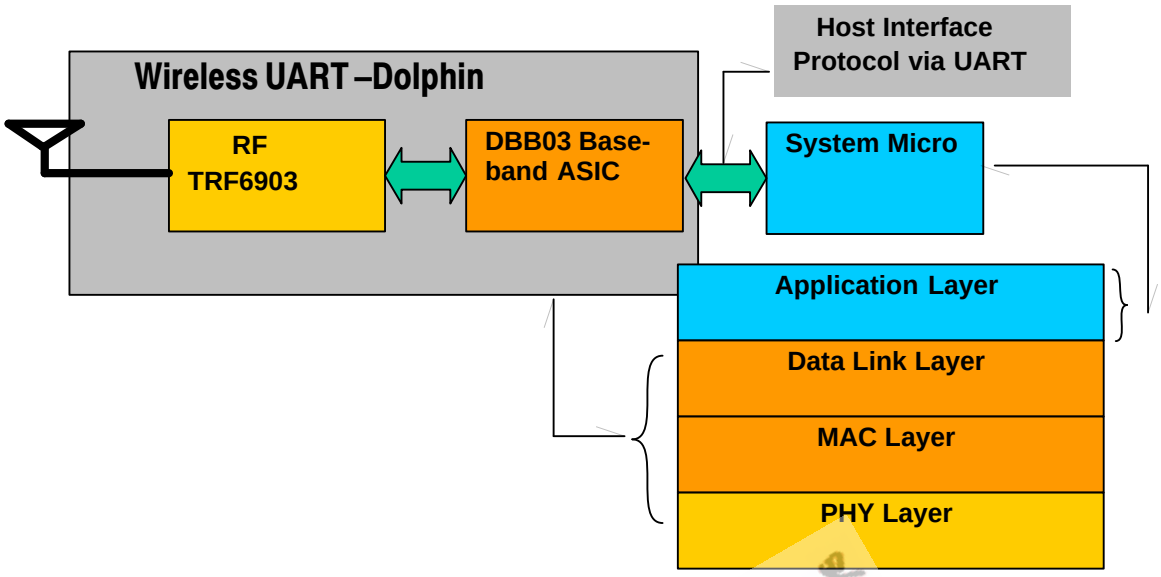



**Figure 1. DBB03 - Baseband ASIC for the Dolphin Chipset**

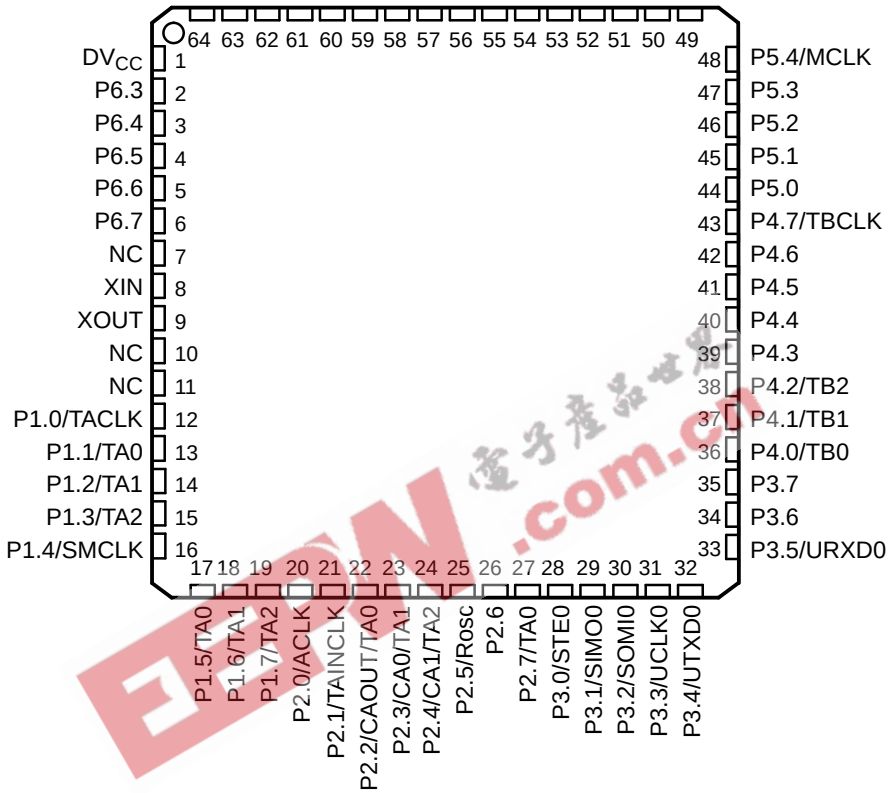
The Wireless UART Dolphin chipset is a true Data-In/RF-out and RF-in/Data-out solution with all aspects of data management and frequency hopping implemented in firmware residing on the DBB03. As illustrated in Figure 1, the DBB03 baseband ASIC contains the complete firmware for Dolphin (PHYsical, MAC and the Data Link layer), while the application layer protocol is handled by the external Host/System Microcontroller.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE | ORDER NUMBER |
|---|---|---|
| -40°C to 85°C | Plastic 64-pin QFP (PM) | DBB03 IPM |

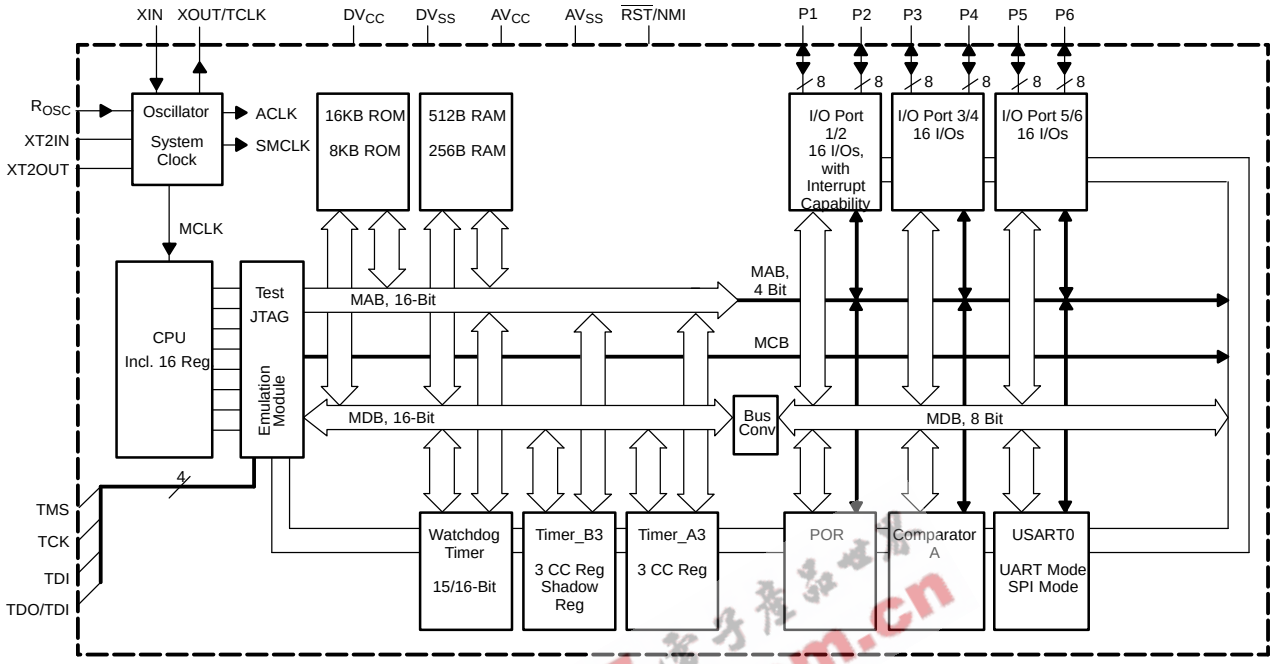
## PIN DESIGNATION, DBB03 Baseband ASIC

**PM PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## FUNCTIONAL BLOCK DIAGRAMS: DBB03




## DEVICE INFORMATION

### TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $AV_{CC}$ | 64 | | Supply voltage, positive terminal. $AV_{CC}$ and $DV_{CC}$ are internally connected together. |
| $AV_{SS}$ | 64 | | Supply voltage, negative terminal. $AV_{SS}$ and $DV_{SS}$ are internally connected together. |
| $DV_{CC}$ | 1 | | Supply voltage, positive terminal. $AV_{CC}$ and $DV_{CC}$ are internally connected together. |
| $DV_{SS}$ | 63 | | Supply voltage, negative terminal. $AV_{SS}$ and $DV_{SS}$ are internally connected together. |
| P1.0/TACLK | 12 | I/O | General-purpose digital I/O pin/Timer_A, clock signal TACLK input |
| P1.1/TA0 | 13 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output |
| P1.2/TA1 | 14 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output |
| P1.3/TA2 | 15 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output |
| P1.4/SMCLK | 16 | I/O | General-purpose digital I/O pin/SMCLK signal output |
| P1.5/TA0 | 17 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output |
| P1.6/TA1 | 18 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output |
| P1.7/TA2 | 19 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output |
| P2.0/ACLK | 20 | I/O | General-purpose digital I/O pin/ACLK output |
| P2.1/TAINCLK | 21 | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK |
| P2.2/CAOUT/TA0 | 22 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output |
| P2.3/CA0/TA1 | 23 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input |
| P2.4/CA1/TA2 | 24 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input |
| P2.5/$R_{OSC}$ | 25 | I/O | General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency |
| P2.6 | 26 | I/O | General-purpose digital I/O pin |

## DEVICE INFORMATION (continued)

### TERMINAL FUNCTIONS (continued)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P2.7/TA0 | 27 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output |
| P3.0/STE0 | 28 | I/O | General-purpose digital I/O pin/slave transmit enable - USART0/SPI mode |
| P3.1/SIMO0 | 29 | I/O | General-purpose digital I/O pin/slave in/master out of USART0/SPI mode |
| P3.2/SOMI0 | 30 | I/O | General-purpose digital I/O pin/slave out/master in of USART0/SPI mode |
| P3.3/UCLK0 | 31 | I/O | General-purpose digital I/O pin/external clock input - USART0/UART or SPI mode, clock output - USART0/SPI mode |
| P3.4/UTXD0 | 32 | I/O | General-purpose digital I/O pin/transmit data out - USART0/UART mode |
| P3.5/URXD0 | 33 | I/O | General-purpose digital I/O pin/receive data in - USART0/UART mode |
| P3.6 | 34 | I/O | General-purpose digital I/O pin |
| P3.7 | 35 | I/O | General-purpose digital I/O pin |
| P4.0/TB0 | 36 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI0A/B input, compare: Out0 output |
| P4.1/TB1 | 37 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output |
| P4.2/TB2 | 38 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output |
| P4.3 | 39 | I/O | General-purpose digital I/O pin |
| P4.4 | 40 | I/O | General-purpose digital I/O pin |
| P4.5 | 41 | I/O | General-purpose digital I/O pin |
| P4.6 | 42 | I/O | General-purpose digital I/O pin |
| P4.7/TBCLK | 43 | I/O | General-purpose digital I/O pin/Timer_B, clock signal TBCLK input |
| P5.0 | 44 | I/O | General-purpose digital I/O pin |
| P5.1 | 45 | I/O | General-purpose digital I/O pin |
| P5.2 | 46 | I/O | General-purpose digital I/O pin |
| P5.3 | 47 | I/O | General-purpose digital I/O pin |
| P5.4/MCLK | 48 | I/O | General-purpose digital I/O pin/main system clock MCLK output |
| P5.5/SMCLK | 49 | I/O | General-purpose digital I/O pin/submain system clock SMCLK output |
| P5.6/ACLK | 50 | I/O | General-purpose digital I/O pin/auxiliary clock ACLK output |
| P5.7/TBOUTH | 51 | I/O | General-purpose digital I/O pin/switch all PWM digital output ports to high impedance - Timer_B7 TB0 to TB2 |
| P6.0 | 59 | I/O | General-purpose digital I/O pin |
| P6.1 | 60 | I/O | General-purpose digital I/O pin |
| P6.2 | 61 | I/O | General-purpose digital I/O pin |
| P6.3 | 2 | I/O | General-purpose digital I/O pin |
| P6.4 | 3 | I/O | General-purpose digital I/O pin |
| P6.5 | 4 | I/O | General-purpose digital I/O pin |
| P6.6 | 5 | I/O | General-purpose digital I/O pin |
| P6.7 | 6 | I/O | General-purpose digital I/O pin |
| $\overline{\text{RST}}$/NMI | 58 | I | Reset input, nonmaskable interrupt input port |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming test. |
| TDI/TCLK | 55 | I | Test data input or test clock input. TDI is used as a data input port. The device protection fuse is connected to TDI. |
| TDO/TDI | 54 | I/O | Test data output port. TDO/TDI data output |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device test. |
| NC | 7, 10, 11 | | No internal connection |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1 |
| XT2IN | 53 | I | Input port for crystal oscillator XT2. Only standard crystals can be connected. |
| XT2OUT | 52 | O | Output terminal of crystal oscillator XT2 |

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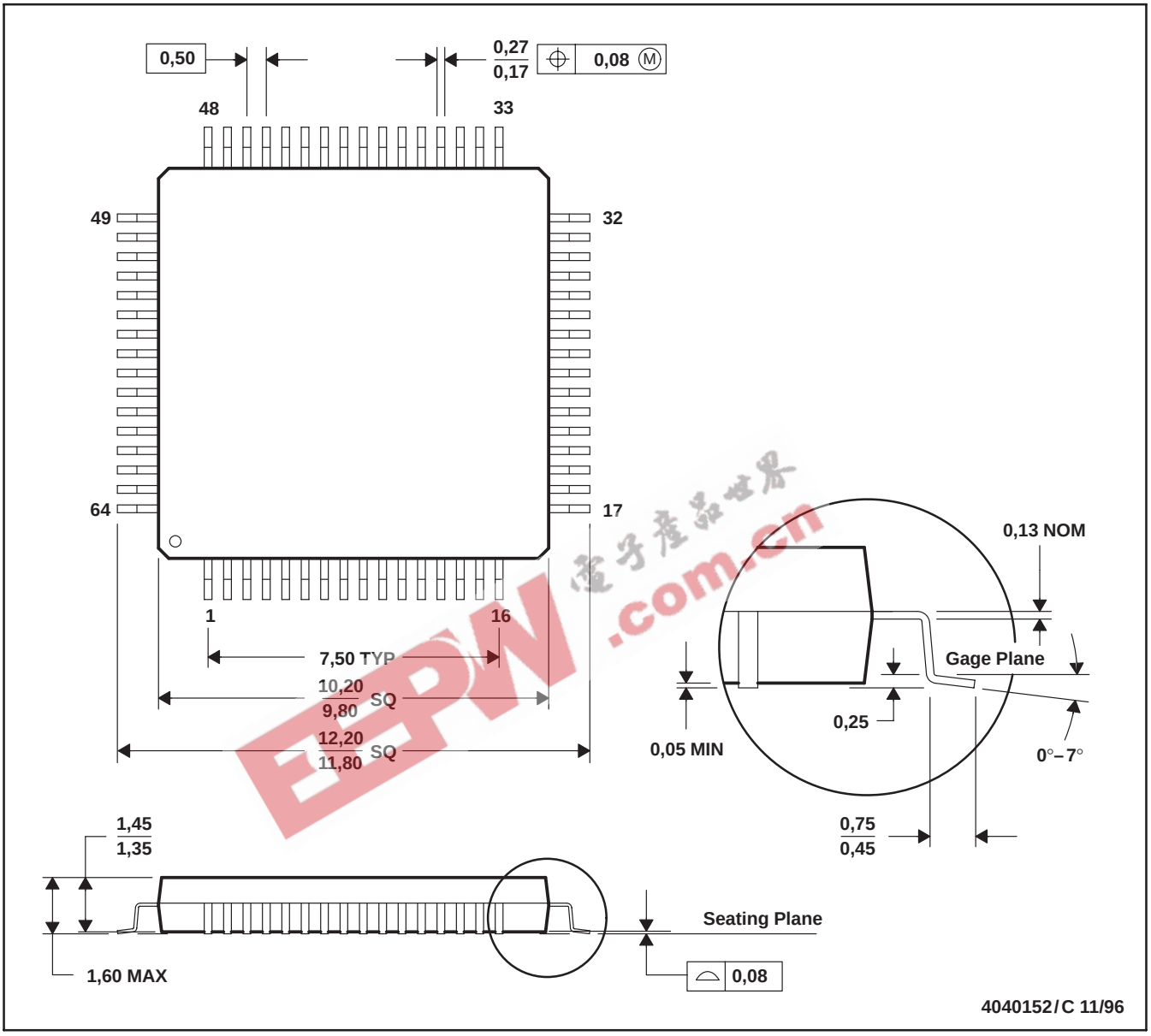
**PM (S-PQFP-G64)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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