

Quad D Flip-Flop with Common Clock and Reset

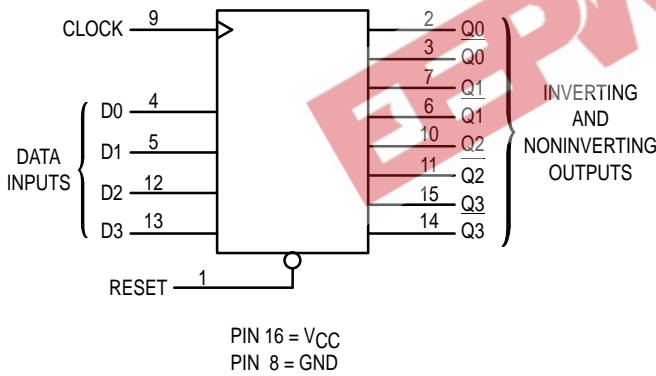
High-Performance Silicon-Gate CMOS

The MC54/74HC175 is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

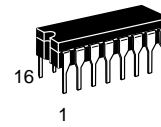
This device consists of four D flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active-low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive going edge of the Clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity 166 FETs or 41.5 Equivalent Gates

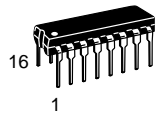
LOGIC DIAGRAM



MC54/74HC175



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

PIN ASSIGNMENT

RESET	1	16	V _{CC}
Q0	2	15	Q3
Q0	3	14	Q3
D0	4	13	D3
D1	5	12	D2
Q1	6	11	Q2
Q1	7	10	Q2
GND	8	9	CLOCK

FUNCTION TABLE

Inputs			Outputs	
Reset	Clock	D	Q	Q
L	X	X	L	H
H	↗	H	H	L
H	↘	L	L	H
H	L	X	No Change	



MC54/74HC175

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125° C
Ceramic DIP: - 10 mW/°C from 100° to 125° C
SOIC Package: - 7 mW/°C from 65° to 125° C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit				
				- 55 to 25° C	≤ 85° C	≤ 125° C					
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V				
			4.5	3.15	3.15	3.15					
			6.0	4.2	4.2	4.2					
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V				
			4.5	0.9	0.9	0.9					
			6.0	1.2	1.2	1.2					
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V				
			4.5	4.4	4.4	4.4					
			6.0	5.9	5.9	5.9					
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V				
			4.5	0.1	0.1	0.1					
			6.0	0.1	0.1	0.1					
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA				
			I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0		8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or Q (Figures 1 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PHL}	Maximum Propagation Delay, Reset to Q or Q (Figures 2 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

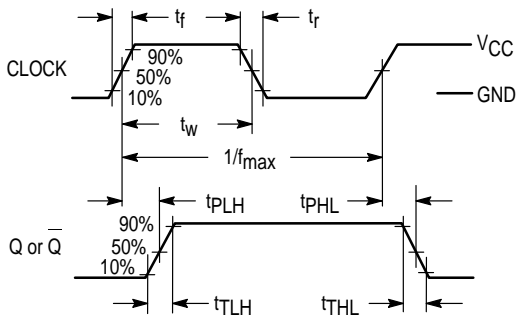


Figure 1.

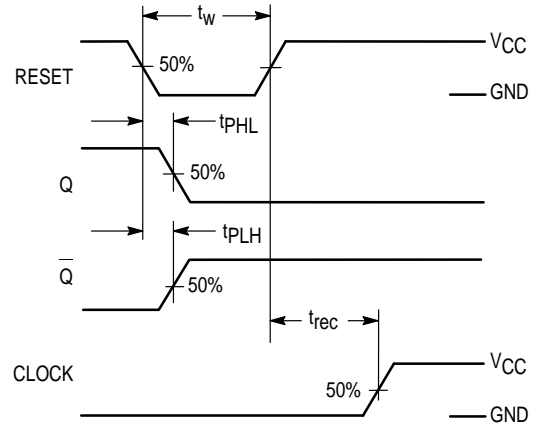


Figure 2.

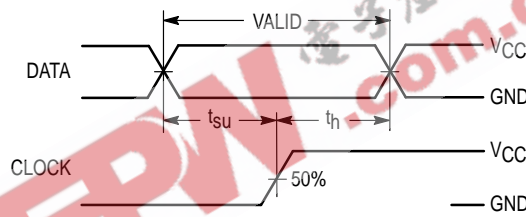
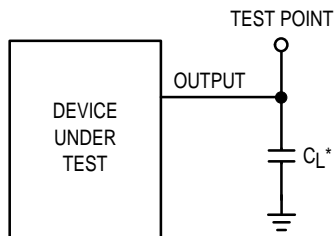


Figure 3.

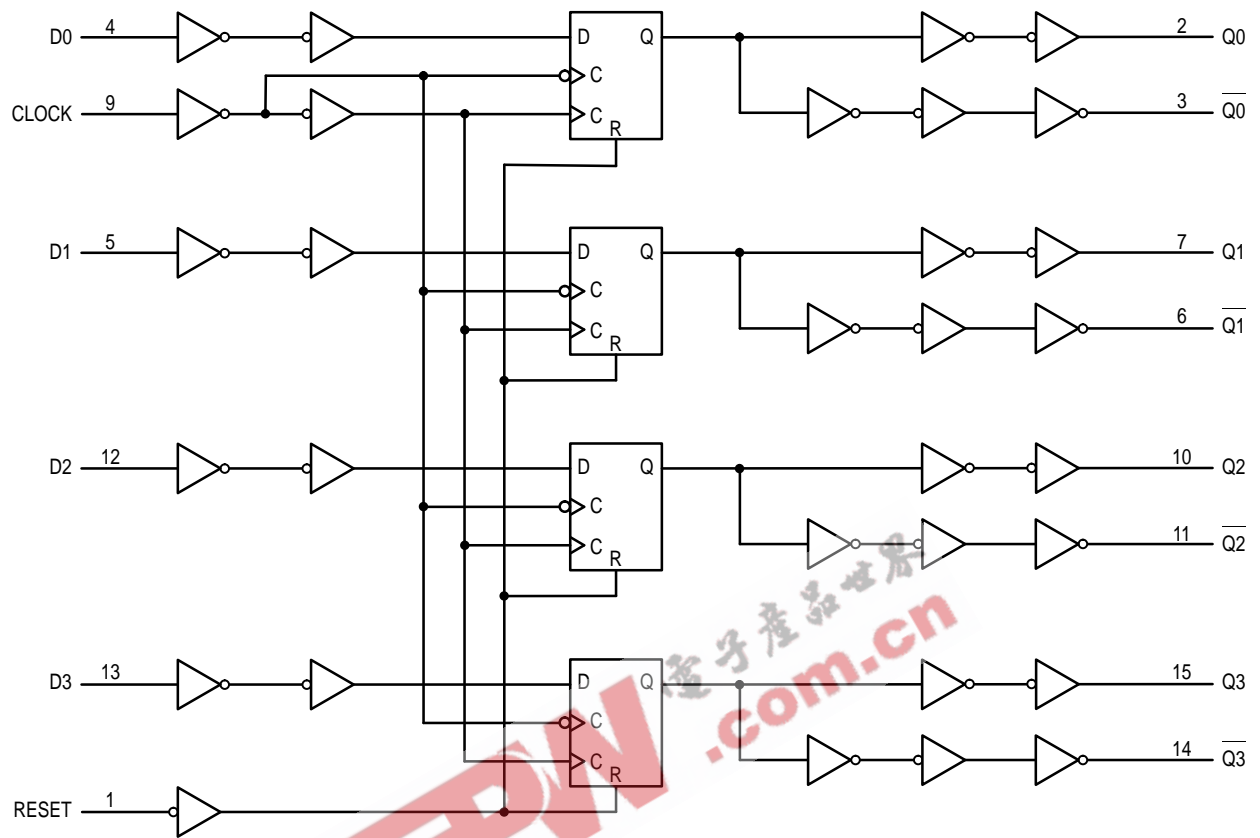
TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 4.

EXPANDED LOGIC DIAGRAM



OUTLINE DIMENSIONS

J SUFFIX
CERAMIC PACKAGE
CASE 620-10
ISSUE V

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.01

D 16 PL $\oplus 0.25 (0.010) \text{ (M) T A (S)}$

J 16 PL $\oplus 0.25 (0.010) \text{ (M) T B (S)}$

N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

D 16 PL $\oplus 0.25 (0.010) \text{ (M) T A (M)}$

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J

NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

P 8 PL $\oplus 0.25 (0.010) \text{ (M) B (M)}$

D 16 PL $\oplus 0.25 (0.010) \text{ (M) T B (S) A (S)}$

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USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609
INTERNET: <http://Design-NET.com>

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



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