

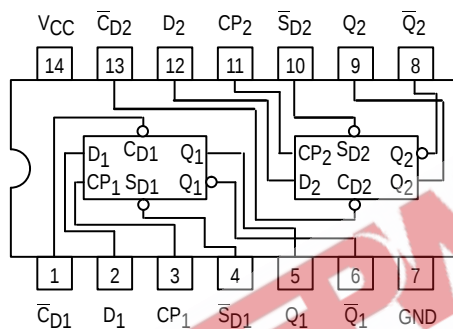


DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

The MC54/74F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q , $\bar{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

- ESD > 4000 Volts

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Input	Outputs
@ t_h	@ $t_h + 1$
D	Q $\bar{Q}$
L	L H
H	H L

Asynchronous Inputs:

- LOW Input to $\bar{S}_D$ sets Q to HIGH level
- LOW Input to $\bar{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\bar{C}_D$ and $\bar{S}_D$ makes both Q and $\bar{Q}$ HIGH

H = HIGH Voltage Level

L = LOW Voltage Level

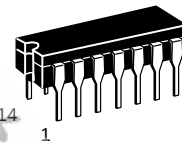
t_h = Bit time before clock pulse

$t_h + 1$ = Bit time after clock pulse

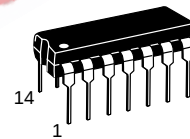
MC54/74F74

DUAL D-TYPE POSITIVE
EDGE-TRIGGERED FLIP-FLOP

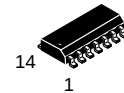
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

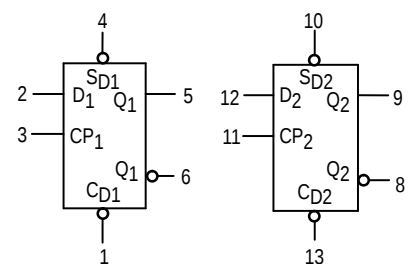


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

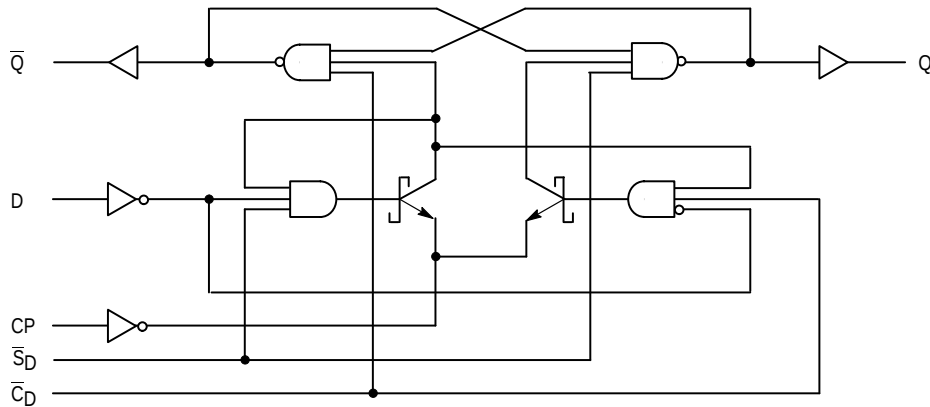
LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

MC54/74F74

LOGIC DIAGRAM



NOTE:

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current (CP and D Inputs) (C _D and S _D Inputs)			-0.6	mA	V _{IN} = 0.5V	V _{CC} = MAX
				-1.8	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		10.5	16	mA	V _{CP} = 0 V	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F74

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100		100		100		MHz
t _{PLH}	Propagation Delay	3.8	6.8	3.8	8.5	3.8	7.8	ns
t _{PHL}	CP _n to Q _n or $\overline{Q}_n$	4.4	8.0	4.4	10.5	4.4	9.2	
t _{PLH}	Propagation Delay	2.5	6.1	2.5	8.0	2.5	7.1	ns
t _{PHL}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	3.5	9.0	3.5	11.5	3.5	10.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = 5.0V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0			3.0		2.0		ns
t _S (L)	D _N to CP _N	3.0			4.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0			2.0		1.0		
t _H (L)	D _N to CP _N	1.0			2.0		1.0		ns
t _W (H)	CP _N Pulse Width, HIGH	4.0			4.0		4.0		
t _W (L)	or LOW	5.0			6.0		5.0		ns
t _W (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.0			4.0		4.0		ns
t _{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			3.0		2.0		ns