National Semiconductor

F100130
Triple D Latch

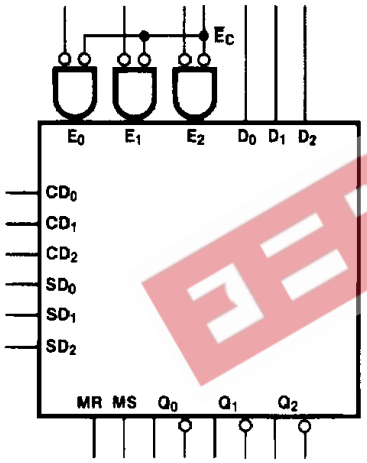
General Description

The F100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{E}_C$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{E}_n$), Direct Set (SD_n) and Direct Clear (CD_n) inputs. The Q output follows its Data (D) input when both $\overline{E}_n$ and $\overline{E}_C$ are LOW (transparent mode). When either $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH, a latch stores the last valid data present on its D_n input before $\overline{E}_n$ or $\overline{E}_C$ goes HIGH.

Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs. The individual CD_n and SD_n also override the Enable inputs. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 8

Logic Symbol



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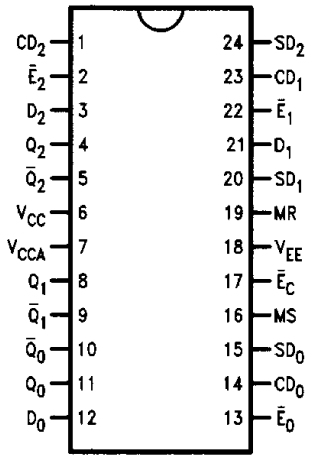
Pin Names	Description
CD_0–CD_2	Individual Direct Clear Inputs
SD_0–SD_2	Individual Direct Set Inputs
$\overline{E}_0$–$\overline{E}_2$	Individual Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable Input (Active LOW)
D_0–D_2	Data Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



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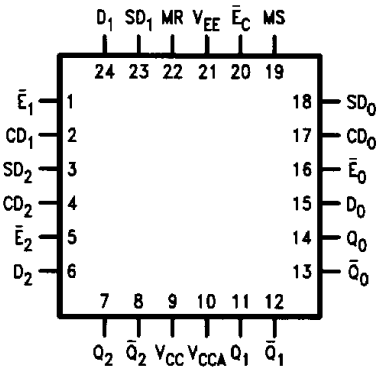
24-Pin Quad Cerpak



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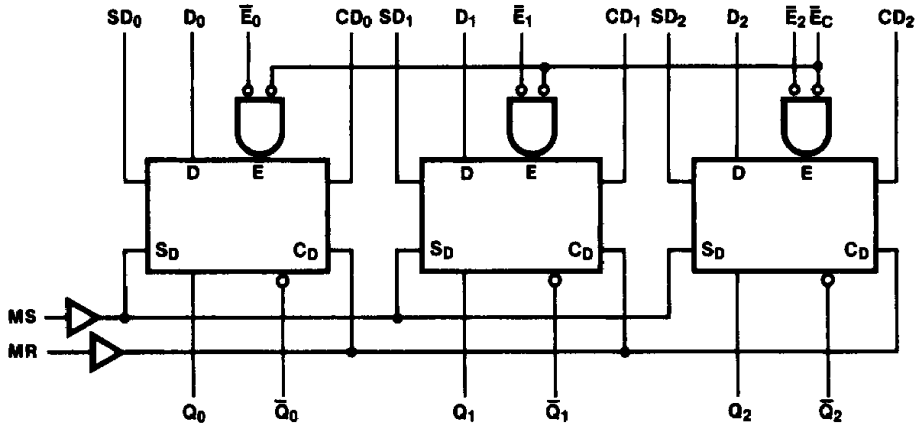
Logic Diagram



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Truth Tables (Each Latch)

Latch Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
X	H	X	L	L	Latched*
X	X	H	L	L	Latched*

*Retains data presented before $\overline{E}$ positive transition

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined

Asynchronous Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current					
	D_n			350		
	CD_n, SD_n			530	μA	V_{IN} = $V_{IH\ (Max)}$
	$\overline{E}_n$			240		
	$\overline{E}_C$, MR, MS			450		
I_{EE}	Power Supply Current	−149	−106	−74	mA	Inputs Open

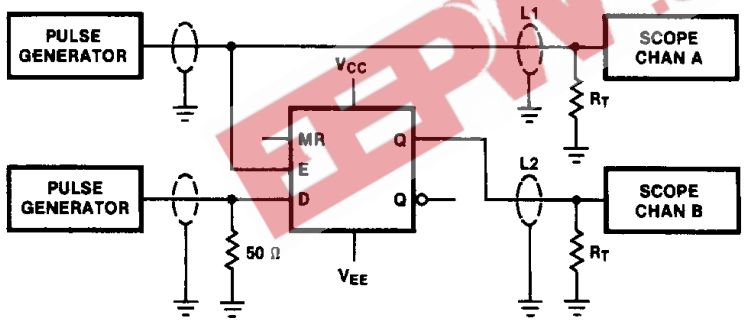
Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.80	0.50	1.70	0.50	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	2.10	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	2.00	0.60	1.75	0.60	2.00	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.50	1.10	2.40	1.10	2.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*
t_s	Setup Time								
	D_0–D_2	0.90		0.70		0.90			
	CD_n, SD_n (Release Time)	1.20		1.10		1.40		ns	*Figures 3* and *4*
	MR, MS (Release Time)	1.90		1.90		2.00			
t_h	Hold Time D_0–D_2	0.60		0.60		0.80		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.60	0.50	1.50	0.50	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	1.90	0.75	1.80	0.75	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	1.80	0.60	1.55	0.60	1.80	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.30	1.10	2.20	1.10	2.40	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_2 CD_n, SD_n (Release Time) MR, MS (Release Time)	 0.80 1.10 1.80		 0.60 1.00 1.80		 0.80 1.30 2.00		ns	*Figures 3* and *4*
t_h	Hold Time D_0–D_2	0.50		0.50		0.70		ns	*Figure 4*
t_{pw}(L)	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw}(H)	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

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FIGURE 1. AC Test Circuit

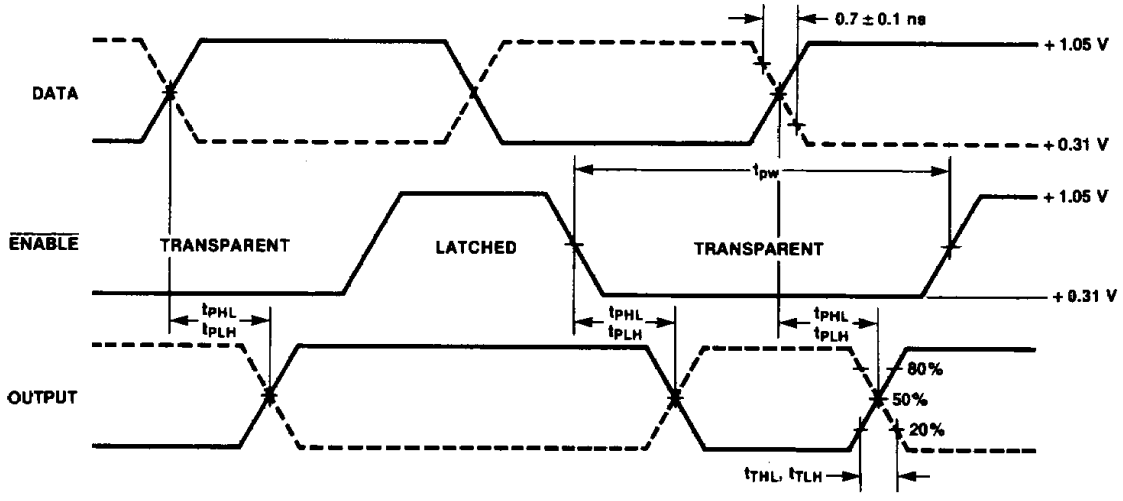

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FIGURE 2. Enable Timing

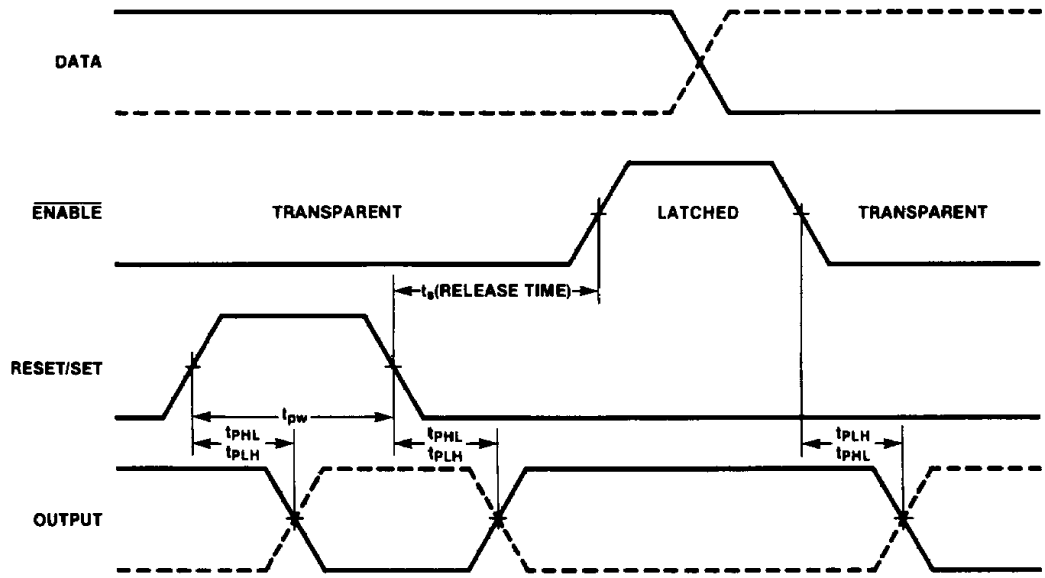

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FIGURE 3. Reset Timing

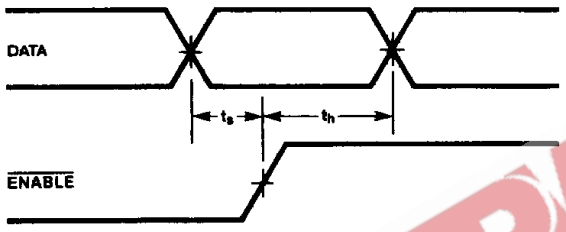

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FIGURE 4. Data Setup and Hold Time

Notes:
t_s is the minimum time before the transition of the enable that information must be present at the data input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.