# MC74HCT74A

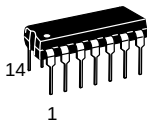
# Dual D Flip-Flop with Set and Reset with LSTTL Compatible Inputs

## High–Performance Silicon–Gate CMOS

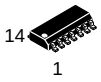
The MC74HCT74A is identical in pinout to the LS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip–flops with individual Set, Reset, and Clock inputs. Information at a D–input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and $\overline{Q}$ outputs are available from each flip–flop. The Set and Reset inputs are asynchronous.

- Output Drive Capability: 10 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 µA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates




**N SUFFIX**
PLASTIC PACKAGE
CASE 646–06

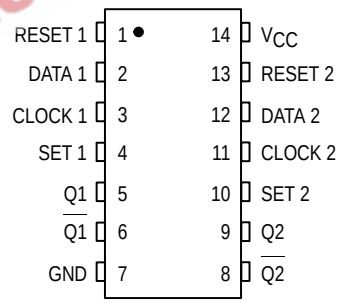



**D SUFFIX**
SOIC PACKAGE
CASE 751A–03

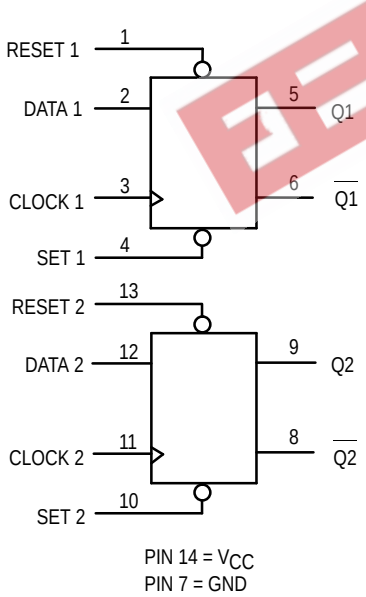
**ORDERING INFORMATION**

| | |
|---|---|
| MC54HCTXXAJ | Ceramic |
| MC74HCTXXAN | Plastic |
| MC74HCTXXAD | SOIC |

**PIN ASSIGNMENT**




**LOGIC DIAGRAM**




PIN 14 = $V_{CC}$
PIN 7 = GND

| Design Criteria | Value | Units |
|---|---|---|
| Internal Gate Count* | 34 | ea. |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | µW |
| Speed Power Product | .0075 | pJ |

* Equivalent to a two–input NAND gate.

**FUNCTION TABLE**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Set | Reset | Clock | Data | Q | Q |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | No Change | |
| H | H | H | X | No Change | |
| H | H | ↓ | X | No Change | |

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | – 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | – 1.5 to $V_{CC}$ + 1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air Plastic DIP† | 750 | mW |
| | SOIC Package† | 500 | |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: –10mW/°C from 65° to 125°C
SOIC Package: –7mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | – 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 2.0<br>2.0 | 2.0<br>2.0 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 0.8<br>0.8 | 0.8<br>0.8 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 4.4<br>5.4 | 4.4<br>5.4 | 4.4<br>5.4 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 4.0 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 4.5<br>5.5 | 0.1<br>0.1 | 0.1<br>0.1 | 0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 4.0 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0 μA | 5.5 | 2.0 | 20 | 80 | μA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{in}$ = 2.4 V, Any One Input<br>$V_{in}$ = $V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0 μA | | ≥ –55°C | 25°C to 125°C | |
| | | | 5.5 | 2.9 | 2.4 | mA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V ± 10%, $C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|
| | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 30 | 24 | 20 | MHz |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4) | 24 | 30 | 36 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4) | 24 | 30 | 36 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 15 | 19 | 22 | ns |
| $C_{in}$ | Maximum Input Capacitance | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Enabled Output)* | 130 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** ($V_{CC}$ = 5.0 V ± 10%, $C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Fig. | Guaranteed Limit | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{su}$ | Minimum Setup Time, Data to Clock | 3 | 15 | | 19 | | 22 | | ns |
| $t_h$ | Minimum Hold Time, Clock to Data | 3 | 3 | | 3 | | 3 | | ns |
| $t_{rec}$ | Minimum Recovery Time, Set or Reset Inactive to Clock | 2 | 6 | | 8 | | 9 | | ns |
| $t_w$ | Minimum Pulse Width, Clock | 1 | 15 | | 19 | | 22 | | ns |
| $t_w$ | Minimum Pulse Width, Set or Reset | 2 | 15 | | 19 | | 22 | | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times | 1 | | 500 | | 500 | | 500 | ns |

## SWITCHING WAVEFORMS

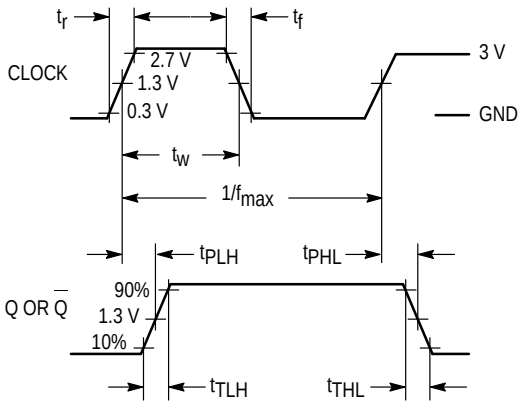



**Figure 1.**

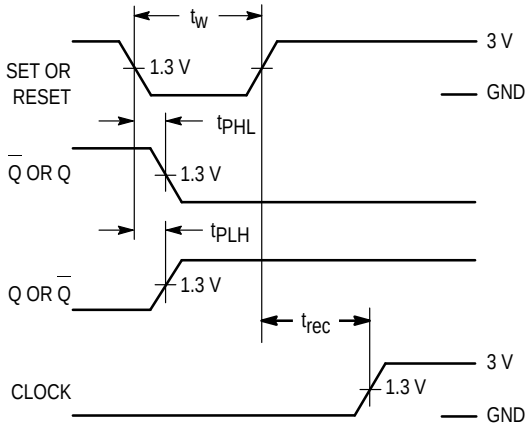



**Figure 2.**

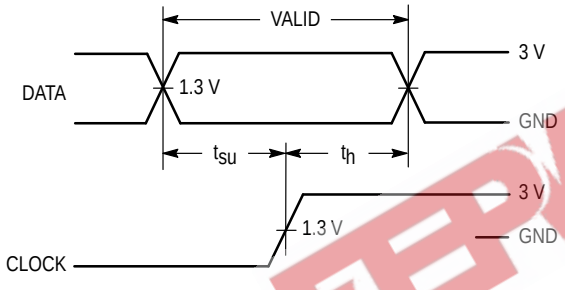
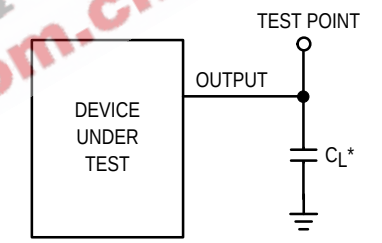


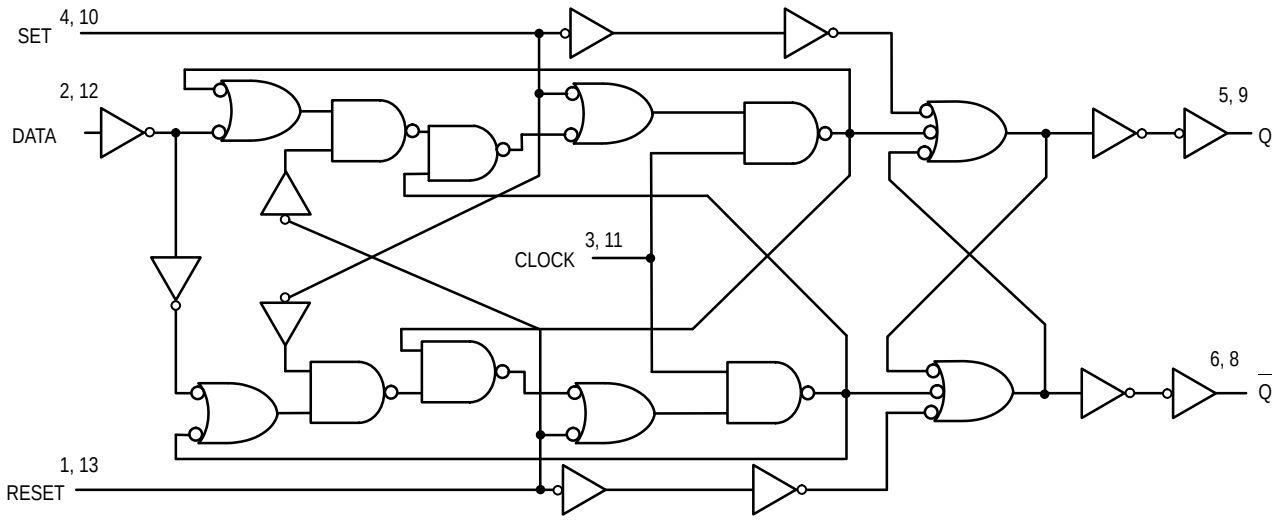

**Figure 3.**




* Includes all probe and jig capacitance

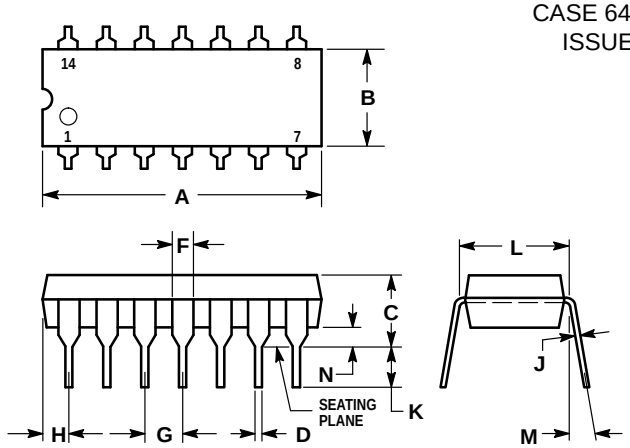
**Figure 4.**

## EXPANDED LOGIC DIAGRAM



## OUTLINE DIMENSIONS

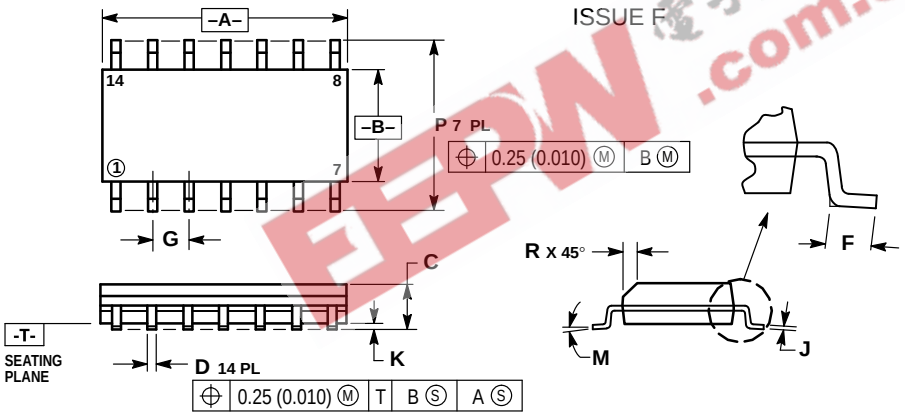
### N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L




NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.015 | 0.039 | 0.39 | 1.01 |

### D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |



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