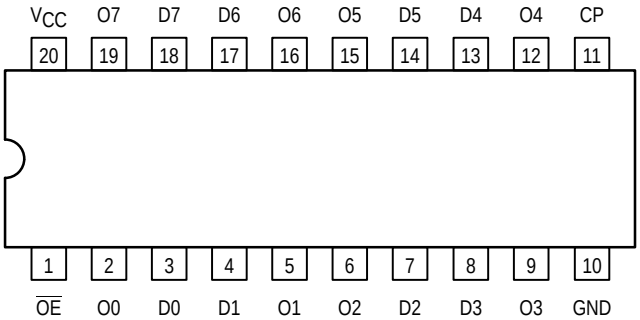
Low-Voltage Quiet CMOS Octal D-Type Flip-Flop
(3-State, Non-Inverting)

The MC74LVQ374 is a high performance, non–inverting octal D–type flip–flop operating from a 2.7 to 3.6V supply. The MC74LVQ374 is suitable for TTL level bus oriented applications where a memory element is required.

Current drive capability is 12mA at the outputs. The MC74LVQ374 consists of 8 edge–triggered flip–flops with individual D–type inputs and 3–state true outputs. The buffered clock and buffered Output Enable ($\overline{OE}$) are common to all flip–flops. The eight flip–flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW–to–HIGH Clock (CP) transition. With the $\overline{OE}$ LOW, the contents of the eight flip–flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. The $\overline{OE}$ input level does not affect the operation of the flip–flops.

- Designed for 2.7 to 3.6V V_{CC} Operation – Ideal for Low Power/Low Noise Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Guaranteed Skew Specifications
- Guaranteed Incident Wave Switching into 75Ω
- Low Static Supply Current (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V

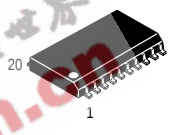
Pinout: 20–Lead (Top View)



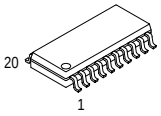
MC74LVQ374

LVQ

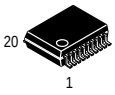
LOW–VOLTAGE CMOS OCTAL D–TYPE FLIP–FLOP



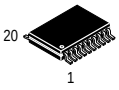
DW SUFFIX
PLASTIC SOIC
CASE 751D–04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967–01



SD SUFFIX
PLASTIC SSOP
CASE 940C–03

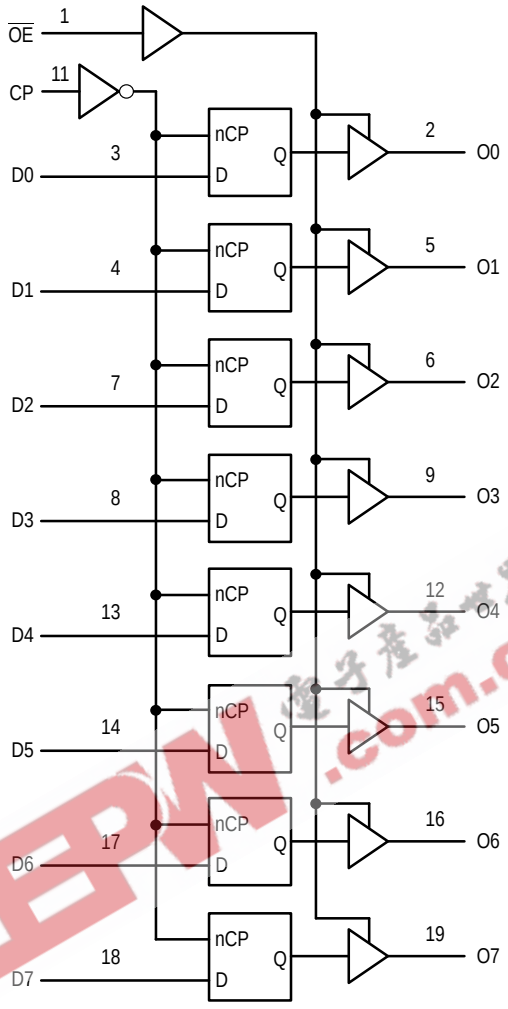


DT SUFFIX
PLASTIC TSSOP
CASE 948E–02

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
CP	Clock Pulse Input
D0–D7	Data Inputs
O0–O7	3–State Outputs

LOGIC DIAGRAM



INPUTS			INTERNAL LATCHES	OUTPUTS	
$\overline{OE}$	CP	Dn	Q	On	OPERATING MODE
L L	↑ ↑	l h	L H	L H	Load and Read Register
L	↥	X	NC	NC	Hold and Read Register
H	↥	X	NC	Z	Hold and Disable Outputs
H H	↑ ↑	l h	L H	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ = Low–to–High Transition; ↥ = Not a Low–to–High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le V_{CC} + 0.5V$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–20	$V_I = -0.5V$	mA
		+20	$V_I = V_{CC} + 0.5V$	mA
I_{OK}	DC Output Diode Current	–20	$V_O = -0.5V$	mA
		+20	$V_I = V_{CC} + 0.5V$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current	±400		mA
I_{GND}	DC Ground Current	±400		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.0	3.3	3.6	V
V_I	Input Voltage	0		V_{CC}	V
V_O	Output Voltage	0		V_{CC}	V
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta V/\Delta t$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		125	mV/ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$, V_O = 0.1V or V_{CC} – 0.1V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$, V_O = 0.1V or V_{CC} – 0.1V		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –50µA	V_{CC} – 0.1		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –12mA	2.48		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OL} = 50µA		0.1	V
		$2.7V \le V_{CC} \le 3.6V$; I_{OL}= 12mA		0.4	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $V_I = V_{CC}$, GND		±1.0	µA
I_{OZ}	Maximum 3–State Leakage Current	$V_I(\overline{OE}) = V_{IL}$, V_{IH}; V_I, $V_O = V_{CC}$, GND		±2.5	µA
I_{OLD}	Minimum Dynamic Output Current (Note 2)	V_{CC} = 3.6V; V_{OLD} = 0.8V Max		36	mA
I_{OHD}		V_{CC} = 3.6V; V_{OHD} = 2.0V Min		–25	mA
I_{CC}	Quiescent Supply Current	$2.7V \le V_{CC} \le 3.6V$; $V_I = V_{CC}$, GND		10	µA

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.
2. Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed. Maximum test duration is 2ms, one output loaded at a time.

DYNAMIC SWITCHING CHARACTERISTICS (V_{CC} = 3.3V)

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 1)	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.6	1.0	V
V_{OLV}	Dynamic LOW Valley Voltage (Note 1)	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		–0.5	–1.0	V
V_{IHD}	High Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 0V to Threshold, f=1MHz		1.5	2.0	V
V_{ILD}	Low Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 3.3V to Threshold, f=1MHz		1.5	0.8	V

1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW. The remaining output is measured in the LOW state.
2. Number of data inputs is defined as “n” switching, “n–1” inputs switching 0V to 3.3V.

AC CHARACTERISTICS ($t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Limits									Unit
		T_A = +25°C						T_A = –40°C to +85°C			
		V_{CC} = 3.0V to 3.6V			V_{CC} = 2.7V			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
		Min	Typ	Max	Min	Typ	Max	Min	Max	Max	
t_{PLH} t_{PHL}	Propagation Delay CP to On	3.0 3.0	11.0 9.5	14.0 12.0	3.0 3.0	12.0 11.0	16.0 14.0	3.0 3.0	14.5 13.5	17.5 16.0	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	3.0 3.0	8.0 8.0	10.0 10.0	3.0 3.0	9.0 9.0	11.5 11.5	3.0 3.0	10.5 10.5	12.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	1.0 1.0	9.0 7.0	11.5 9.0	1.0 1.0	11.0 8.5	13.0 11.0	1.0 1.0	13.0 10.0	14.0 11.5	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 1)		1.0 1.0	1.5 1.5		1.0 1.0	1.5 1.5		1.5 1.5		ns

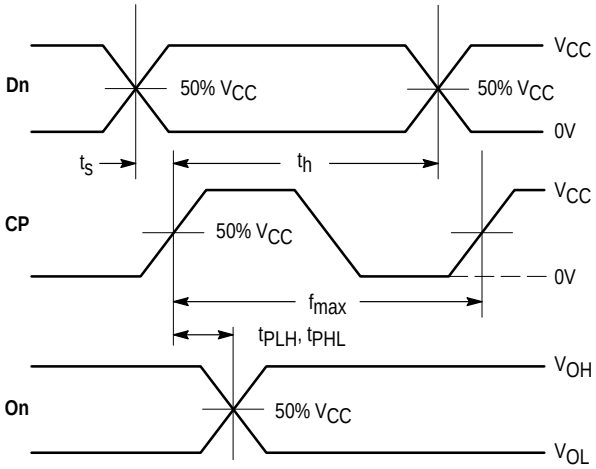
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

AC OPERATING REQUIREMENTS ($t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

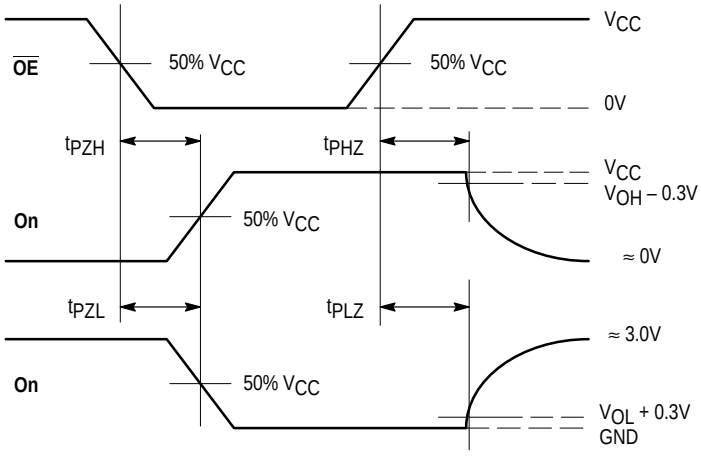
Symbol	Parameter	Limits				Unit
		T_A = +25°C		T_A = –40°C to +85°C		
		V_{CC} = 3.0V to 3.6V	V_{CC} = 2.7V	V_{CC} = 3.0V to 3.6V	V_{CC} = 2.7V	
		Min	Min	Min	Min	
t_s	Setup TIme, HIGH or LOW Dn to CP	3.0	4.0	3.0	4.5	ns
t_h	Hold TIme, HIGH or LOW Dn to CP	1.5	1.5	1.5	1.5	ns
t_w	CP Pulse Width, HIGH or LOW	4.0	5.0	4.0	6.0	ns

CAPACITIVE CHARACTERISTICS

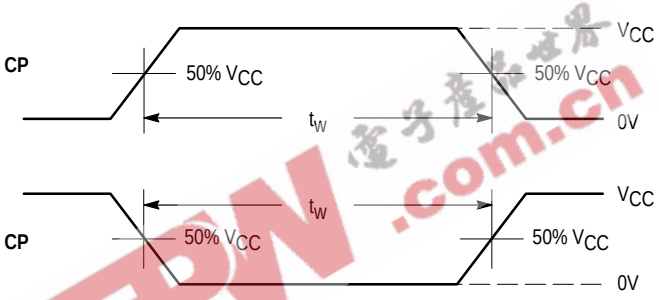
Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	4.5	pF



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

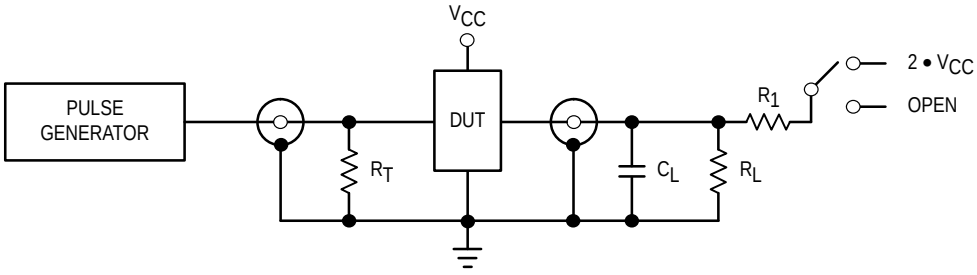


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F$ = 2.5ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8V$, $V_{OH} \geq 2.0V$

Figure 1. AC Waveforms



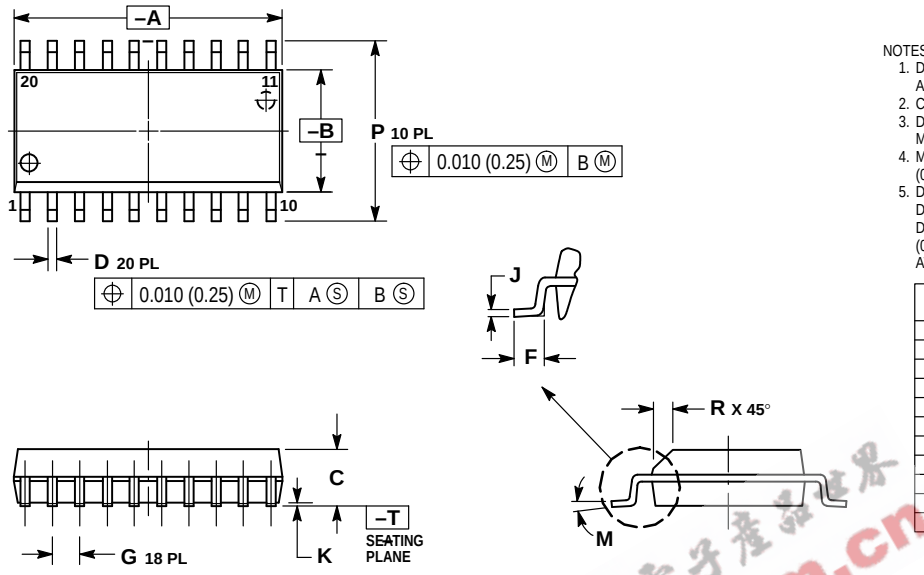
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	2 • V_{CC}
Open Collector/Drain t_{PLH} and t_{PHL}	2 • V_{CC}
t_{PZH}, t_{PHZ}	Open

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 2. Test Circuit

OUTLINE DIMENSIONS

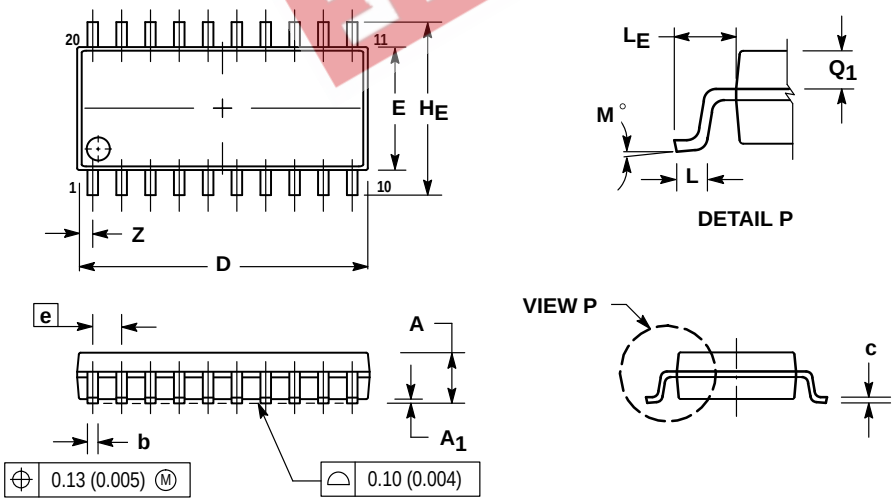
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O

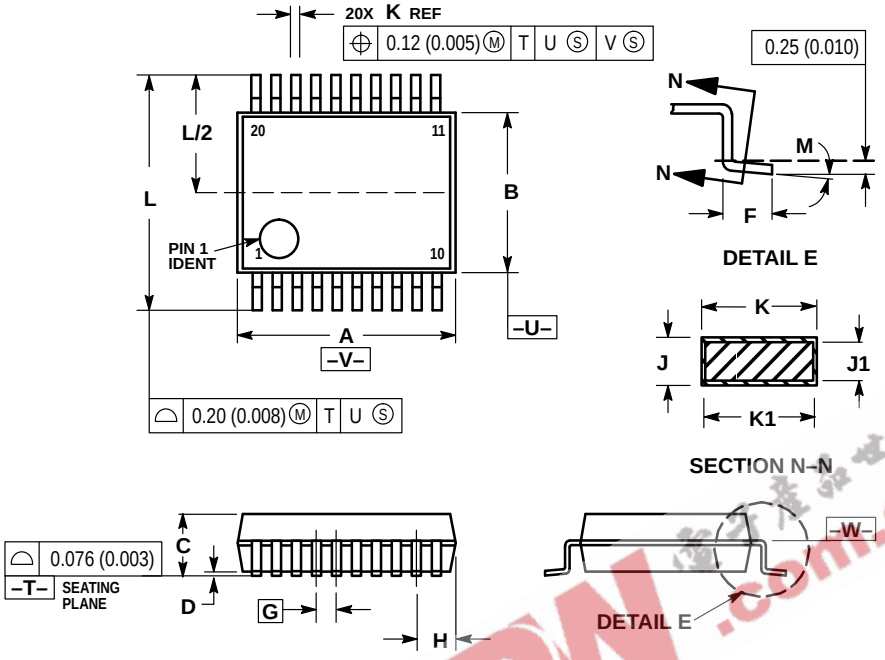


NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

OUTLINE DIMENSIONS

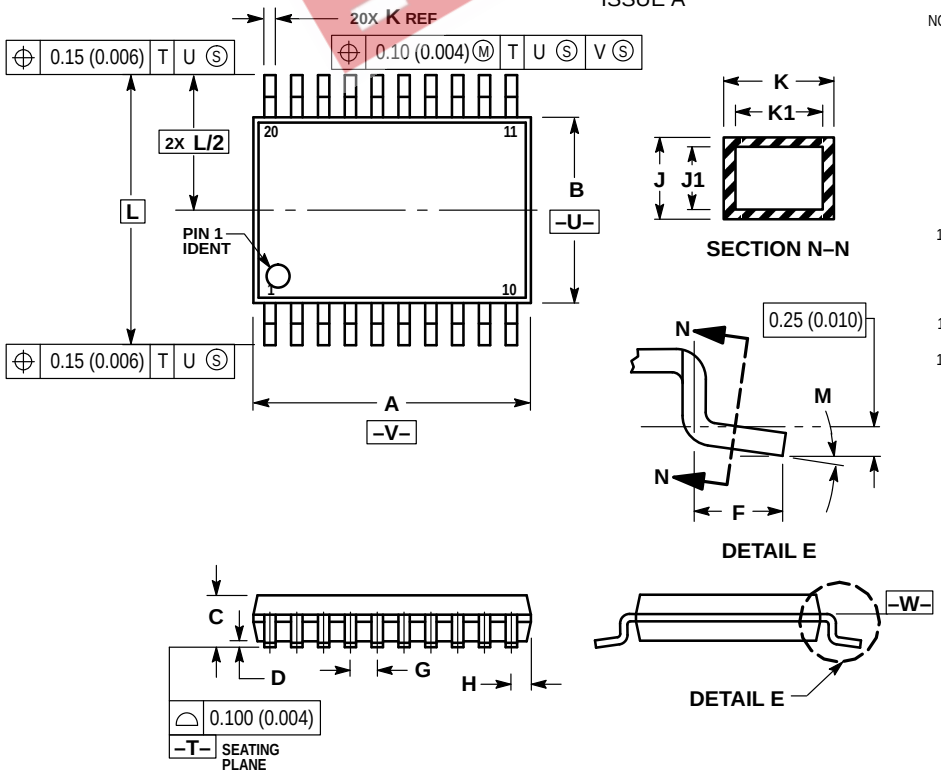
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940C–03
ISSUE B



NOTES:
13 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
14 CONTROLLING DIMENSION: MILLIMETER.
15 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
16 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
17 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
18 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
19 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
6 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7 CONTROLLING DIMENSION: MILLIMETER.
8 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
9 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
10 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
11 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
12 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

How to reach us:
USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com –TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298