MOTOROLA

MC74F377

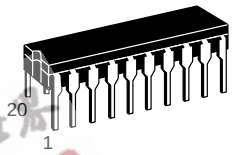
OCTAL D FLIP-FLOP WITH ENABLE

The MC74F377 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable (E) is LOW. This device is supplied in a 20-pin package.

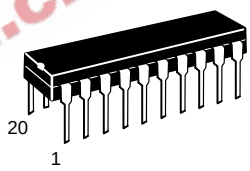
- High Impedance NPN Base Inputs for Reduced Loading (20 µA in HIGH and LOW States)
- Ideal for Addressable Register Applications
- Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- See: MC74F373 for Transparent Latch Version
  MC74F374 for 3-State Version

OCTAL D FLIP-FLOP WITH ENABLE

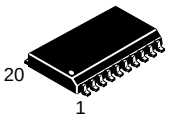
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

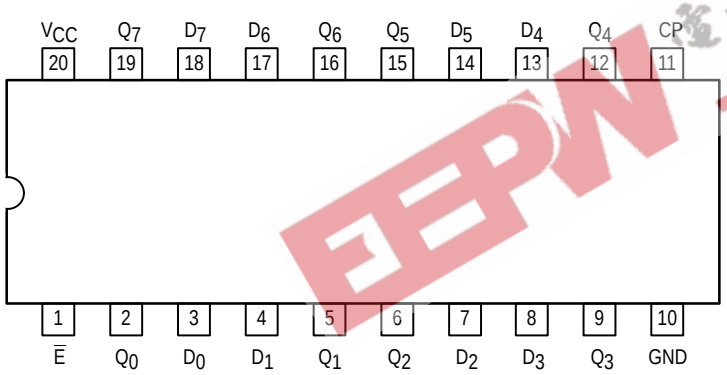


DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

CONNECTION DIAGRAM (TOP VIEW)



FUNCTION TABLE

Operating Mode	Inputs			Outputs
	CP	$\overline{E}$	D_n	Q_n
Load “1”	↑	l	h	H
Load “0”	↑	l	l	L
Hold (do nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH voltage level steady state; h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition; L = LOW voltage level steady state; l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition; X = Don’t Care; ↑ = LOW-to-HIGH clock transition

MC74F377

FUNCTIONAL DESCRIPTION

The MC74F377 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Enable ($\overline{E}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — HIGH	74			–1.0	mA
I_{OL}	Output Current — LOW	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	2.5	2.5			V	I_{OH} = –1.0 mA	V_{CC} = 4.5 V
		2.7	2.7					V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
I_{IL}	Input LOW Current				–20	µA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Total Supply Current		I_{CCH}	55	72	mA	D_n = 4.5 V, CP = ↑, $\overline{E}$ = GND	V_{CC} = MAX
			I_{CCL}	70	90	mA	D_n = $\overline{E}$ = GND, CP = ↑	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF Min	Typ	Max	74F T_A = 0 to +70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF Min	Max	Unit
f_{MAX}	Maximum Clock Frequency	110	120		100		MHz
t_{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10	ns
t_{PHL}	CP to Q_n	4.0	7.0	9.0	4.0	10.5	

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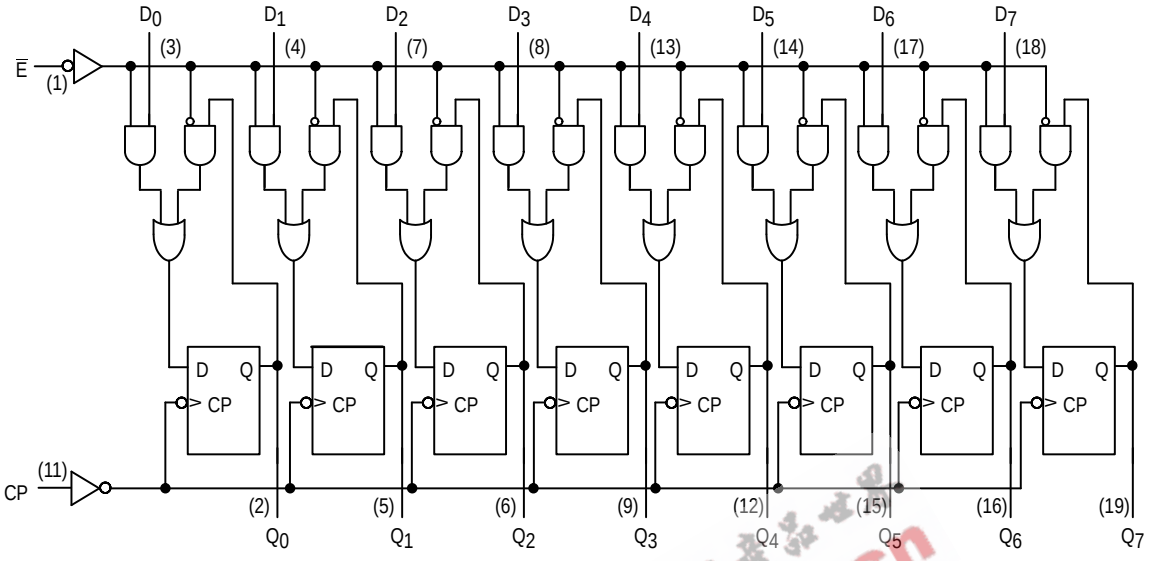
LOGIC DIAGRAM



V_{CC} = PIN 20
GND = PIN 10

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F T_A = +25°C, V_{CC} = 5.0 V, C_L = 50 pF			74F T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{s(H)}$	Setup Time, HIGH or LOW	3.0			3.0			ns
$t_{s(L)}$	D_n to CP	3.0			3.0			
$t_{h(H)}$	Hold Time, HIGH or LOW	1.0			1.0			ns
$t_{h(L)}$	D_n to CP	1.0			1.0			
$t_{s(H)}$	Setup Time, HIGH or LOW	2.5			2.5			ns
$t_{s(L)}$	$\overline{E}$ to CP	4.0			4.0			
$t_{h(H)}$	Hold Time, HIGH or LOW	0			0			ns
$t_{h(L)}$	$\overline{E}$ to CP	0			0			
$t_{w(H)}$	Clock Pulse Width	4.0			5.0			ns
$t_{w(L)}$	HIGH or LOW	4.0			5.0			