

# MC74LVX74

## Dual D-Type Flip-Flop with Set and Clear

### With 5.0 V-Tolerant Inputs

The MC74LVX74 is an advanced high speed CMOS D-type flip-flop. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The signal level applied to the D input is transferred to O output during the positive going transition of the Clock pulse.

Clear ( $\overline{CD}$ ) and Set ( $\overline{SD}$ ) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

#### Features

- High Speed:  $f_{max} = 145$  MHz (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 2$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Pb-Free Packages are Available\*

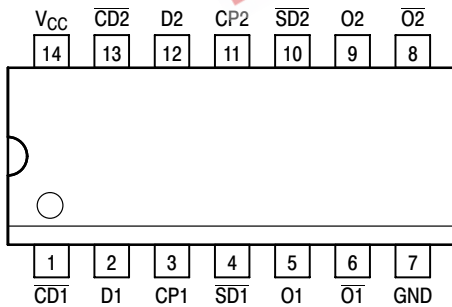


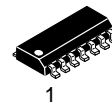
Figure 1. 14-Lead Pinout (Top View)



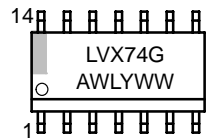
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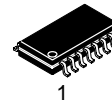
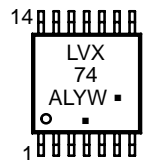
#### MARKING DIAGRAMS



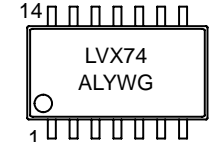
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
M SUFFIX  
CASE 965



- A = Assembly Location
- WL, L = Wafer Lot
- Y = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
D1, D2	Data Inputs
$\overline{CD1}$ , $\overline{CD2}$	Direct Clear Inputs
$\overline{SD1}$ , $\overline{SD2}$	Direct Set Inputs
O <sub>n</sub> , $\overline{O_n}$	Outputs

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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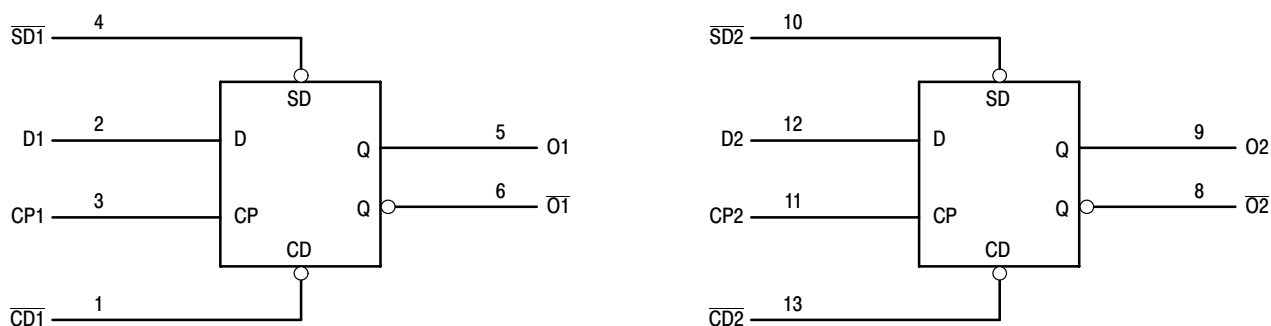


Figure 2. Logic Diagram

INPUTS				OUTPUTS		OPERATING MODE
SD $\bar{n}$	CD $\bar{n}$	CP $n$	D $n$	Q $n$	Q $\bar{n}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	$\uparrow$	h	H	L	Load and Read Register
H	H	$\uparrow$	l	L	H	
H	H	$\nabla$	X	NC	NC	Hold

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable;  $\uparrow$  = Low-to-High Transition;  $\nabla$  = Not a Low-to-High Transition; For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs

### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OH</sub> = -50μA I <sub>OH</sub> = -50μA I <sub>OH</sub> = -4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50μA I <sub>OL</sub> = 50μA I <sub>OL</sub> = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6			2.0		20.0	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay CP to O or $\bar{O}$	V <sub>CC</sub> = 2.7V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		7.3 9.8	15.0 18.5	1.0 1.0	18.5 22.0	ns
		V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.7 8.2	9.7 13.2	1.0 1.0	11.5 15.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay $\bar{SD}$ or $\bar{CD}$ to O or $\bar{O}$	V <sub>CC</sub> = 2.7V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		8.4 10.9	15.6 19.1	1.0 1.0	18.5 22.0	ns
		V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		6.6 9.1	10.1 13.6	1.0 1.0	12.0 15.5	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	V <sub>CC</sub> = 2.7V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	55 45	135 60		50 40		MHz
		V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	95 60	145 85		80 50		
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output-to-Output Skew (Note 1)	V <sub>CC</sub> = 2.7V V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 50pF C <sub>L</sub> = 50pF			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit		Unit
			T <sub>A</sub> = 25°C	T <sub>A</sub> = - 40 to 85°C	
t <sub>w</sub>	Minimum Pulse Width, CP	2.7V 3.3V ± 0.3	8.5 6.0	10.0 7.0	ns
t <sub>w</sub>	Minimum Pulse Width, $\bar{CD}$ or $\bar{SD}$	2.7V 3.3V ± 0.3	8.5 6.0	10.0 7.0	ns
t <sub>su</sub>	Minimum Setup Time, D to CP	2.7V 3.3V ± 0.3	8.0 5.5	9.5 6.5	ns
t <sub>h</sub>	Minimum Hold Time, D to CP	2.7V 3.3V ± 0.3	0.5 0.5	0.5 0.5	ns
t <sub>rec</sub>	Minimum Recovery Time, $\bar{SD}$ or $\bar{CD}$ to CP	2.7V 3.3V ± 0.3	6.5 5.0	7.5 5.0	ns

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## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
		Min	Typ	Max	Min	Max	
C <sub>in</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)		25				pF

2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/2 (per flip-flop). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns, C<sub>L</sub> = 50pF, V<sub>CC</sub> = 3.3V, Measured in SOIC Package)

Symbol	Characteristic	T <sub>A</sub> = 25°C		Unit
		Typ	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.5	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.3	-0.5	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V

## ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX74DR2	SOIC-14	2500 Tape & Reel
MC74LVX74DR2G	SOIC-14 (Pb-Free)	
MC74LVX74DT	TSSOP-14*	96 Units / Rail
MC74LVX74DTG	TSSOP-14*	
MC74LVX74DTR2	TSSOP-14*	2500 Tape & Reel
MC74LVX74DTR2G	TSSOP-14*	
MC74LVX74M	SOEIAJ-14	50 Units / Rail
MC74LVX74MG	SOEIAJ-14 (Pb-Free)	
MC74LVX74MEL	SOEIAJ-14	2000 Tape & Reel
MC74LVX74MELG	SOEIAJ-14 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## SWITCHING WAVEFORMS

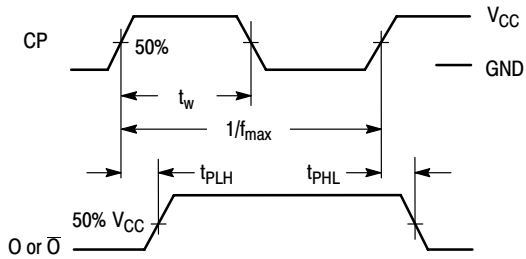


Figure 3.

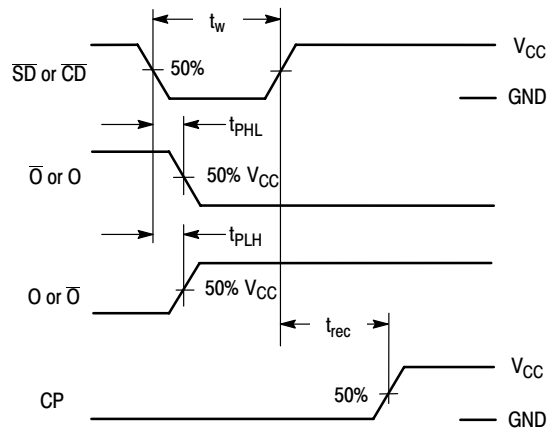


Figure 4.

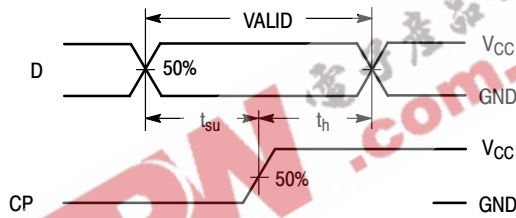
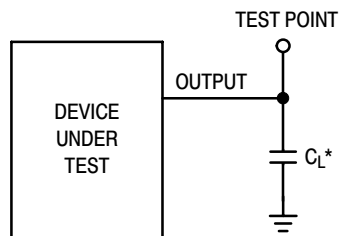


Figure 5.

## TEST CIRCUIT



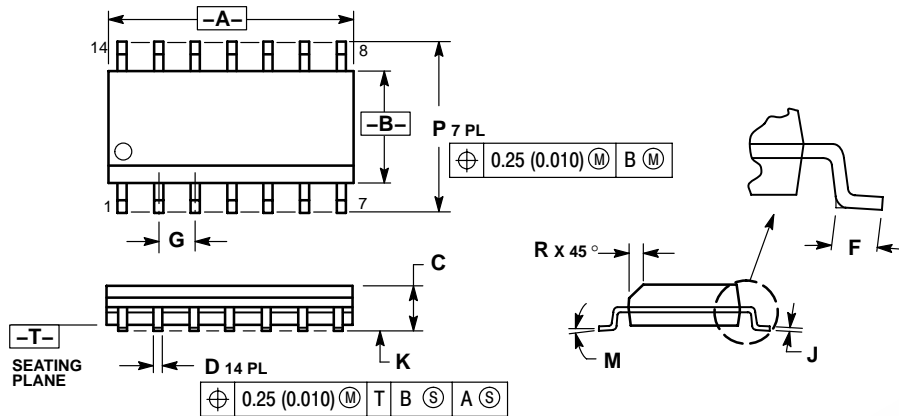
\*Includes all probe and jig capacitance

Figure 6.

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## PACKAGE DIMENSIONS

SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE G

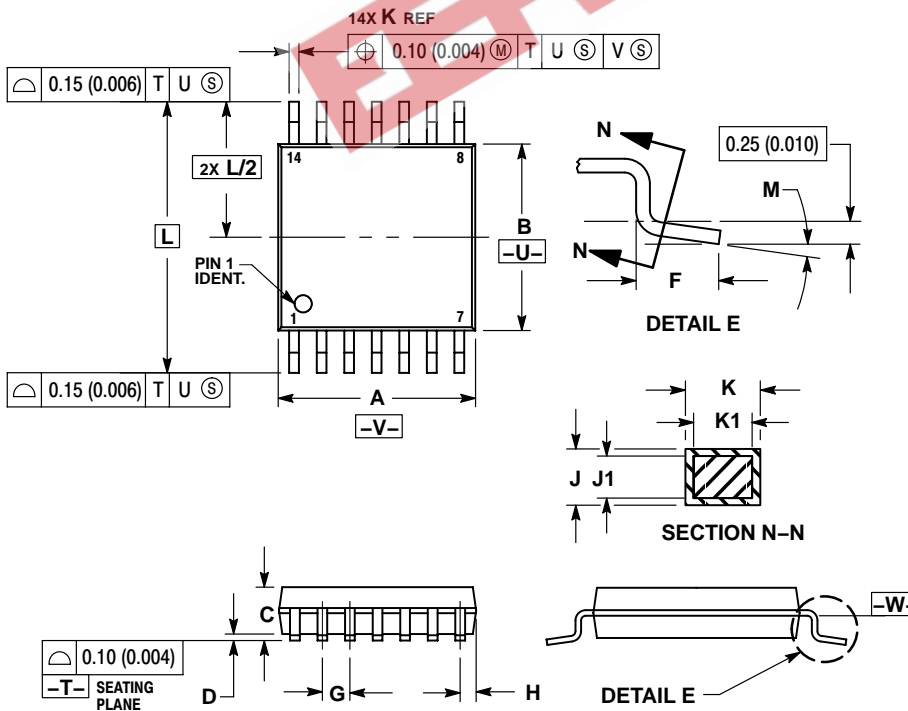


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14  
CASE 948G-01  
ISSUE A



NOTES:

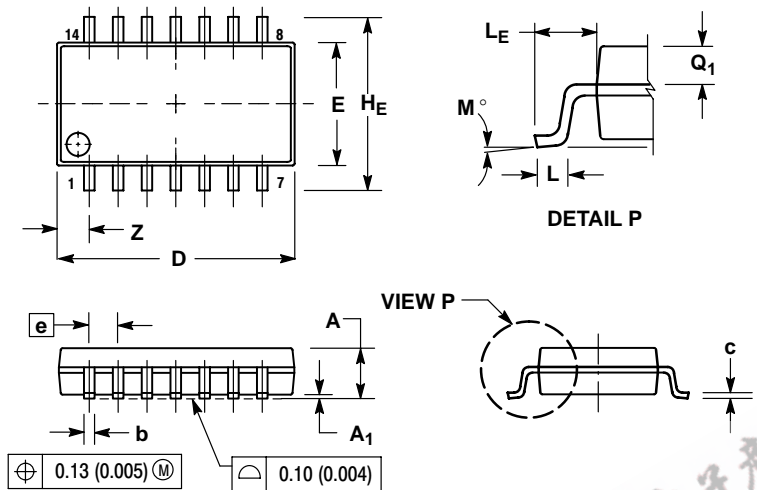
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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## PACKAGE DIMENSIONS

SOEIAJ-14  
CASE 965-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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