October 2005

# FDMA1027P

## Dual P-Channel PowerTrench® MOSFET

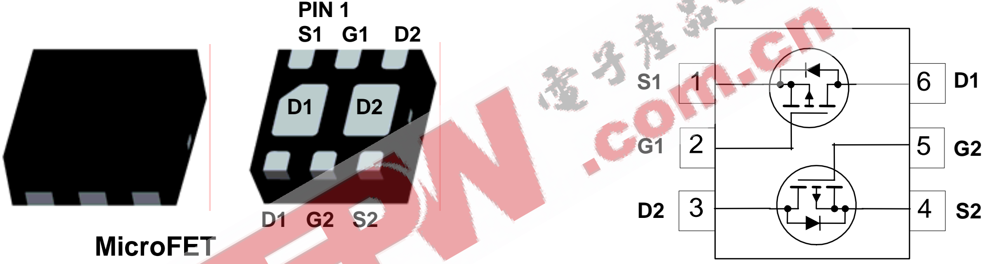
### General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

The MicroFET 2x2 package offers exceptional thermal performance for it's physical size and is well suited to linear mode applications.

### Features

- –3.0 A, –20V. $R_{DS(ON)}$ = 120 mΩ @ $V_{GS}$ = –4.5V
  $R_{DS(ON)}$ = 160 mΩ @ $V_{GS}$ = –2.5V
  $R_{DS(ON)}$ = 240 mΩ @ $V_{GS}$ = –1.8V
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm




## Absolute Maximum Ratings $T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | –20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±8 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | –2.2 | A |
| | – Pulsed | | –6 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 1.4 | W |
| | | (Note 1b) | 0.7 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $R_{θJA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 86 (Single Operation) | °C/W |
| $R_{θJA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 173 (Single Operation) | |
| $R_{θJA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1c) | 69 (Dual Operation) | |
| $R_{θJA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1d) | 151 (Dual Operation) | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| 027 | FDMA1027P | 7 in | 8 mm | 3000 units |



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## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 µA | –20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | –12 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V | | | –1 | µA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ± 8 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | –0.4 | –0.7 | –1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | 2 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –4.5 V, $I_D$ = –3.0 A<br>$V_{GS}$ = –2.5 V, $I_D$ = –2.5 A<br>$V_{GS}$ = –1.8 V, $I_D$ = –1.0 A<br>$V_{GS}$= –4.5 V, $I_D$ = –3.0 A, $T_J$=125°C | | 90<br>120<br>172<br>118 | 120<br>160<br>240<br>160 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –4.5 V, $V_{DS}$ = –5 V | –20 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = –3.0 A | | 7 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 435 | | pF |
| $C_{oss}$ | Output Capacitance | | | 80 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 45 | | pF |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –10 V, $I_D$ = –1 A, $V_{GS}$ = –4.5 V, $R_{GEN}$ = 6 Ω | | 9 | 18 | ns |
| $t_r$ | Turn–On Rise Time | | | 11 | 19 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 15 | 27 | ns |
| $t_f$ | Turn–Off Fall Time | | | 6 | 12 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –10 V, $I_D$ = –3.0 A, $V_{GS}$ = –4.5 V | | 4 | 6 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 0.8 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 0.9 | | nC |

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## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | –1.1 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –1.1 A (Note 2) | | –0.8 | –1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = –3.0 A, $dI_F/dt$ = 100 A/µs | | 17 | | ns |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 6 | | nC |

**Notes:**

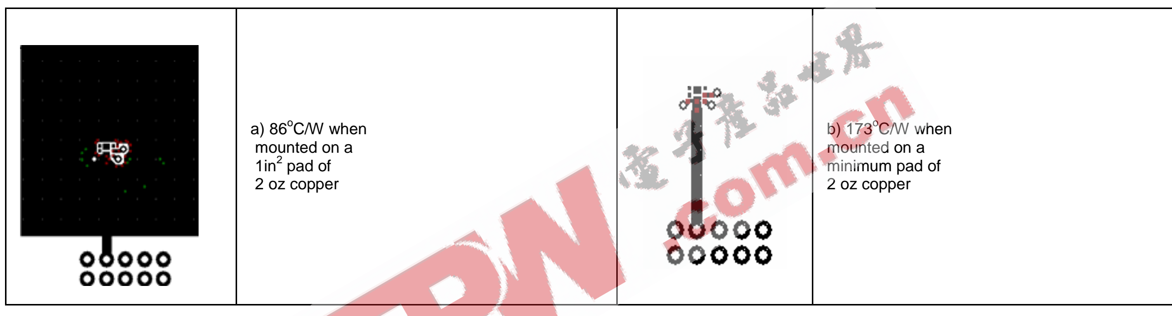
**1.** $R_{\theta JA}$ is determined with the device mounted on a 1 in$^2$ oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

**(a)** $R_{\theta JA}$ = 86°C/W when mounted on a 1in$^2$ pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB

**(b)** $R_{\theta JA}$ = 173°C/W when mounted on a minimum pad of 2 oz copper

**(c)** $R_{\theta JA}$ = 69°C/W when mounted on a 1in$^2$ pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB

**(d)** $R_{\theta JA}$ = 151°C/W when mounted on a minimum pad of 2 oz copper




Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics

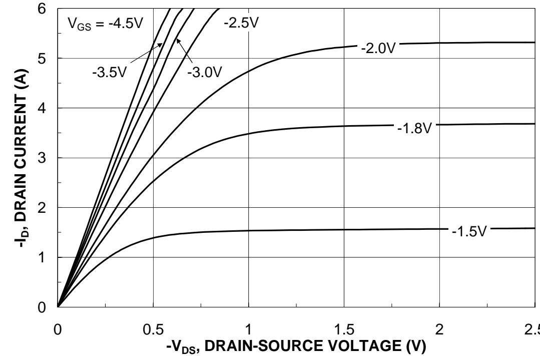



**Figure 1. On-Region Characteristics.**

**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

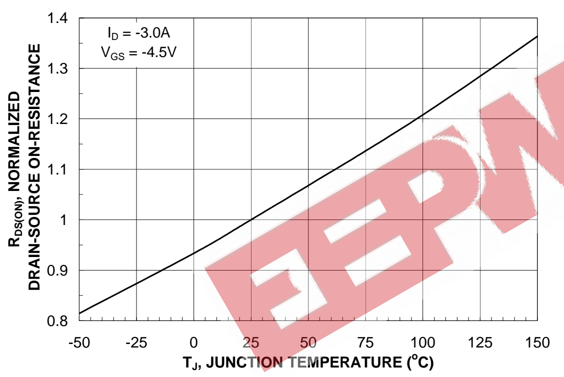



**Figure 3. On-Resistance Variation with Temperature.**

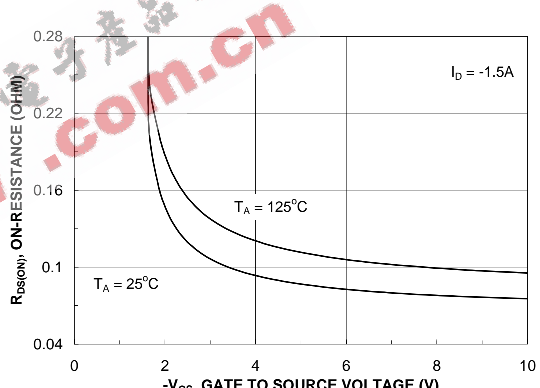



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

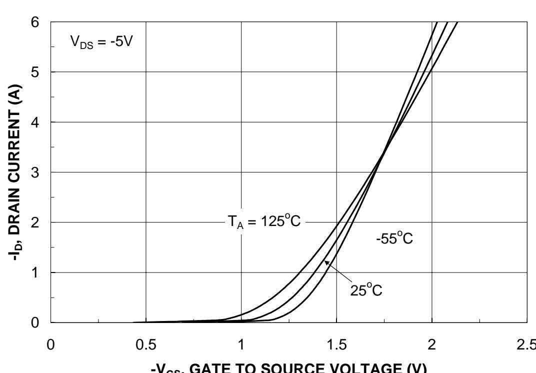



**Figure 5. Transfer Characteristics.**

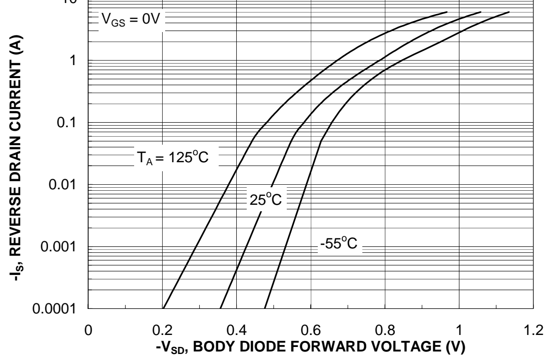



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

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## Typical Characteristics

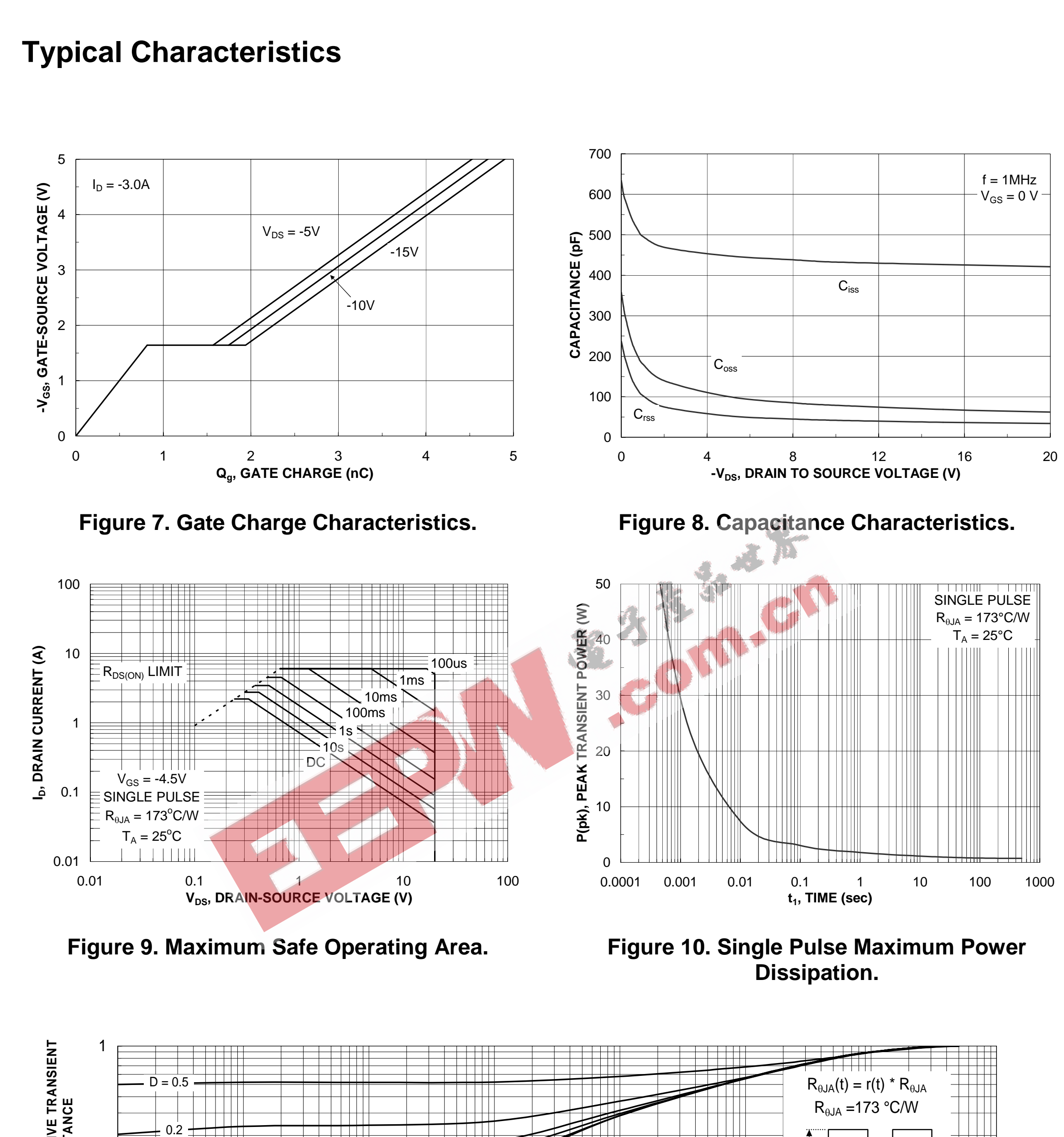



Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.

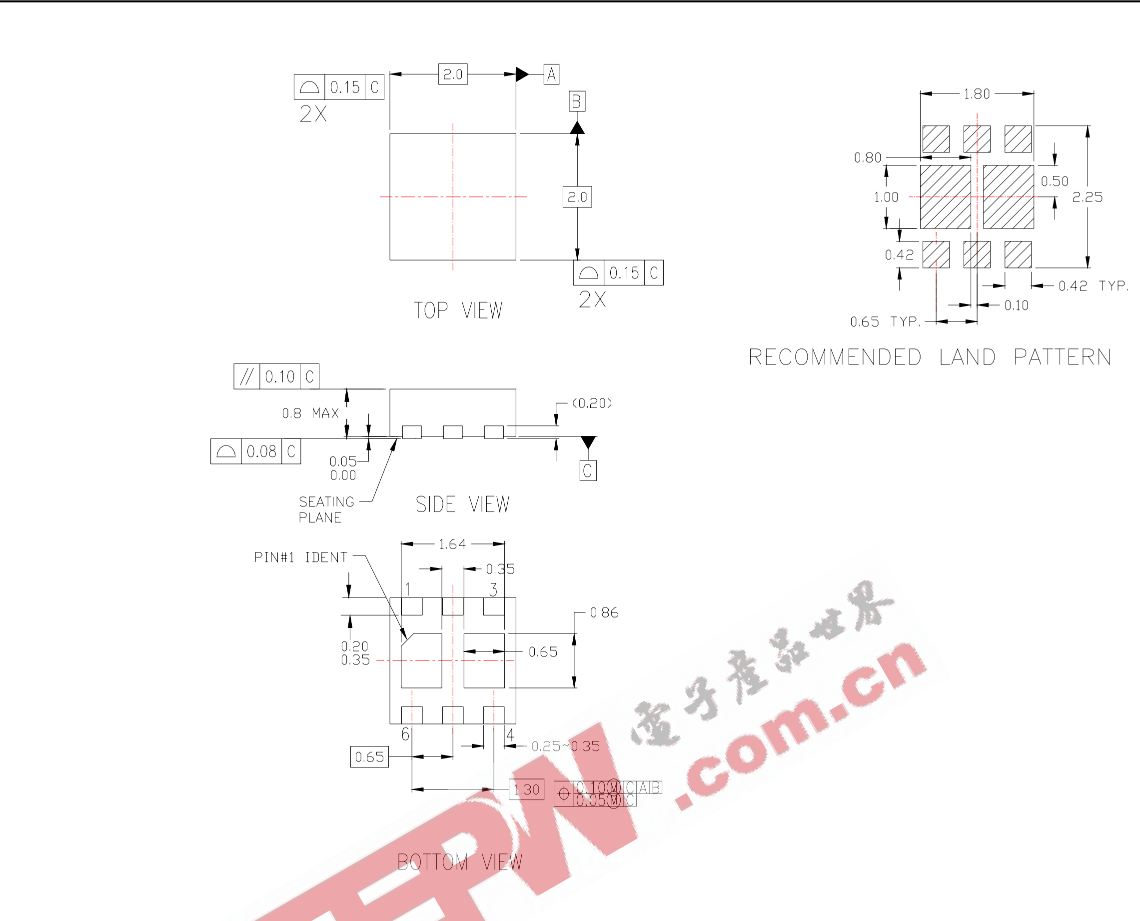
Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.



Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC, DATED 11/2001

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP06JrevB