

FDD5690

60V N-Channel PowerTrench™ MOSFET

General Description

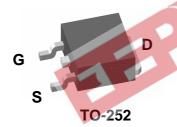
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

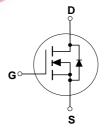
These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{\scriptscriptstyle DS(ON)}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 30 A, 60 V. $R_{DS(ON)} = 0.027\Omega$ @ $V_{GS} = 10$ V $R_{DS(ON)} = 0.032~\Omega$ @ $V_{GS} = 6$ V.
- Low gate charge (23nC typical).
- · Fast switching speed.
- High performance trench technology for extremely low $R_{\text{DS/OND}}$.





Absolute Maximum Ratings Tc=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	60	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Maximum Drain Current -Continuous (Note 1)	30	Α
	(Note 1a)	9	1
	Maximum Drain Current -Pulsed	100	1
P _D	Maximum Power Dissipation @ $T_C = 25^{\circ}C$ (Note 1)	50	W
	$T_A = 25^{\circ}C$ (Note 1a)	3.2	1
	$T_A = 25^{\circ}C$ (Note 1b)	1.3	
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _e JC	Thermal Resistance, Junction-to- Case	(Note 1)	2.5	°C/W
R _e JA	Thermal Resistance, Junction-to- Ambient	(Note 1a)	40	°C/W
		(Note 1b)	96	°C/W

Package Marking and Ordering Information

FDD5690 FDD5690 13" 16mm 2500	Device Marking	Device	Reel Size	Tape width	Quantity
	FDD5690	FDD5690		16mm	2500

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 30 V, I _D = 30 A			90	mJ
I _{AR}	Maximum Drain-Source Avalanche	Current			30	Α
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C		57		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V			1	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20V, V_{DS} = 0 V$			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
On Chara	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2	2.5	4	V
$\Delta V_{GS(th)} \ \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μ A,Referenced to 25°C	1	-6		mV/°(
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 9 A V _{GS} = 10 V, I _D = 9 A, T _J = 125°C V _{GS} = 6 V, I _D = 8 A	CI	0.023 0.032 0.026	0.027 0.048 0.032	Ω
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	25			Α
g FS	Forward Transconductance	V _{DS} = 5 V, I _D = 9 A		24		S
Dynamic	Characteristics					
Ciss	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}$		1110		pF
Coss	Output Capacitance	f = 1.0 MHz		150		pF
C _{rss}	Reverse Transfer Capacitance			75		pF
Switchin	g Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_{D} = 1 \text{ A}$		10	18	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		9	18	ns
t _{d(off)}	Turn-Off Delay Time			24	39	ns
t _f	Turn-Off Fall Time			10	18	ns
Qg	Total Gate Charge	V _{DS} = 30 V, I _D = 9 A		23	32	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V,		4		nC
Q_{gd}	Gate-Drain Charge			6.8		nC
Drain-So	urce Diode Characteristics					
Is	Maximum Continuous Drain-Source	e Diode Forward Current			2.3	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2.3 \text{ A}$ (Note 2)		0.75	1.2	V

^{1.} $R_{\theta,UC}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. $R_{\theta,UC}$ is guaranteed by design while $R_{\theta,CA}$ is determined by the user's board design.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300~\mu s,~Duty~Cycle \leq 2.0\%$

Typical Characteristics

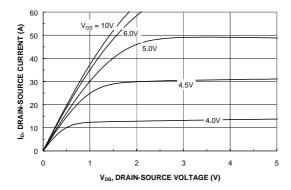


Figure 1. On-Region Characteristics.

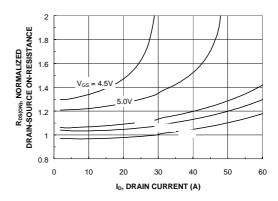


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

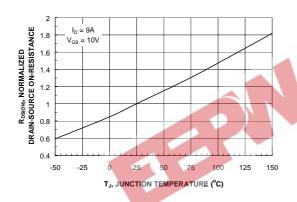


Figure 3. On-Resistance Variation with Temperature.

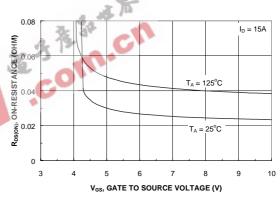


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

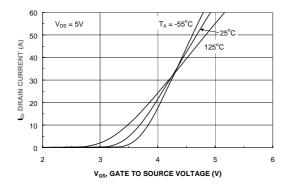


Figure 5. Transfer Characteristics.

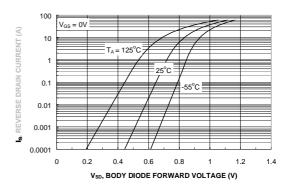
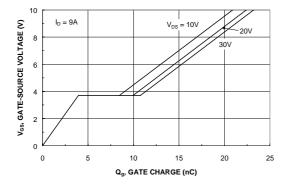


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)



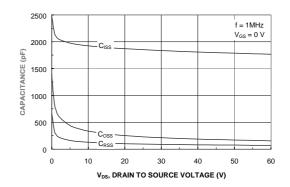
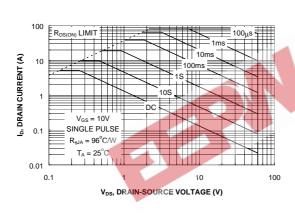


Figure 7. Gate-Charge Characteristics.

Figure 8. Capacitance Characteristics.



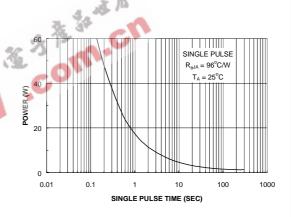


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

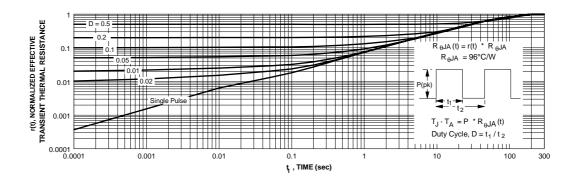
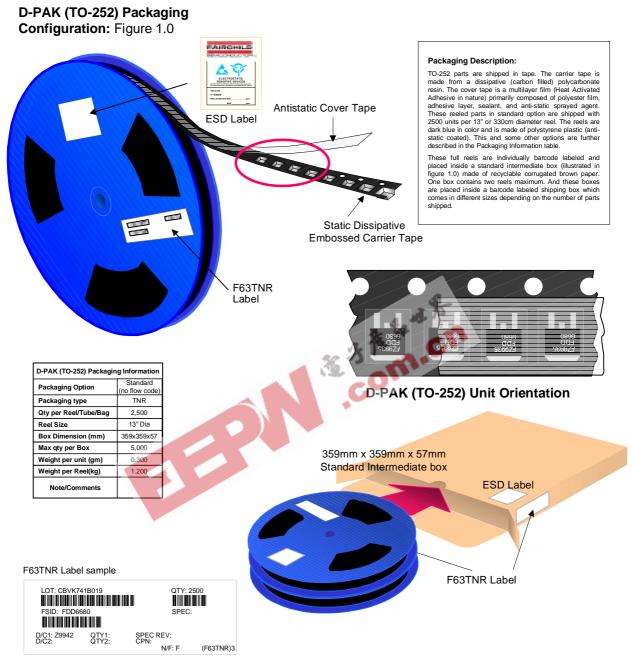
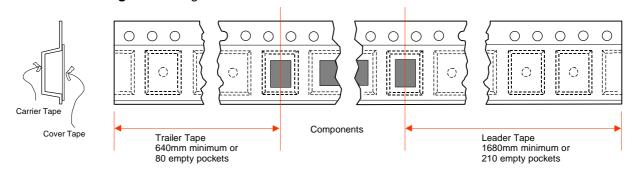


Figure 11. Transient Thermal Response Curve.

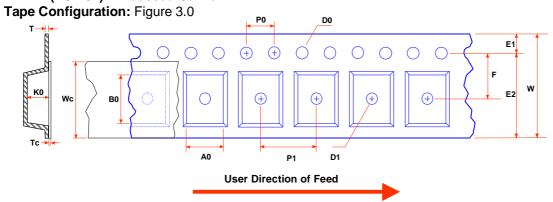
Thermal characterization performed using the conditions described in Note 1b. Transient themal response will change depending on the circuit board design.



TO-252 (D-PAK) Tape Leader and Trailer Configuration: Figure 2.0

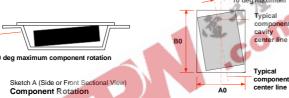


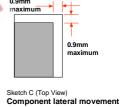




Dimensions are in millimeter														
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
TO252 (24mm)	6.90 +/-0.10	10.50 +/-0.10	16.0 +/-0.3	1.55 +/-0.05	1.5 +/-0.10	1.75 +/-0.10	14.25 min	7.50 +/-0.10	8.0 +/-0.1	4 .0 +/-0.1	2.65 +/-0.10	0.30 +/-0.05	13.0 +/-0.3	0.06 +/-0.02

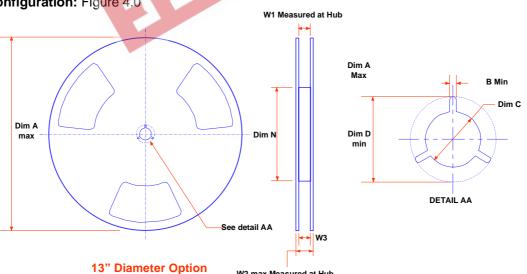
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).





Sketch B (Top View)
Component Rotation

D-PAK (TO-252) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters											
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)		
164mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.646 +0.078/-0.000 16.4 +2/0	0.882 22.4	0.626 – 0.764 15.9 – 19.4		

W2 max Measured at Hub

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