

## FDS6982

### Dual N-Channel, Notebook Power Supply MOSFET

#### General Description

This part is designed to replace two single SO-8 MOSFETs in synchronous DC:DC power supplies that provide the various peripheral voltage rails required in notebook computers and other battery powered electronic devices. FDS6982 contains two unique 30V, N-channel, logic level, PowerTrench™ MOSFETs designed to maximize power conversion efficiency.

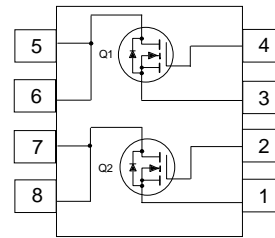
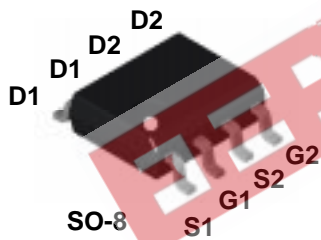
The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized for low conduction (less than 20mΩ at  $V_{GS} = 4.5V$ ).

#### Applications

- Battery powered synchronous DC:DC converters.
- Embedded DC:DC conversion.

#### Features

- Q2: 8.6A, 30V.  $R_{DS(on)} = 0.015 \Omega @ V_{GS} = 10V$   
 $R_{DS(on)} = 0.020 \Omega @ V_{GS} = 4.5V$
- Q1: 6.3A, 30V.  $R_{DS(on)} = 0.028 \Omega @ V_{GS} = 10V$   
 $R_{DS(on)} = 0.035 \Omega @ V_{GS} = 4.5V$
- Fast switching speed.
- Low gate charge (Q1 typical = 8.5nC).
- High performance trench technology for extremely low  $R_{DS(on)}$ .



#### Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Q2	Q1	Units
$V_{DSS}$	Drain-Source Voltage	30	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	8.6	6.3	A
	- Pulsed	30	20	
$P_D$	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ C$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ C/W$

#### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS6982	FDS6982	13"	12mm	2500 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q2 Q1		27 26		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	All			1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	Q2 Q1	1 1	2.2 1.6	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q2 Q1		-5 -4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.6\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 8.6\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 5.6\text{ A}$	Q2 Q1		0.012 0.018 0.016 0.021 0.038 0.028	0.015 0.024 0.020 0.028 0.047 0.035	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	Q2 Q1	30 20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 8.6\text{ A}$ $V_{DS} = 5\text{ V}, I_D = 6.3\text{ A}$	Q2 Q1		50 40		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	Q2 Q1		2085 760		pF
$C_{oss}$	Output Capacitance		Q2 Q1		420 160		pF
$C_{riss}$	Reverse Transfer Capacitance		Q2 Q1		160 70		pF

**Electrical Characteristics (continued)**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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**Switching Characteristics** (Note 2)

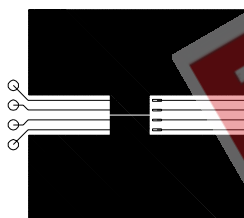
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	Q2		15	27	ns
			Q1		10	18	
$t_r$	Turn-On Rise Time		Q2		11	20	ns
			Q1		14	25	
$t_{d(off)}$	Turn-Off Delay Time		Q2		36	58	ns
			Q1		21	34	
$t_f$	Turn-Off Fall Time	Q2		18	29	ns	
		Q1		7	14		
$Q_g$	Total Gate Charge	Q2		18.5	26	nC	
		Q1		8.5	12		
$Q_{gs}$	Gate-Source Charge	Q2		7.3		nC	
		Q1		2.4			
$Q_{gd}$	Gate-Drain Charge	Q2		6.2		nC	
		Q1		3.1			

**Drain-Source Diode Characteristics and Maximum Ratings**

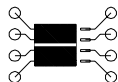
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		Q2		1.3	A
			Q1		1.3	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q2		0.72	V
		$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q1		0.74	

**Notes:**

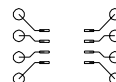
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a) 78° C/W when mounted on a 0.5 in<sup>2</sup> pad of 2 oz. copper.



b) 125° C/W when mounted on a 0.02 in<sup>2</sup> pad of 2 oz. copper.



c) 135° C/W when mounted on a 0.003 in<sup>2</sup> pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

### Typical Characteristics: Q2

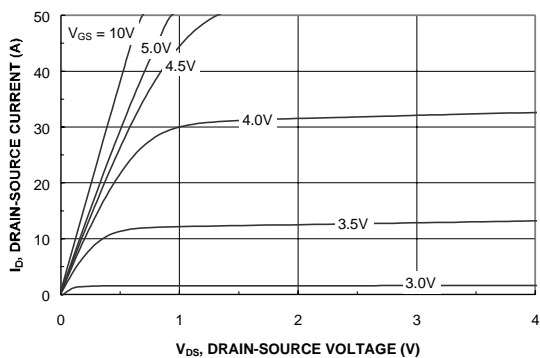


Figure 1. On-Region Characteristics.

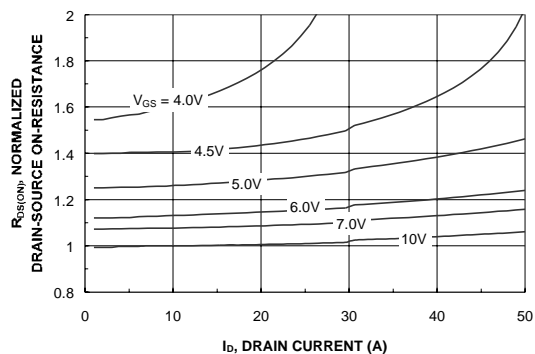


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

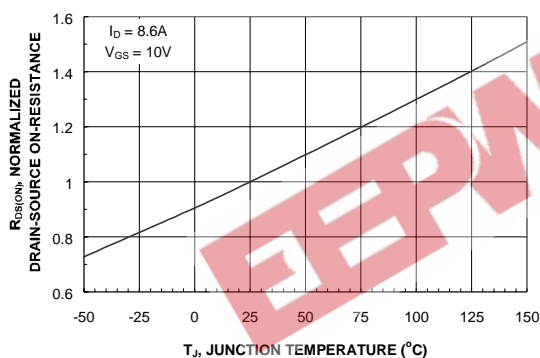


Figure 3. On-Resistance Variation with Temperature.

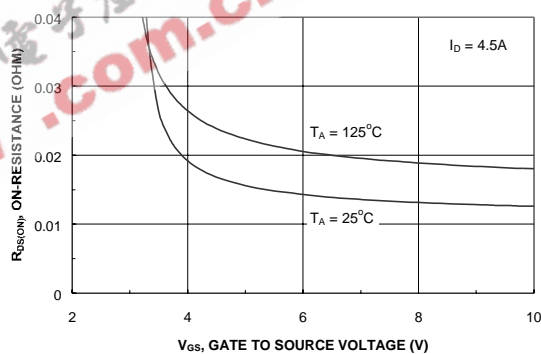


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

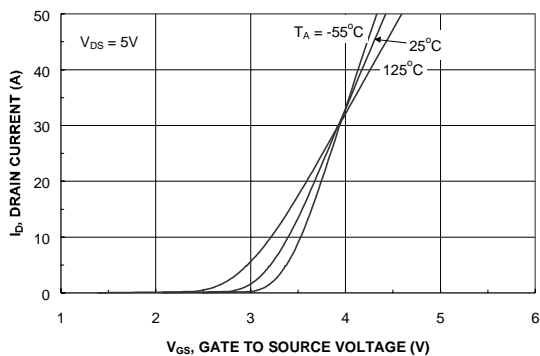


Figure 5. Transfer Characteristics.

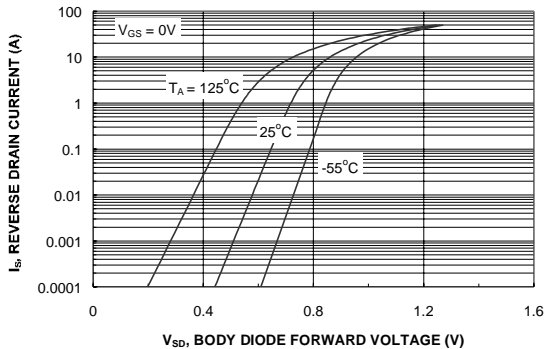


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (continued)

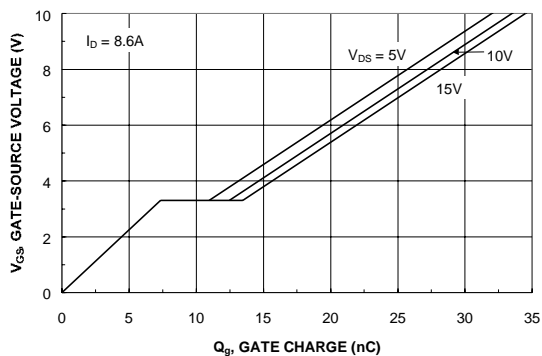


Figure 7. Gate-Charge Characteristics.

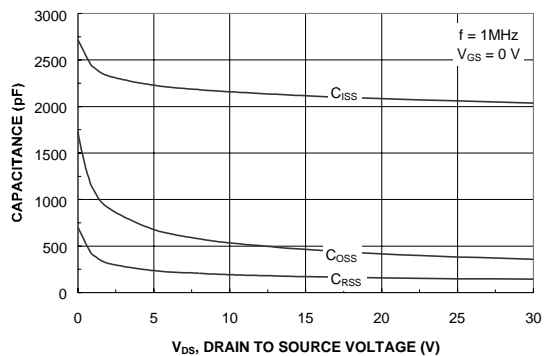


Figure 8. Capacitance Characteristics.

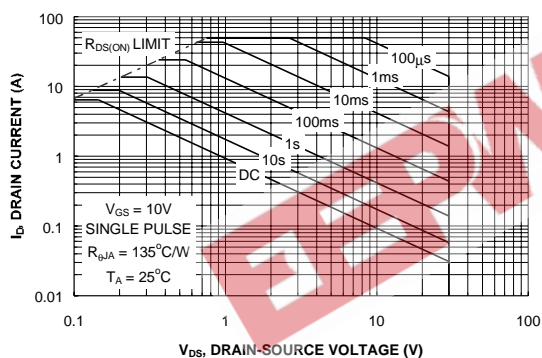


Figure 9. Maximum Safe Operating Area.

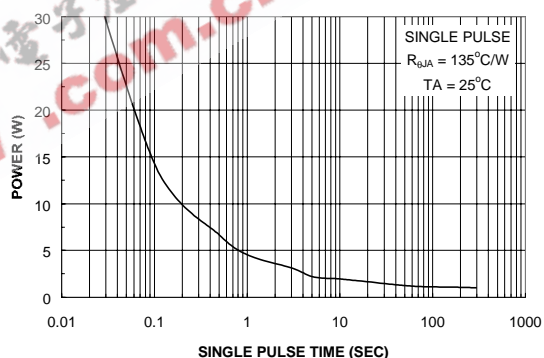


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1

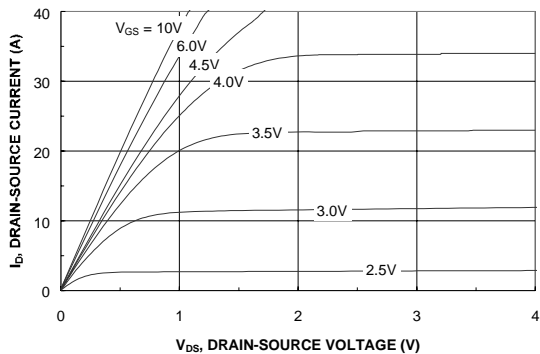


Figure 11. On-Region Characteristics.

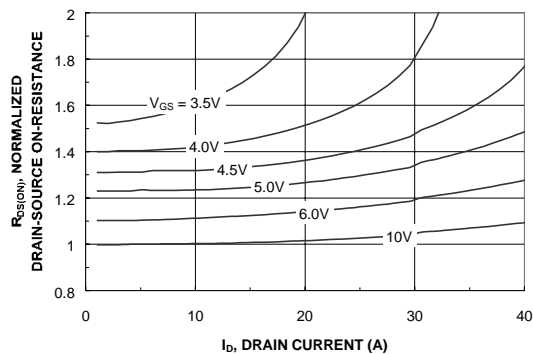


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

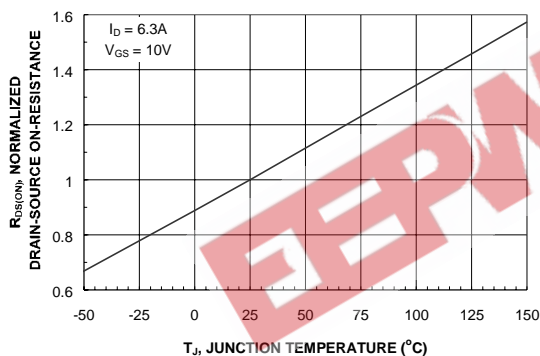


Figure 13. On-Resistance Variation with Temperature.

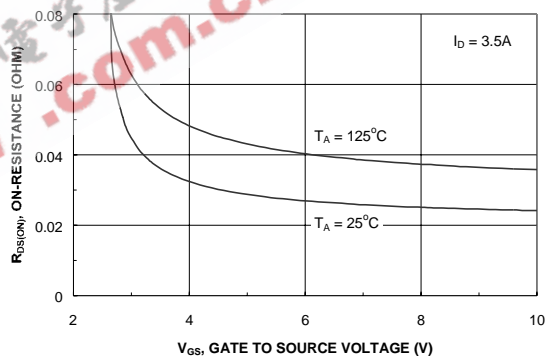


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

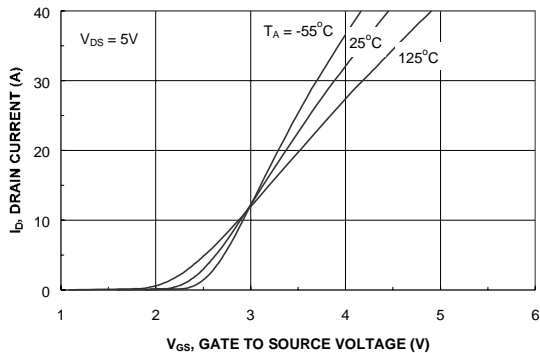


Figure 15. Transfer Characteristics.

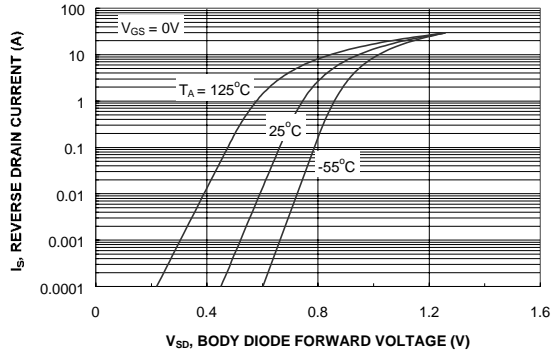


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1 (continued)

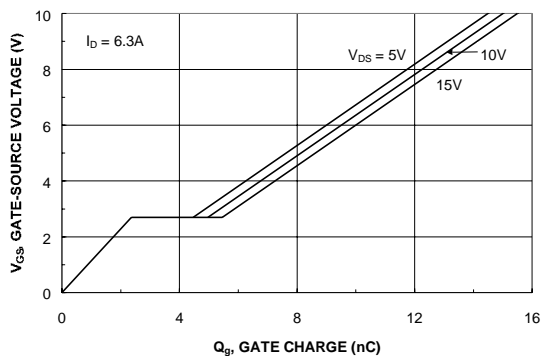


Figure 17. Gate-Charge Characteristics.

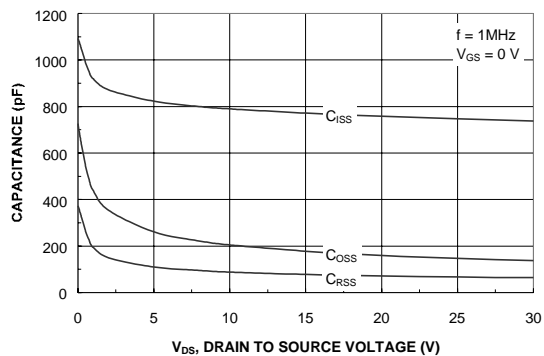


Figure 18. Capacitance Characteristics.

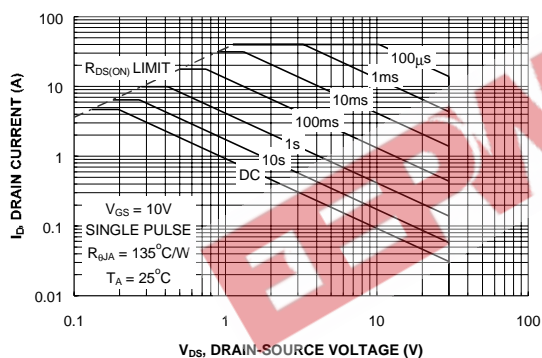


Figure 19. Maximum Safe Operating Area.

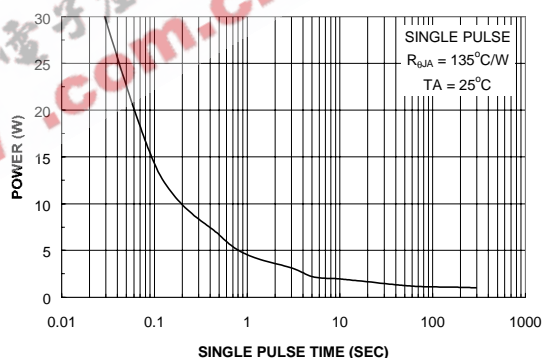


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1 & Q2 (continued)

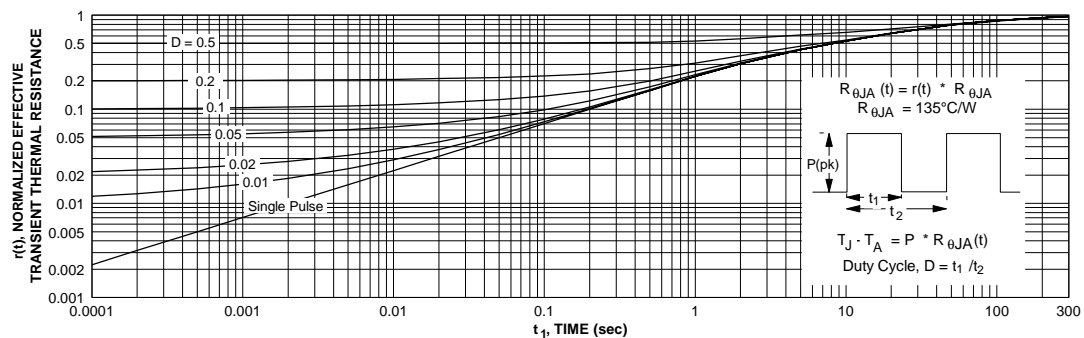


Figure 21. Transient Thermal Response Curve.

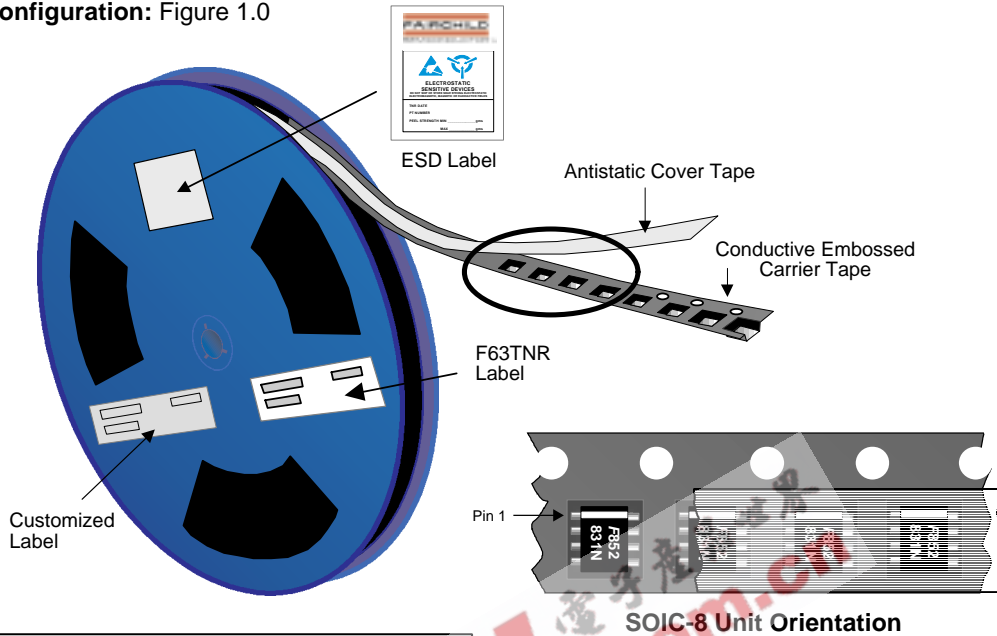
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# SO-8 Tape and Reel Data and Package Dimensions



## SOIC(8lds) Packaging Configuration: Figure 1.0

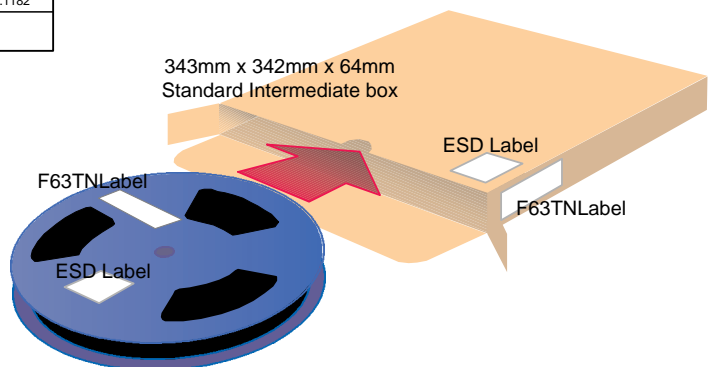


SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	S62Z	D84Z
Packaging type	TNR	Rail/Tube	Bag	TNR
Qty per Reel/Tube/Bag	2,500	95	200	500
Reel Size	13" Dia	-	-	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	76x102x127	184x187x47
Max qty per Box	5,000	30,000	1,000	2,500
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	-	0.1182
Note/Comments			Bulk	

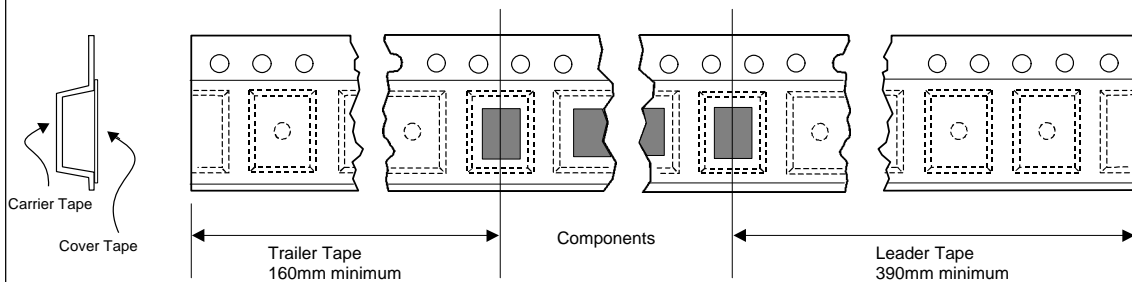
## SOIC-8 Unit Orientation

### F63TNR Label sample

LOT: CBVK741B019		QTY: 2500	
FSID: FDS9953A		SPEC:	
D/C1: D9842	QTY1:	SPEC REV:	QARV:
D/C2:	QTY2:	CPN:	(F63TNR)2

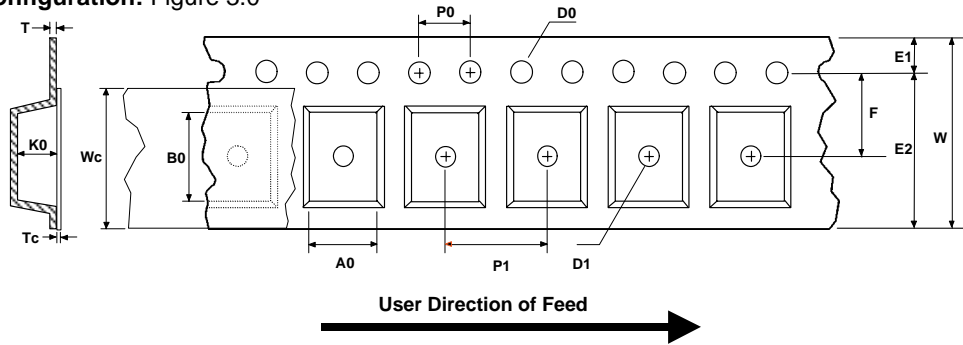


## SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



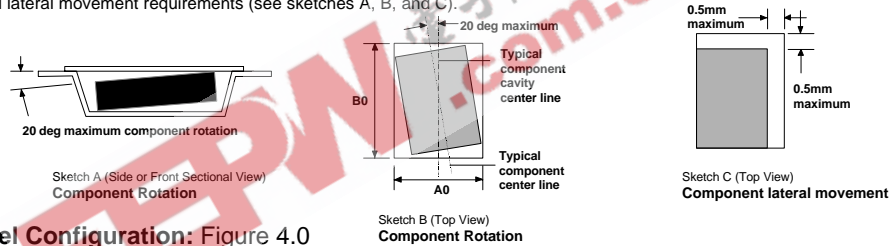
## SO-8 Tape and Reel Data and Package Dimensions, continued

### SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0

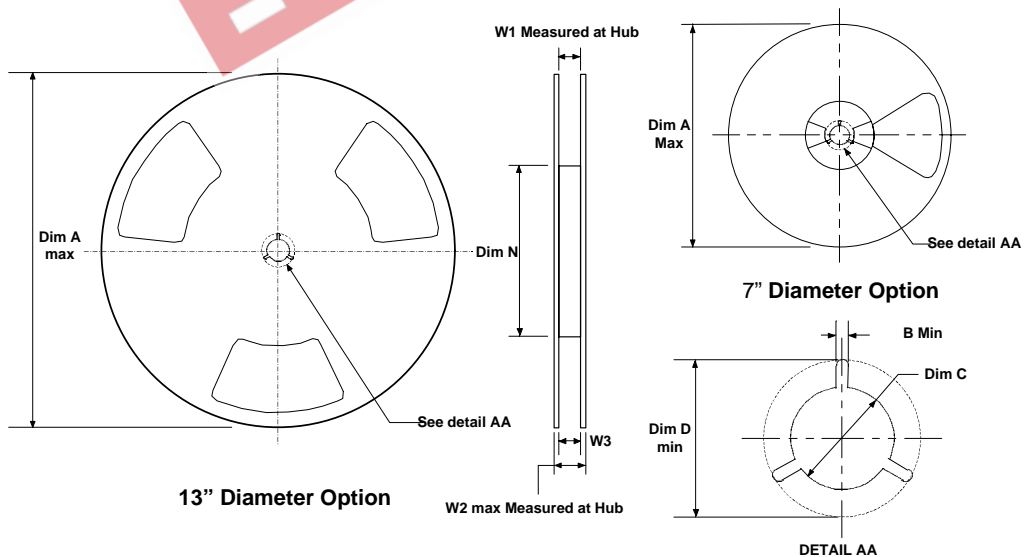


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 ±0.10	5.30 ±0.10	12.0 ±0.3	1.55 ±0.05	1.60 ±0.10	1.75 ±0.10	10.25 min	5.50 ±0.05	8.0 ±0.1	4.0 ±0.1	2.1 ±0.10	0.450 ±/- 0.150	9.2 ±0.3	0.06 ±0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



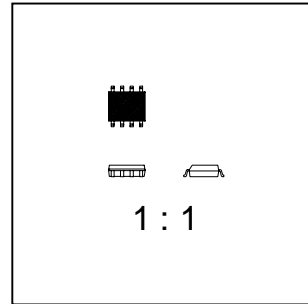
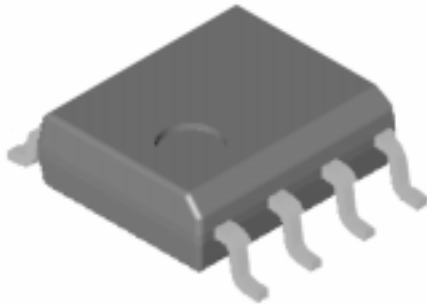
### SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

# SO-8 Tape and Reel Data and Package Dimensions, continued

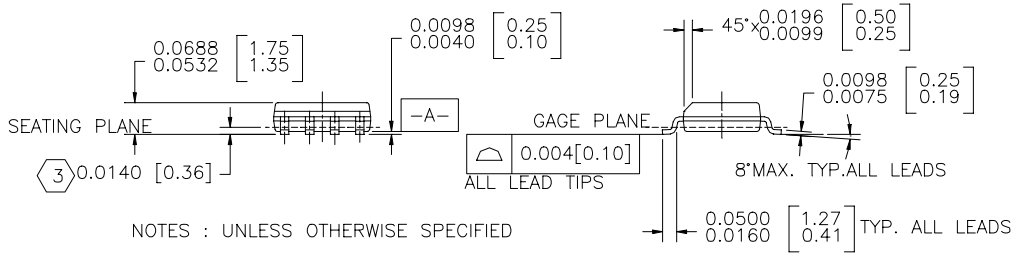
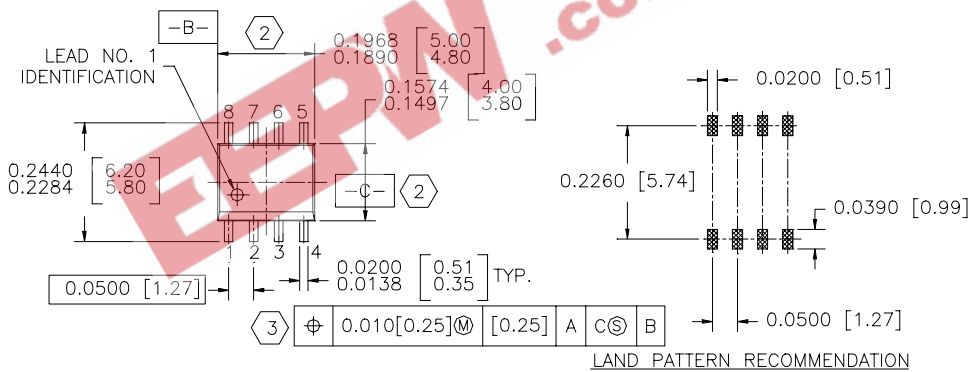
## SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:  
inches [millimeters]

Part Weight per unit (gram): 0.0774



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:  
200 MICROINCHES / 5.08 MICRONS MINIMUM  
LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

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E <sup>2</sup> CMOS™	PowerTrench™	
FACT™	QS™	
FACT Quiet Series™	Quiet Series™	
FAST®	SuperSOT™-3	
FASTr™	SuperSOT™-6	
GTO™	SuperSOT™-8	
HiSeC™	TinyLogic™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.