

FDFM2P110

Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

General Description

FDFM2P110 combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in a MicroFET package.

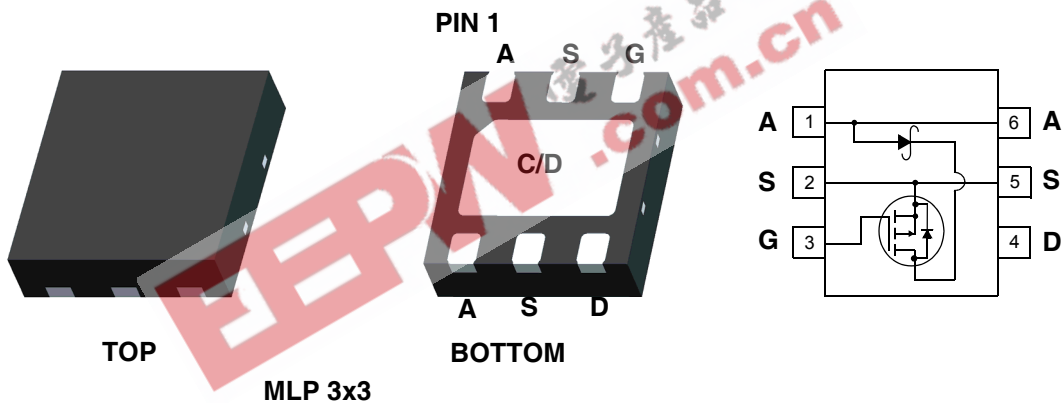
This device is designed specifically as a single package solution for Buck Boost. It features a fast switching, low gate charge MOSFET with very low on-state resistance.

Applications

- Buck Boost

Features

- -3.5 A, -20 V $R_{DS(ON)} = 140m\Omega @ V_{GS} = -4.5 V$
 $R_{DS(ON)} = 200m\Omega @ V_{GS} = -2.5 V$
- Low Profile - 0.8 mm maximum - in the new package MicroFET 3x3 mm



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current -Continuous (Note 1a)	-3.5	A
	-Pulsed	-10	
V_{RRM}	Schottky Repetitive Peak Reverse voltage	20	V
I_O	Schottky Average Forward Current (Note 1a)	2	A
P_D	Power dissipation (Steady State) (Note 1a) (Note 1b)	2	W
		0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	60	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	145	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
2P110	FDFM2P110	7inch	12mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain-Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-20	-	-	V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, Referenced to 25°C	-	-11	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{V}, V_{DS} = -16\text{V}$	-	-	-1	μA
I_{GSS}	Gate-Body Leakage,	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics (Note 2)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.6	-1.0	-1.5	V
$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, Referenced to 25°C	-	3	-	mV/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$I_D = -3.5\text{A}, V_{GS} = -4.5\text{V}$	-	101	140	m Ω
		$I_D = -3.0\text{A}, V_{GS} = -2.5\text{V}$	-	145	200	
		$I_D = -3.5\text{A}, V_{GS} = -4.5\text{V}$, $T_J = 125^\circ\text{C}$	-	136	202	
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = -2.5\text{V}, V_{DS} = -5\text{V}$	-10	-	-	A
g_{FS}	Forward Transconductance	$I_D = -3.5\text{A}, V_{DS} = -5\text{V}$	-	6	-	S

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	280	-	pF
C_{OSS}	Output Capacitance		-	65	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	35	-	pF
R_G	Gate Resistance		$f = 1\text{MHz}$	-	7	-

Switching Characteristics (Note 2)

$t_{d(ON)}$	Turn-On Delay Time	$V_{DD} = -10\text{V}, I_D = -1\text{A}$ $V_{GS} = -4.5\text{V}, R_{GEN} = 16\Omega$	-	8	16	ns
t_r	Turn-On Rise Time		-	12	22	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	11	20	ns
t_f	Turn-Off Fall Time		-	3.2	6.4	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{V}, I_D = -3.5\text{A}$, $V_{GS} = -4.5\text{V}$	-	3	4	nC
Q_{gs}	Gate-Source Charge		-	0.7	-	nC
Q_{gd}	Gate-Drain Charge		-	1	-	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	-2	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -2\text{A}$ (Note 2)	-	-0.9	-1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -3.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	-	13	-	ns
Q_{rr}	Diode Reverse Recovery Charge		-	3	-	nC

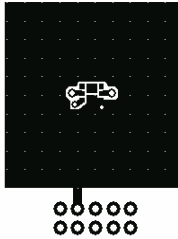
Schottky Diode Characteristic

V_R	Reverse Voltage	$I_R = 1\text{mA}$	20	-	-	V	
I_R	Reverse Leakage	$V_R = 5\text{V}$	$T_J = 25^\circ\text{C}$	-	-	100	μA
			$T_J = 100^\circ\text{C}$	-	-	10	mA
V_F	Forward Voltage	$I_F = 1\text{A}$	$T_J = 25^\circ\text{C}$	-	0.32	0.39	V

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta CA}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 60°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 145°C/W when mounted on a minimum pad of 2 oz copper

Scale 1: 1 on letter size paper

2. Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty Cycle $< 2.0\%$



Typical Characteristics

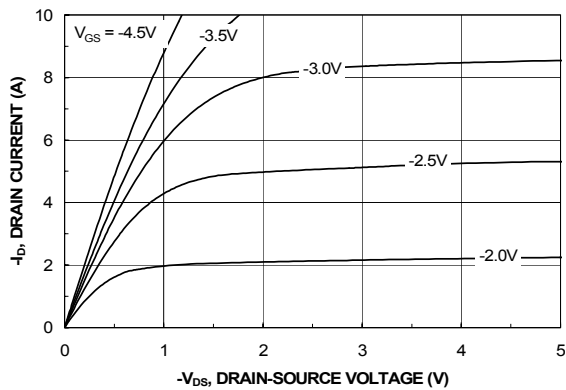


Figure 1. On-Region Characteristics

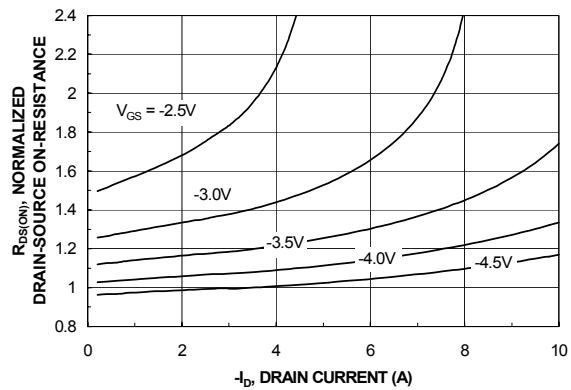


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

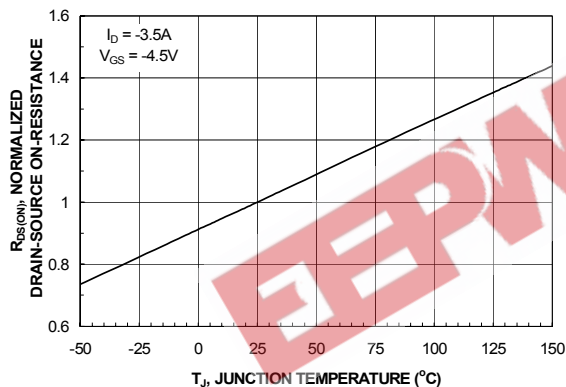


Figure 3. On-Resistance Variation with Temperature

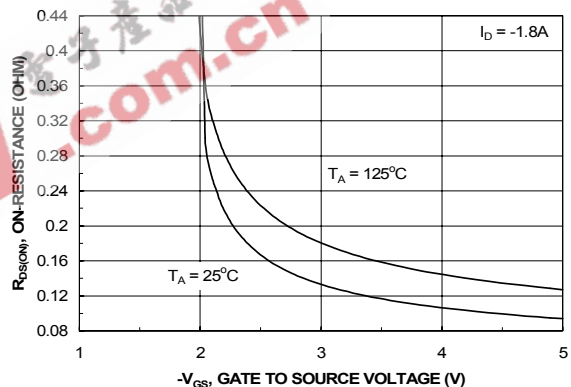


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

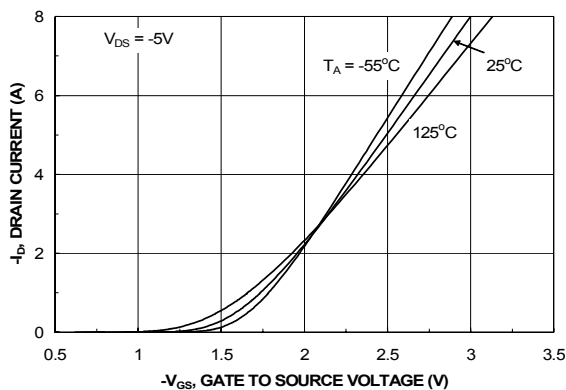


Figure 5. Transfer Characteristics

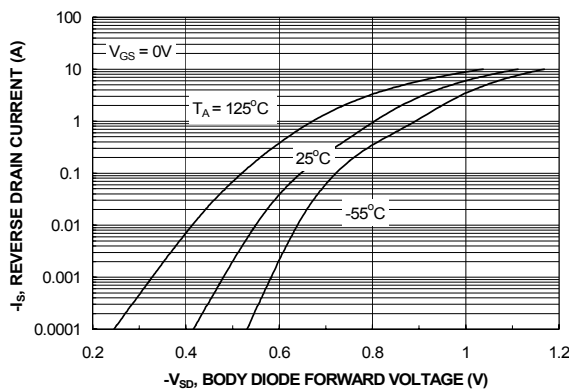


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

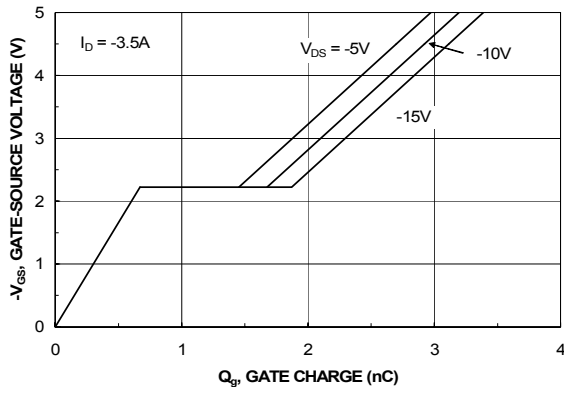


Figure 7. Gate Charge Characteristics

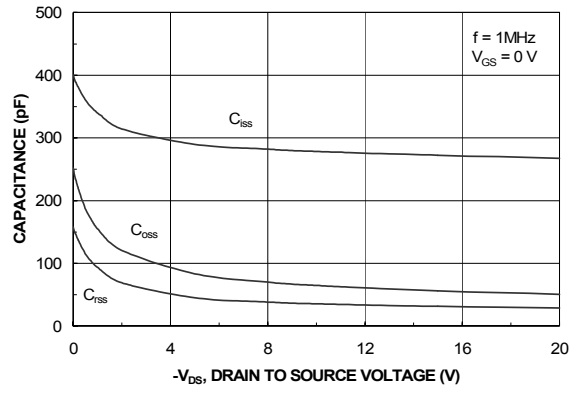


Figure 8. Capacitance Characteristics

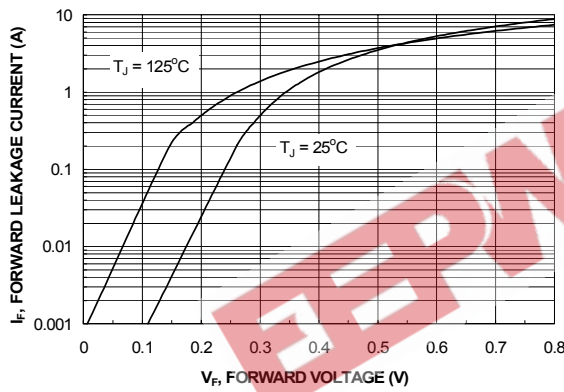


Figure 9. Schottky Diode Forward Voltage

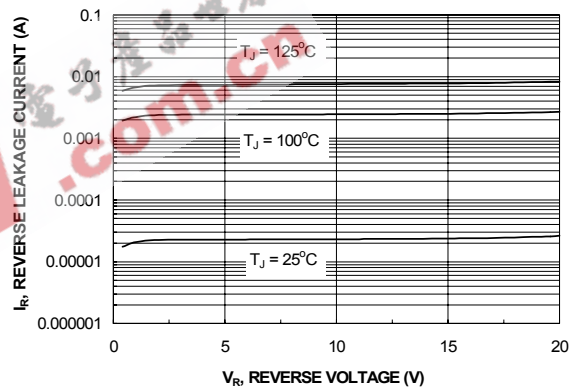


Figure 10. Schottky Diode Reverse Current

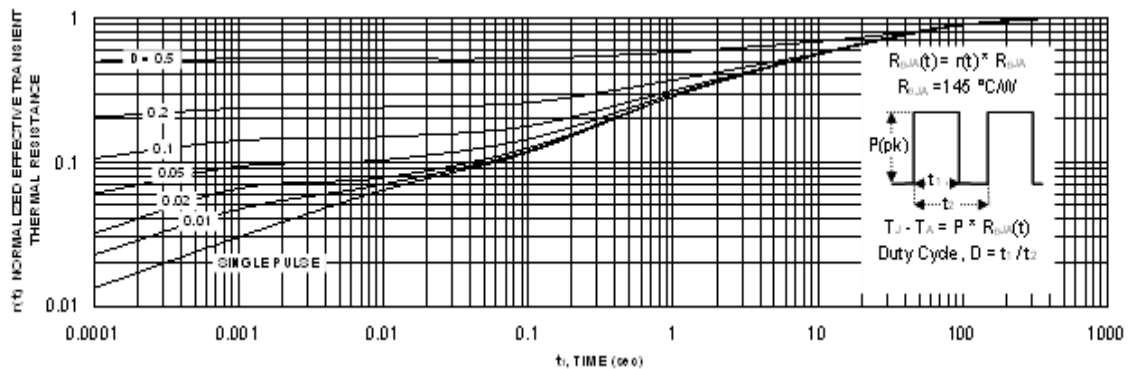
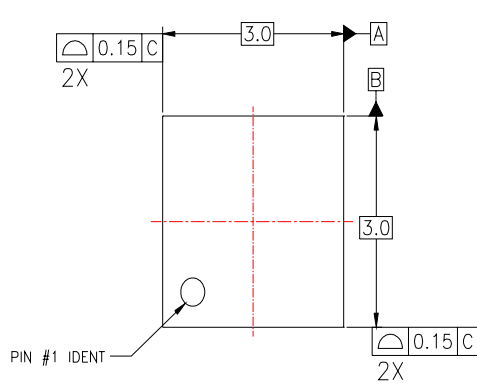
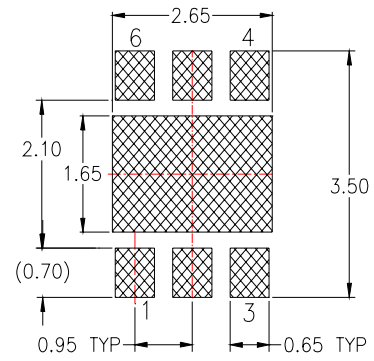


Figure 11. Transient Thermal Response Curve

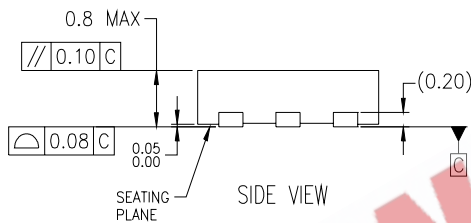
Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



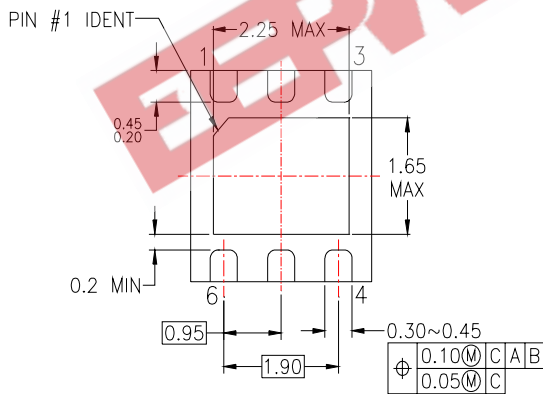
TOP VIEW



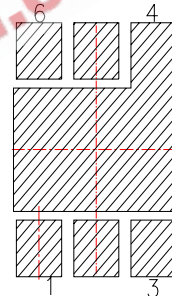
RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW



RECOMMENDED COPPER TRACE

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEEA, DATED 11/2001
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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Rev. 116