FAIRCHILD SEMICONDUCTOR TM

July 1998

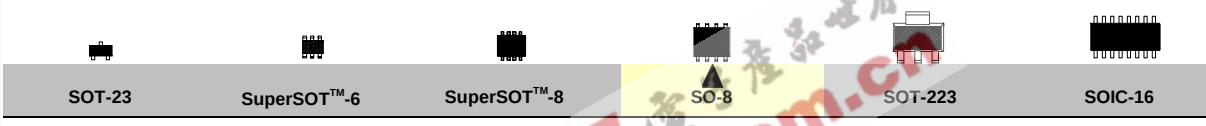
FDS8928A
Dual N & P-Channel Enhancement Mode Field Effect Transistor

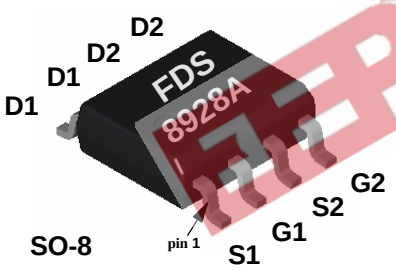
General Description

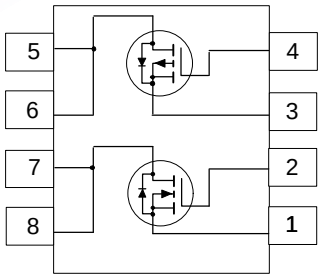
These dual N- and P -Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 5.5 A,30 V, $R_{DS(ON)}$=0.030 Ω @ V_{GS}=4.5 V
  $R_{DS(ON)}$=0.038 Ω @ V_{GS}=2.5 V.
  P-Channel -4 A,-20 V, $R_{DS(ON)}$=0.055 Ω @ V_{GS}=-4.5 V
  $R_{DS(ON)}$=0.072 Ω @ V_{GS}=-2.5 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.







Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-20	V
V_{GSS}	Gate-Source Voltage	8	-8	V
I_D	Drain Current - Continuous (Note 1a)	5.5	-4	A
	- Pulsed	20	-20	
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C	N-Ch		32		mV/°C
		I_D = -250 µA, Referenced to 25 °C	P-Ch		-23		
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.4	0.67	1	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-0.4	-0.6	-1	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C	N-Ch		-3		mV/°C
		I_D = -250 µA, Referenced to 25 °C	P-Ch		4		
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 5.5 A	N-Ch		0.025	0.03	Ω
		V_{GS} = 2.5 V, I_D = 4.5 A			0.031	0.038	
		V_{GS} = -4.5 V, I_D = -4 A	P-Ch		0.043	0.055	
		V_{GS} = -2.5 V, I_D = -3.4 A			0.059	0.072	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	N-Ch	20			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	P-Ch	-20			
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 5.5 A	N-Ch		20		S
		V_{DS} = -5 V, I_D = -4 A	P-Ch		13		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		900		pF
			P-Ch		1130		
C_{oss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		410		pF
			P-Ch		480		
C_{rss}	Reverse Transfer Capacitance		N-Ch		110		pF
			P-Ch		120		

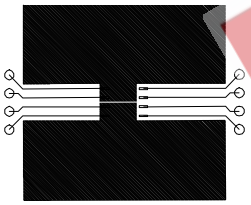
Electrical Characteristics (continued)

SWITCHING CHARACTERISTICS (Note 2)

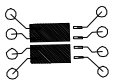
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
$t_{D(on)}$	Turn - On Delay Time	V_{DS} = 6 V, I_D = 1 A	N-Ch		6	12	ns
		V_{GS} = 4.5 V , R_{GEN} = 6 Ω	P-Ch		8	16	
t_r	Turn - On Rise Time		N-Ch		19	31	ns
			P-Ch		23	37	
$t_{D(off)}$	Turn - Off Delay Time	V_{DS}= -10 V, I_D= -1 A	N-Ch		42	67	ns
		V_{GS} = -4.5 V , R_{GEN} = 6 Ω	P-Ch		260	360	
t_f	Turn - Off Fall Time		N-Ch		13	24	ns
			P-Ch		90	125	
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 5.5 A,	N-Ch		19.8	28	nC
		V_{GS} = 4.5 V	P-Ch		20	28	
Q_{gs}	Gate-Source Charge		N-Ch		2		nC
		V_{DS} = -5 V, I_D = -4 A,	P-Ch		2.8		
Q_{gd}	Gate-Drain Charge	V_{GS} = -5 V	N-Ch		6.3		nC
			P-Ch		3.2		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.3	A
			P-Ch			-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)	N-Ch		0.68	1.2	V
		V_{GS} = 0 V, I_S = -1.3 A (Note 2)	P-Ch		-0.7	-1.2	V

Notes:

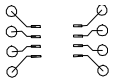
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%..

Typical Electrical Characteristics: N-Channel

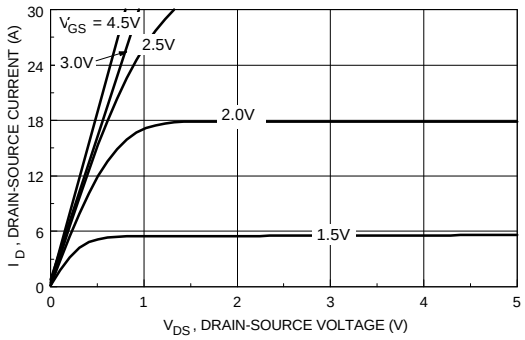


Figure 1. On-Region Characteristics.

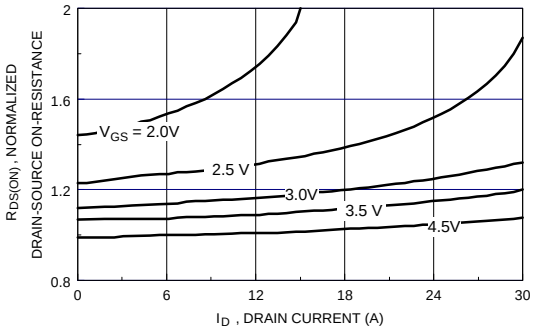


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

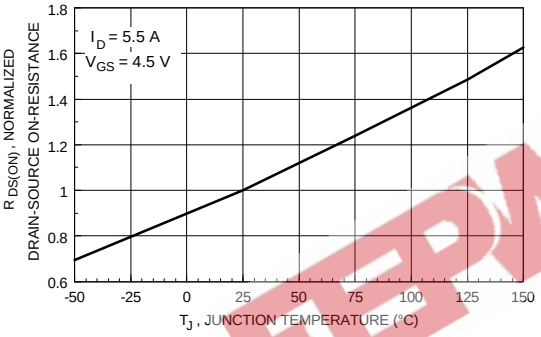


Figure 3. On-Resistance Variation with Temperature.

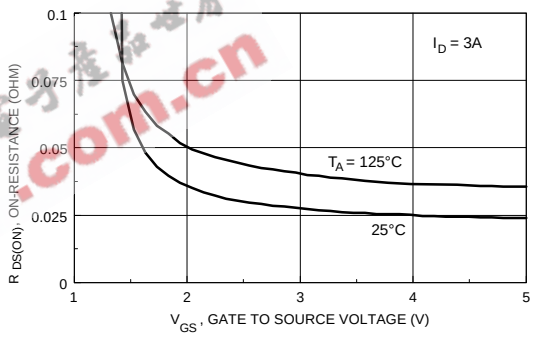


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

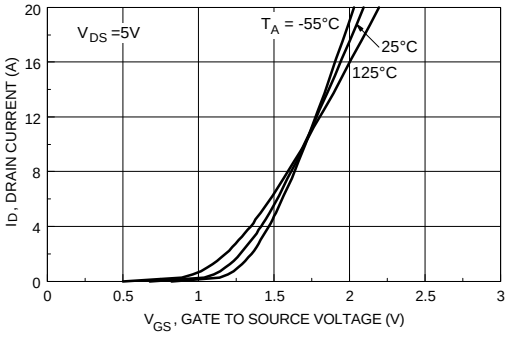


Figure 5. Transfer Characteristics.

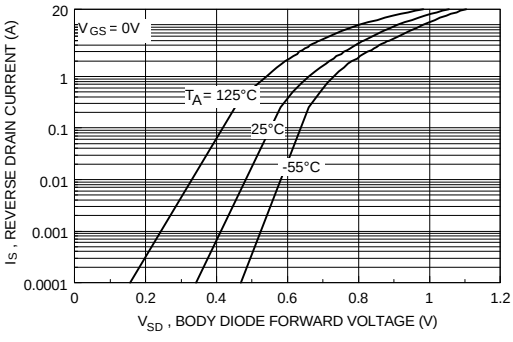


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: N-Channel (continued)

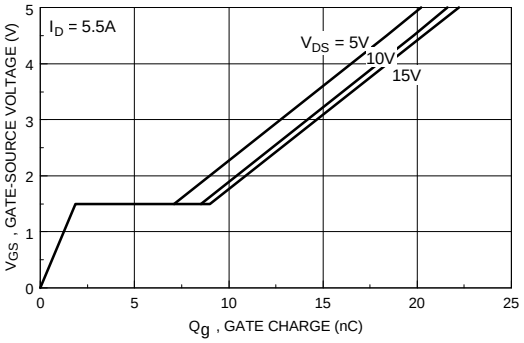


Figure 7. Gate Charge Characteristics.

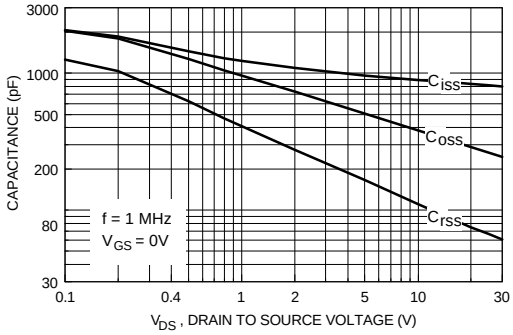


Figure 8. Capacitance Characteristics.

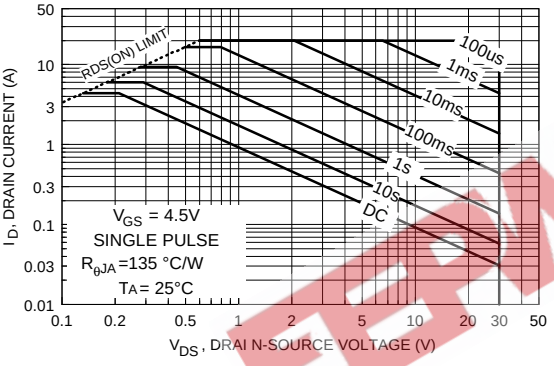


Figure 9. Maximum Safe Operating Area.

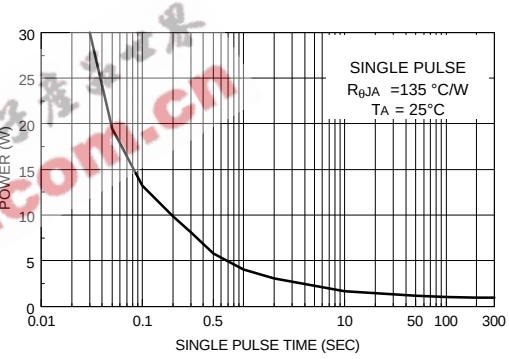


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Electrical Characteristics: P-Channel

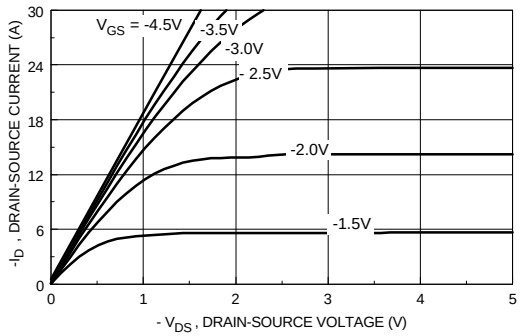


Figure 11. On-Region Characteristics.

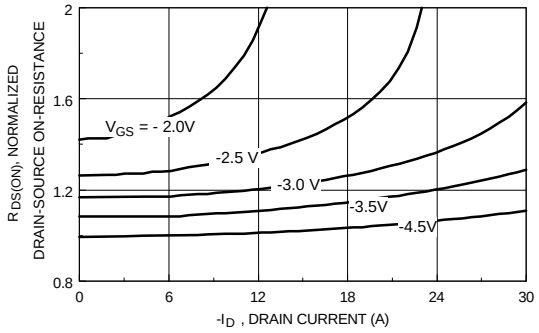


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

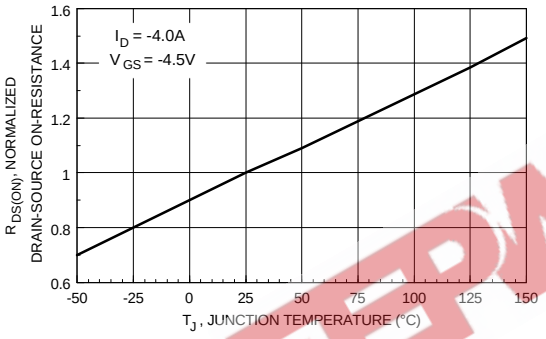


Figure 13. On-Resistance Variation with Temperature.

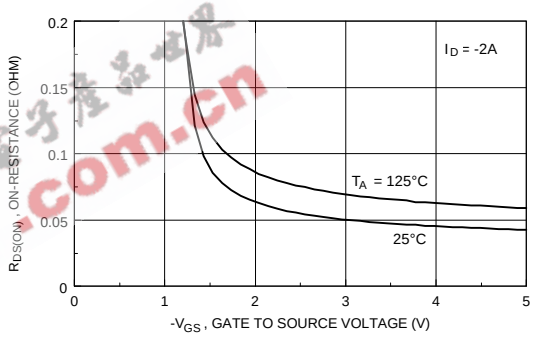


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

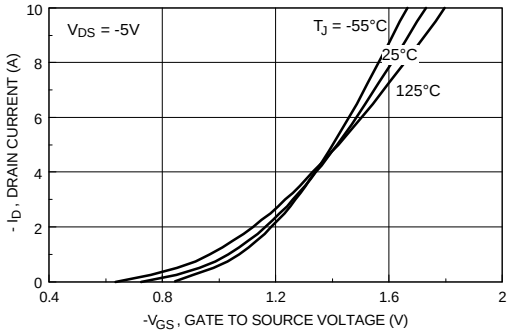


Figure 15. Transfer Characteristics.

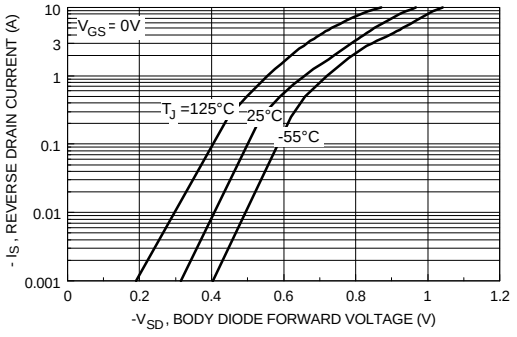


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

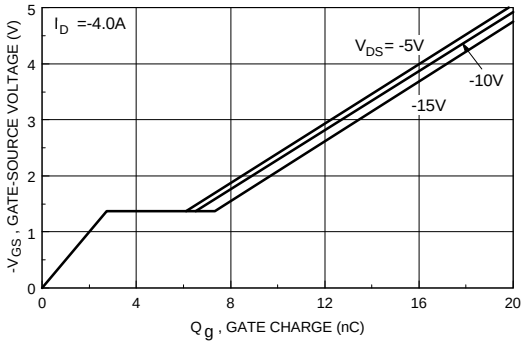


Figure 17. Gate Charge Characteristics.

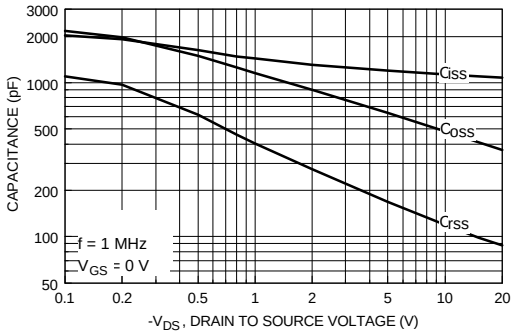


Figure 18. Capacitance Characteristics.

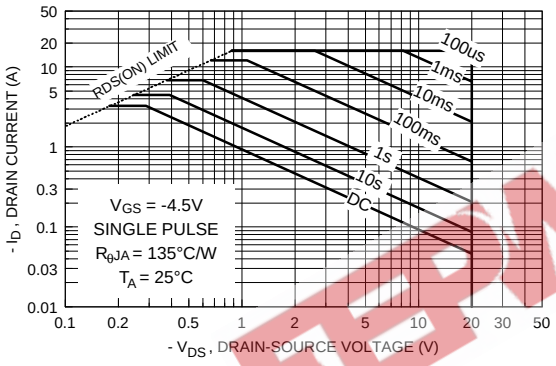


Figure 19. Maximum Safe Operating Area.

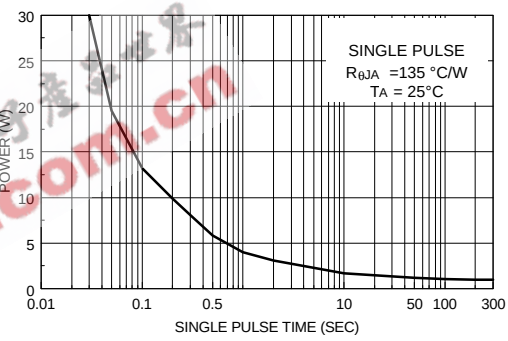


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Thermal Characteristics: N & P-Channel (continued)

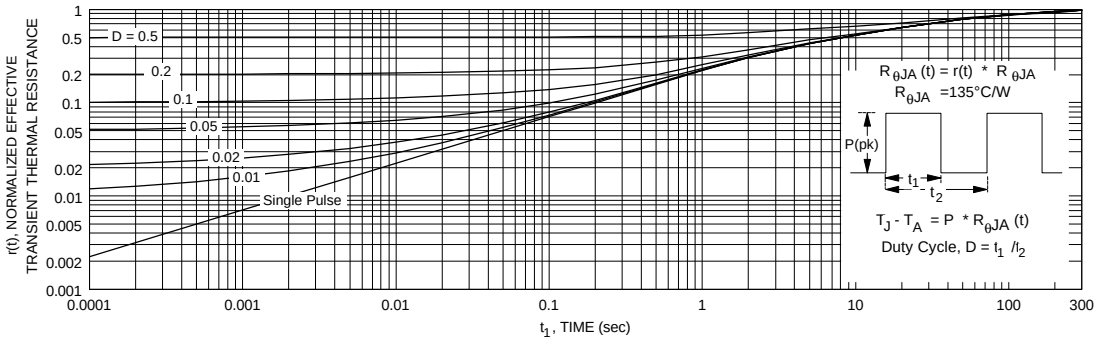


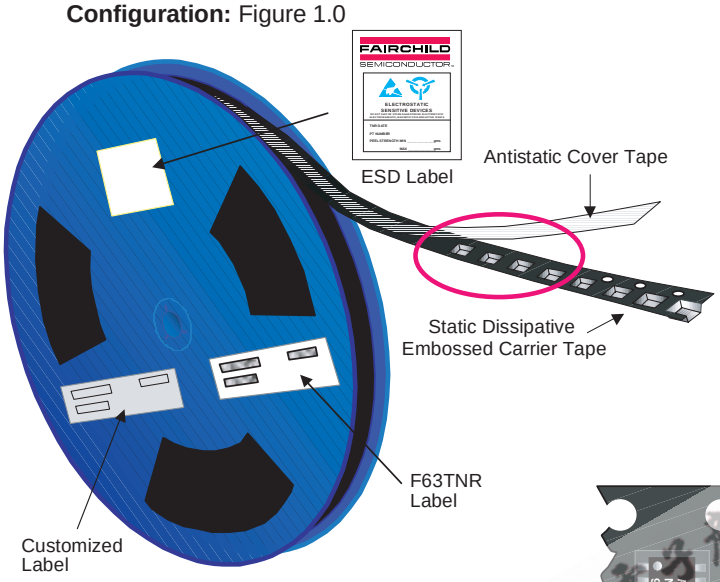
Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1.
Transient thermalresponse will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

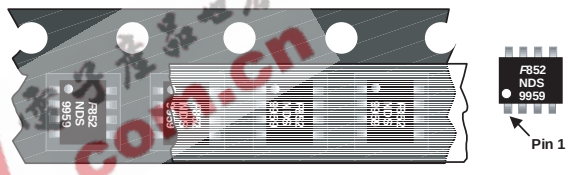
SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

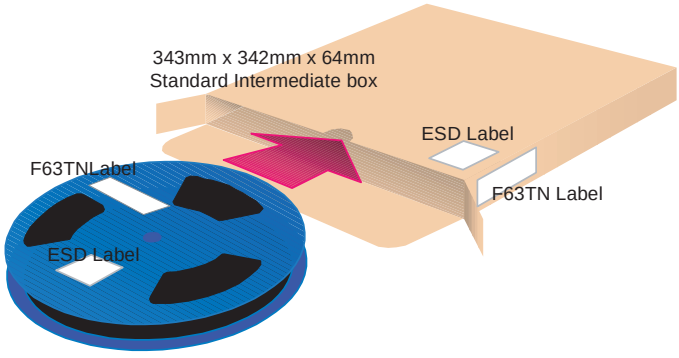
SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



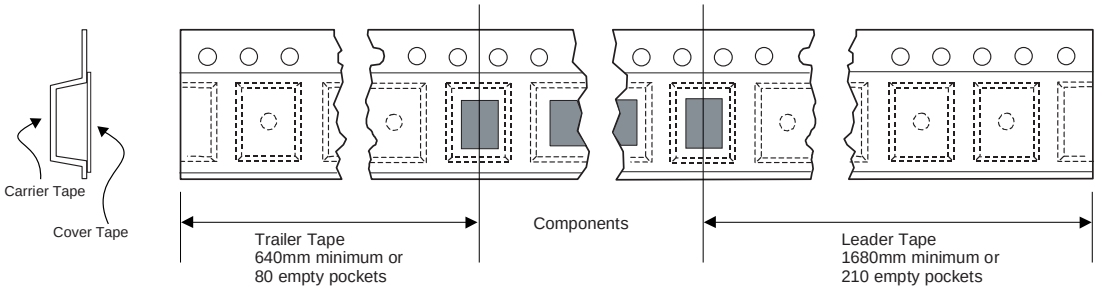
SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				



F63TNR Label sample

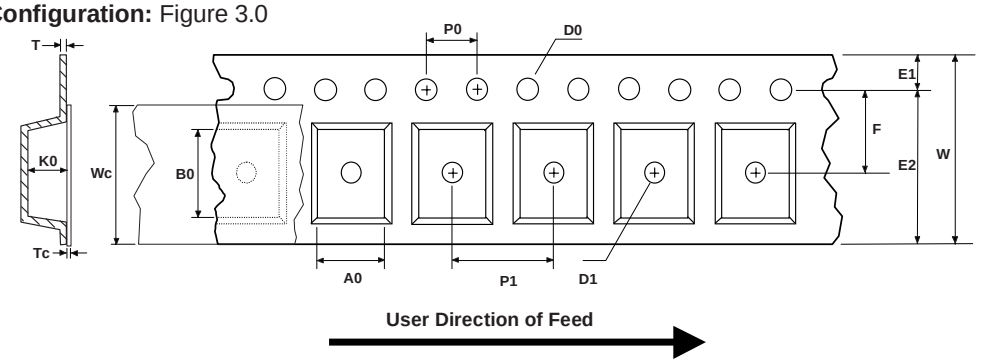
SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



SO-8 Tape and Reel Data and Package Dimensions, continued

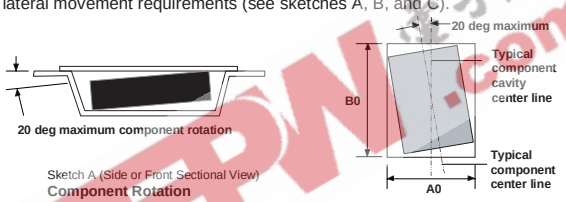
SOIC(8lds) Embossed Carrier Tape

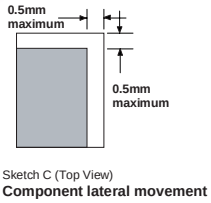
Configuration: Figure 3.0



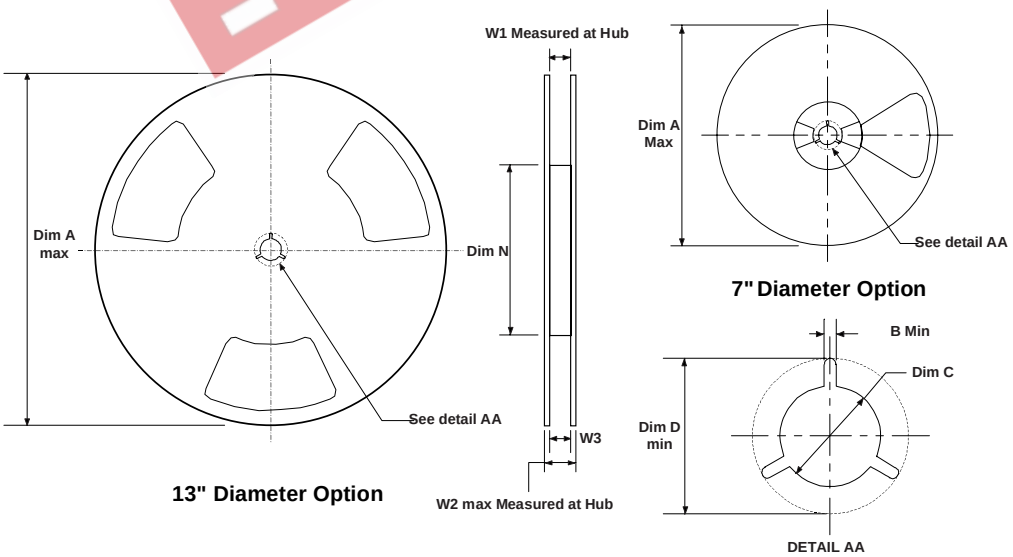
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).





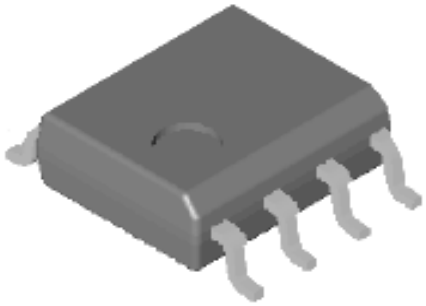
SOIC(8lds) Reel Configuration: Figure 4.0

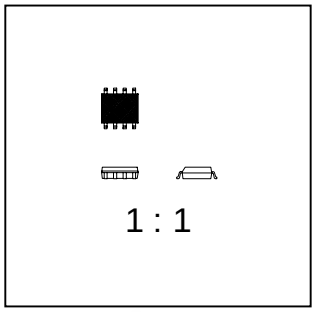


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC-8 (FS PKG Code S1)

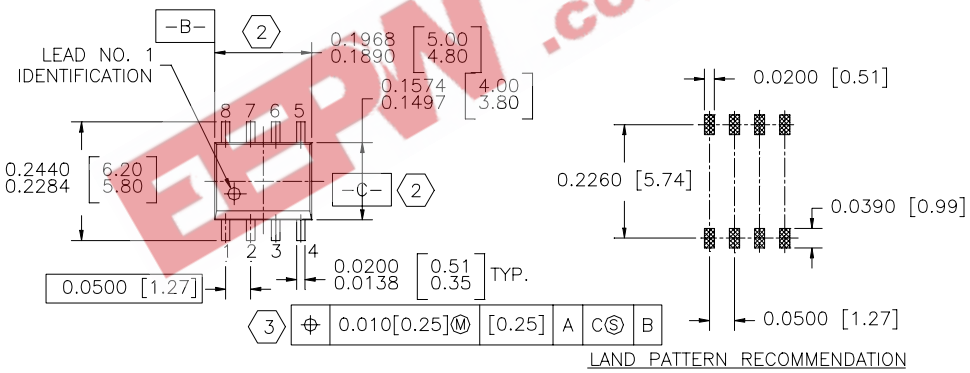


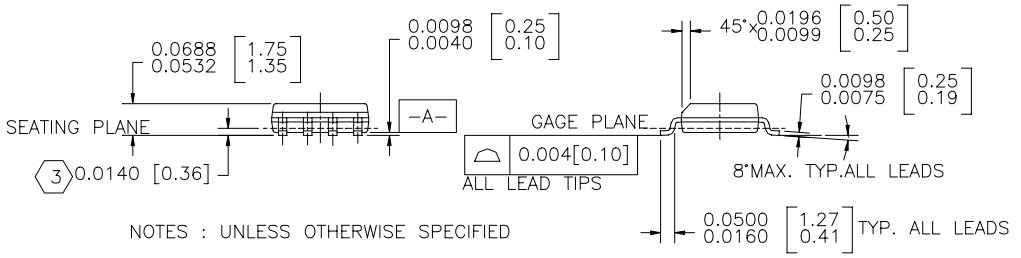


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774





NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MINIMUM
LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

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POP™
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