FAIRCHILD SEMICONDUCTOR TM

April 1998

FDR4410
N-Channel Enhancement Mode Field Effect Transistor

General Description

The FDR4410 has been designed as a smaller, low cost alternative to the popular Si4410DY.

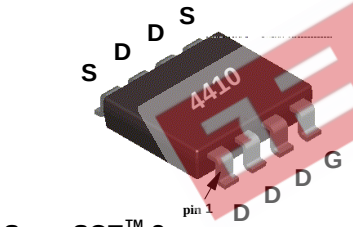
The SuperSOT™-8 package is 40% smaller than the SO-8 package.

The SuperSOT™-8 advanced package design and optimized pinout allow the typical power dissipation to be similar to the bigger SO-8 package.

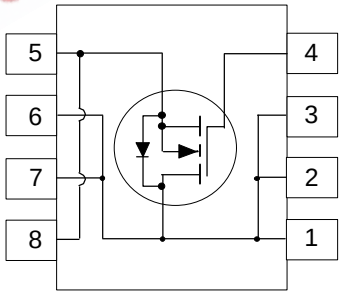
Features

- 9.3 A, 30 V. $R_{DS(ON)}$ = 0.013 Ω @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 0.020 Ω @ V_{GS} = 4.5 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- Proprietary SuperSOT™-8 small outline surface mount package with high power and current handling capability.

SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

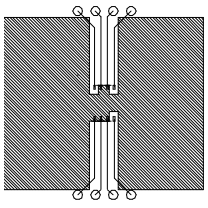
Symbol	Parameter		FDR4410	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Draint Current - Continuous	(Note 1a)	9.3	A
	- Pulsed		40	
P_D	Maximum Power Dissipation	(Note 1a)	1.8	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

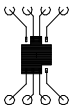
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		35		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			25	µA
I_{GSS}	Gate - Body Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSS}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	2	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	I_D = 250 µA, Referenced to 25 °C		-4.4		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 9.3 A		0.011	0.013	Ω
		T_J =125°C		0.017	0.02	
		V_{GS} = 4.5 V, I_D = 5 A		0.016	0.02	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 9.3 A		25		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1170		pF
C_{oss}	Output Capacitance			627		pF
C_{rss}	Reverse Transfer Capacitance			180		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		12	22	ns
t_r	Turn - On Rise Time			11	20	ns
$t_{D(off)}$	Turn - Off Delay Time			41	66	ns
t_f	Turn - Off Fall Time			34	55	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 9.3 A, V_{GS} = 10 V		36	50	nC
Q_{gs}	Gate-Source Charge			4.5		nC
Q_{gd}	Gate-Drain Charge			10		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)		0.72	1.2	V

Notes:

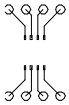
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 board in still air.



a. 70°C/W on a 1 in² pad of 2oz copper.



b. 125°C/W on a 0.026 in² of pad of 2oz copper.



c. 135°C/W on a 0.005 in² of pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

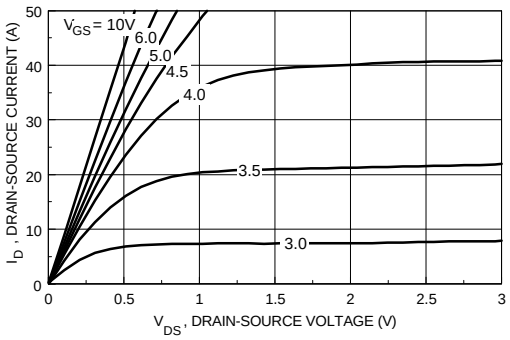


Figure 1. On-Region Characteristics.

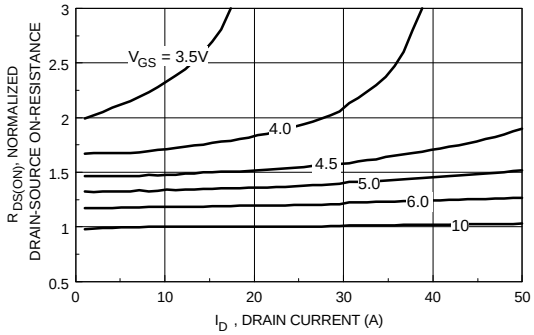


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

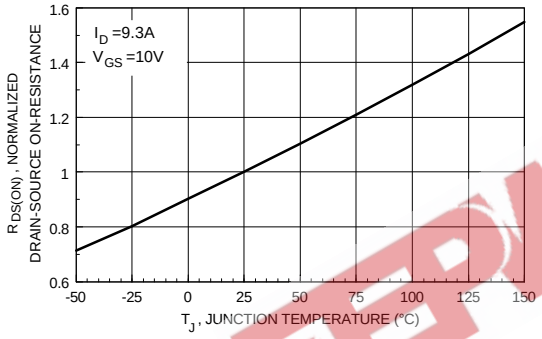


Figure 3. On-Resistance Variation with Temperature.

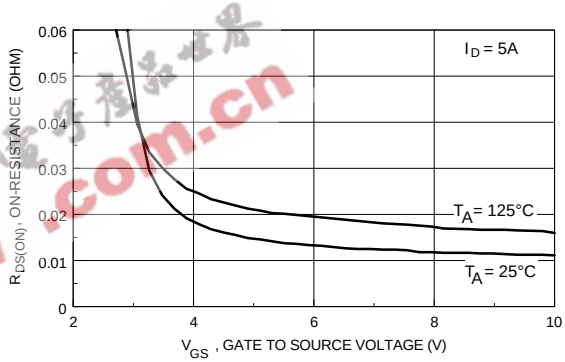


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

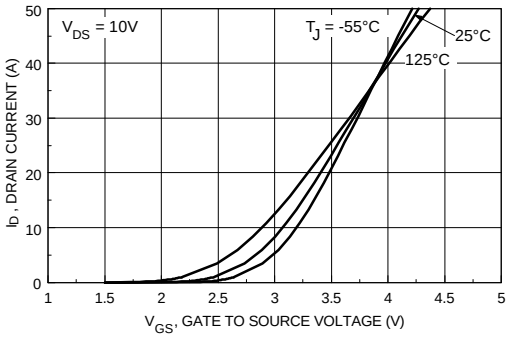


Figure 5. Transfer Characteristics.

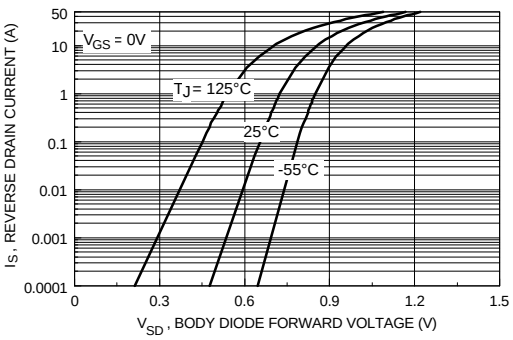


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

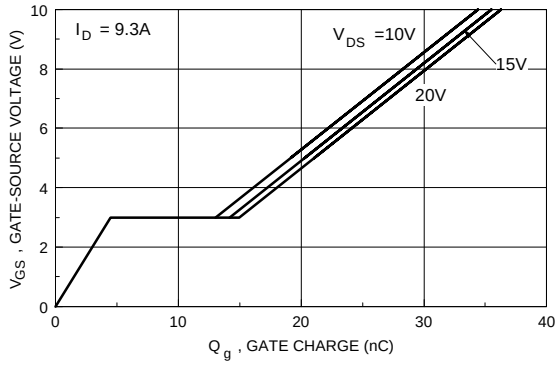


Figure 7. Gate Charge Characteristics.

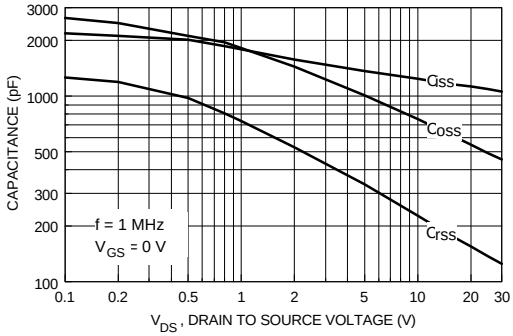


Figure 8. Capacitance Characteristics.

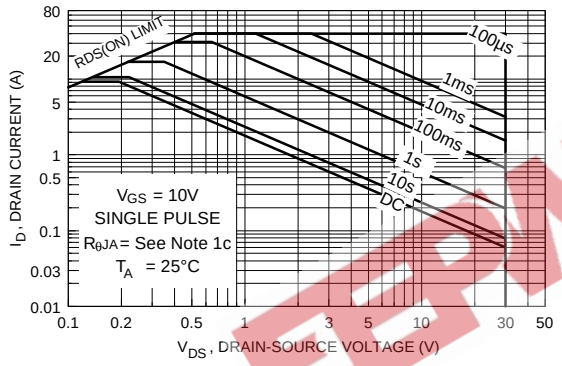


Figure 9. Maximum Safe Operating Area.

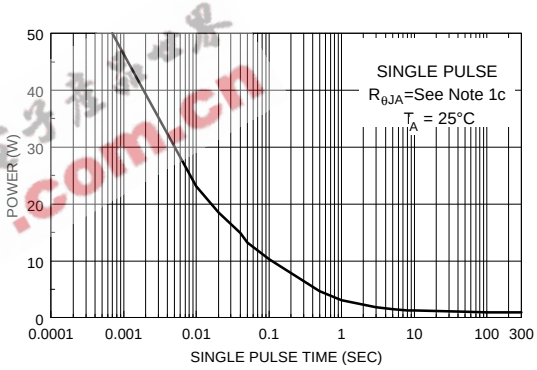


Figure 10. Single Pulse Maximum Power Dissipation.

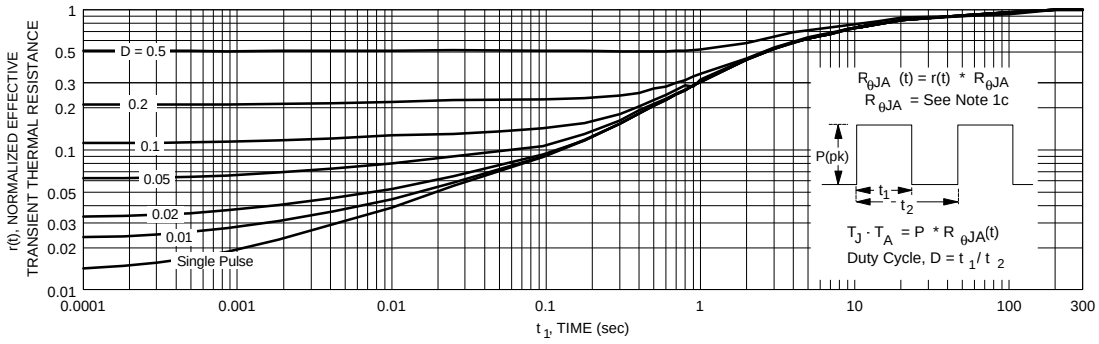


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c.
Transient thermalresponse will change depending on the circuit board design.