

## FDH50N50 / FDA50N50

### 500V N-Channel MOSFET

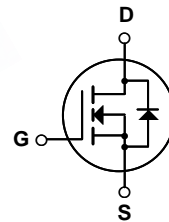
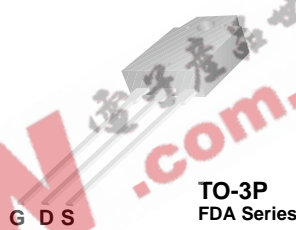
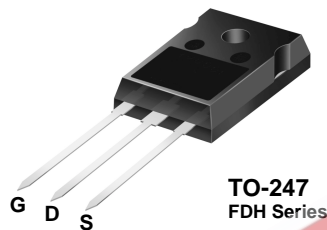
#### Features

- 48A, 500V,  $R_{DS(on)} = 0.105\Omega @ V_{GS} = 10\text{ V}$
- Low gate charge ( typical 105 nC)
- Low  $C_{rss}$  ( typical 45 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



#### Absolute Maximum Ratings

Symbol	Parameter	FDH50N50/FDA50N50	Unit
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	48 30.8	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	192	A
$V_{GSS}$	Gate-Source voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1868	mJ
$I_{AR}$	Avalanche Current (Note 1)	48	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	62.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	625 5	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.2	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24	--	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH50N50	FDH50N50	TO-247	-	-	30
FDA50N50	FDA50N50	TO-3P	-	-	30

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

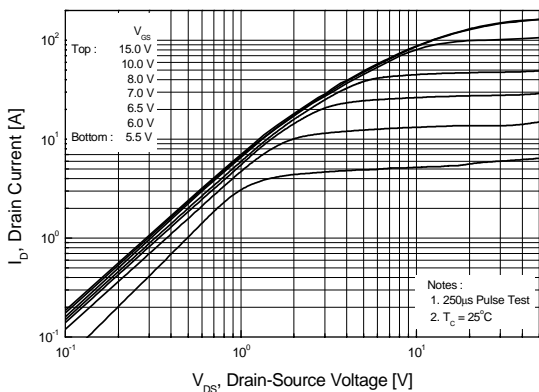
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 400V, T <sub>C</sub> = 125°C	--	--	25 250	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 24A	--	0.089	0.105	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 48A (Note 4)	--	20	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	4979	6460	pF
C <sub>oss</sub>	Output Capacitance		--	760	1000	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	50	65	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	161	--	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0V to 400V, V <sub>GS</sub> = 0V	--	342	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250V, I <sub>D</sub> = 48A R <sub>G</sub> = 25Ω	--	105	220	ns
t <sub>r</sub>	Turn-On Rise Time		--	360	730	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	225	460	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4, 5)	--	230	470	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400V, I <sub>D</sub> = 48A V <sub>GS</sub> = 10V	--	105	137	nC
Q <sub>gs</sub>	Gate-Source Charge		--	33	--	nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4, 5)	--	45	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	48	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	192	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 48A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 48A	--	580	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> /dt = 100A/μs (Note 4)	--	10	--	μC

### NOTES:

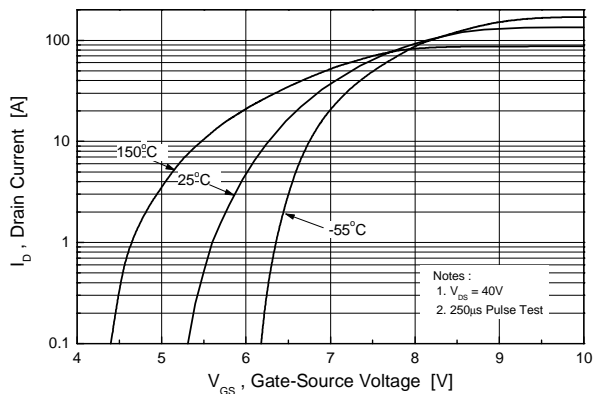
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 1.46mH, I<sub>AS</sub> = 48A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 48A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

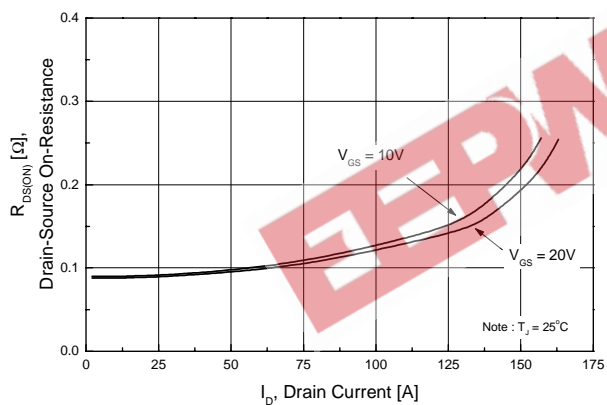
**Figure 1. On-Region Characteristics**



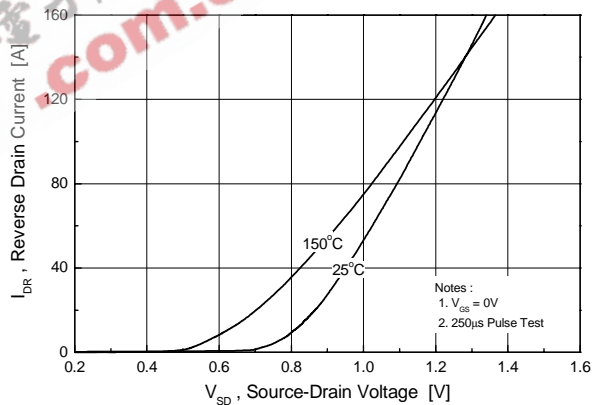
**Figure 2. Transfer Characteristics**



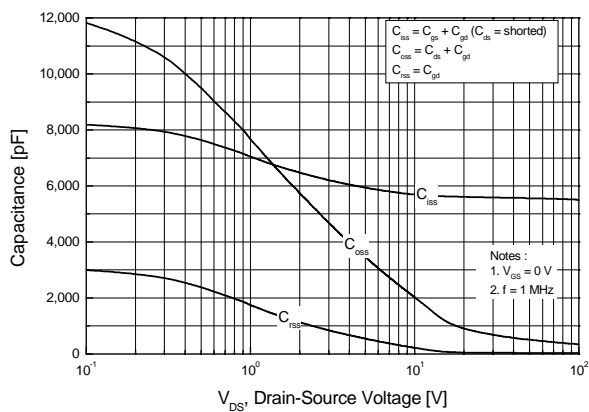
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



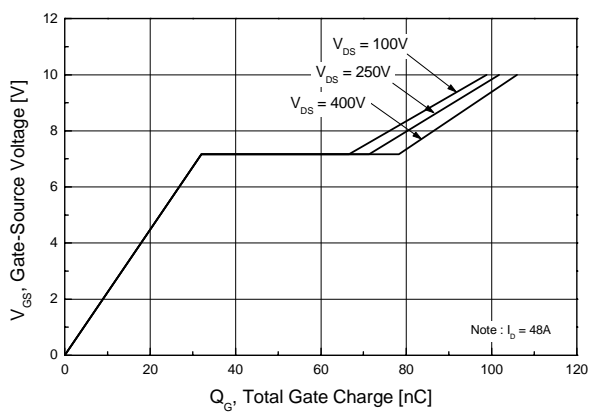
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

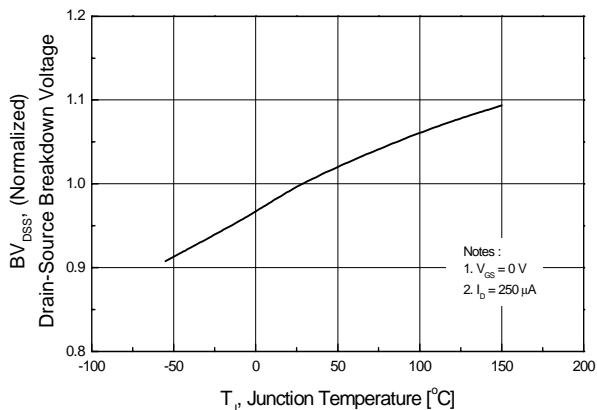


**Figure 6. Gate Charge Characteristics**

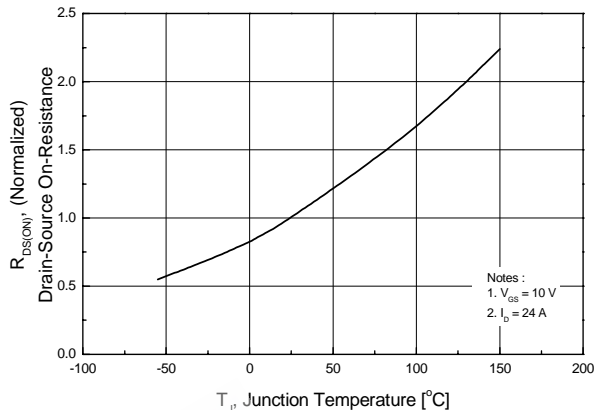


**Typical Performance Characteristics (Continued)**

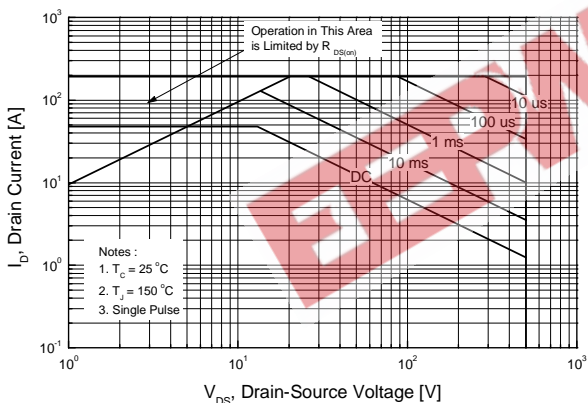
**Figure 7. Breakdown Voltage Variation vs. Temperature**



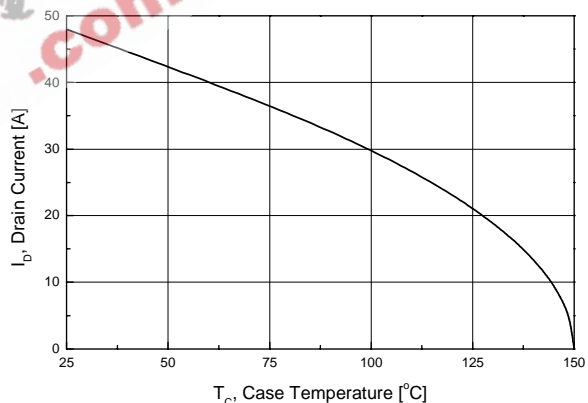
**Figure 8. On-Resistance Variation vs. Temperature**



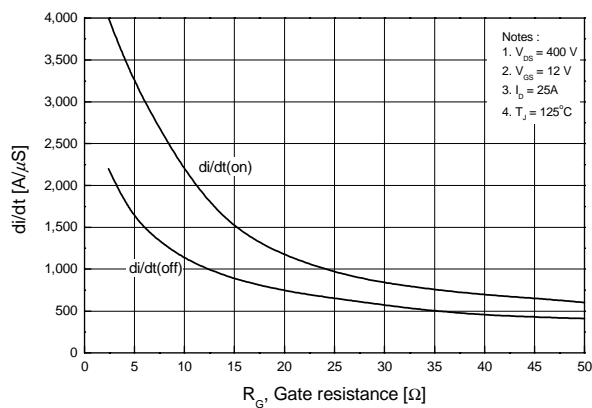
**Figure 9. Maximum Safe Operating Area**



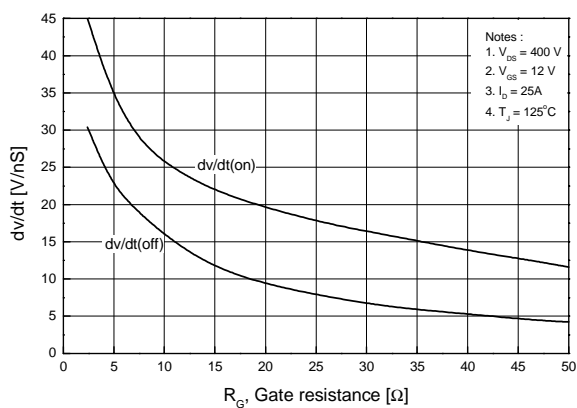
**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Typical Drain Current Slope vs. Gate Resistance**

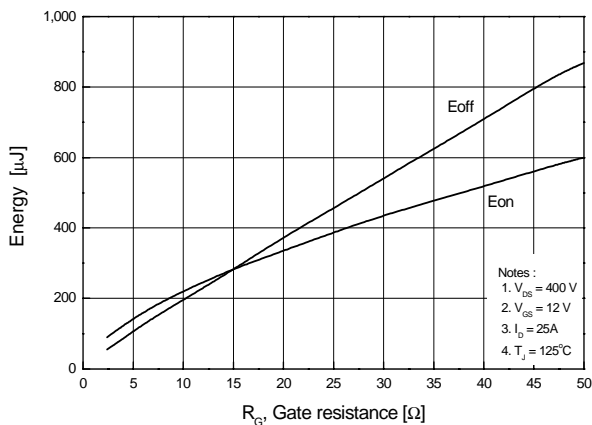


**Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance**

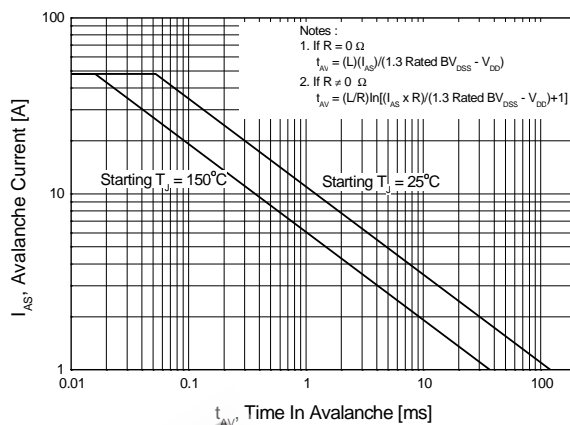


**Typical Performance Characteristics (Continued)**

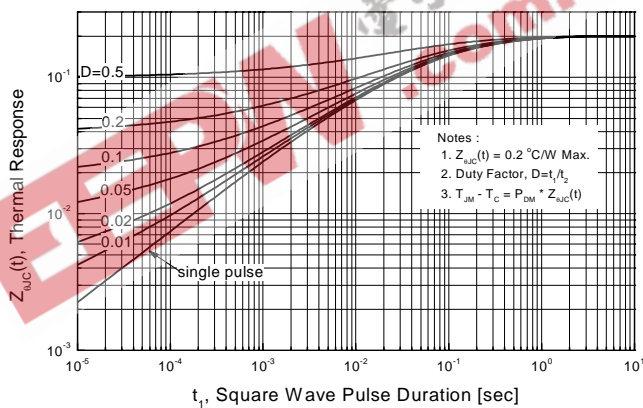
**Figure 13. Typical Switching Losses vs. Gate Resistance**



**Figure 14. Unclamped Inductive Switching Capability**



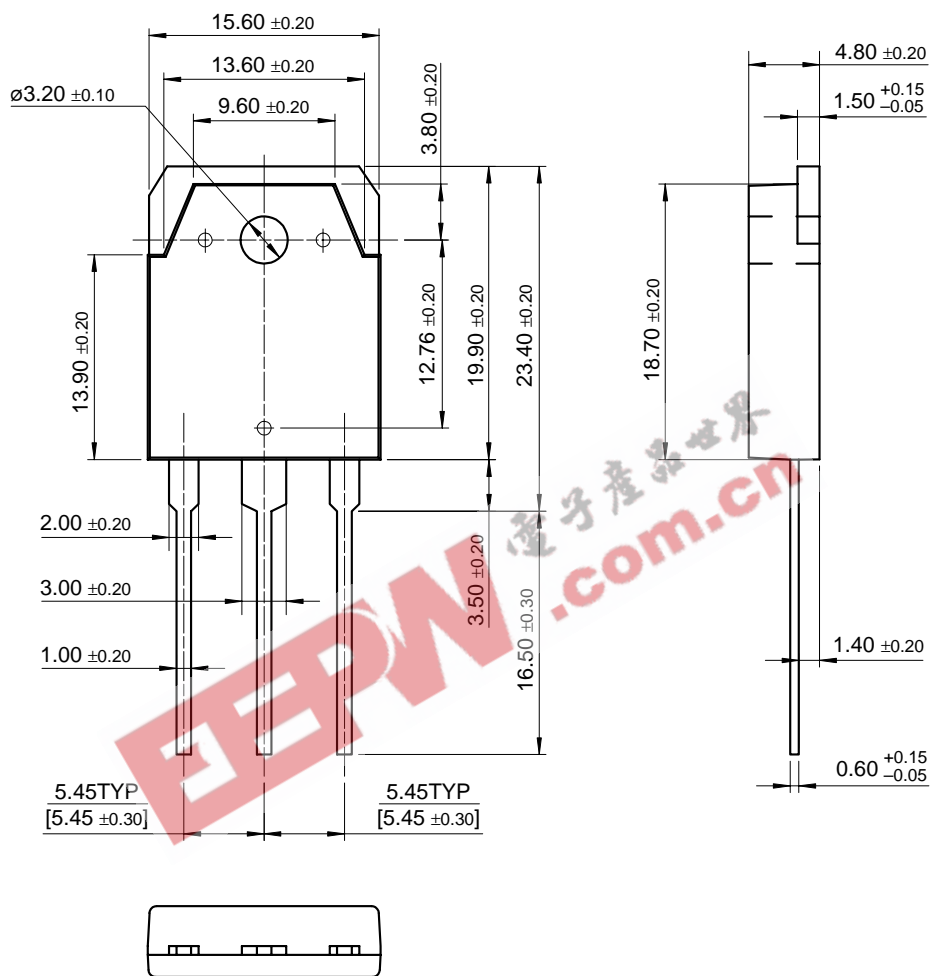
**Figure 15. Transient Thermal Resistance Curve**





Mechanical Dimensions (Continued)

TO-3P



Dimensions in Millimeters

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