FAIRCHILD SEMICONDUCTOR®

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FIN224AC
µSerDes™ 22-Bit Bi-Directional Serializer/Deserializer

Features

- Industry smallest 22-bit Serializer/ Deserializer pair
- Low power for minimum impact on battery life
  – Multiple power-down modes
- 100nA in standby mode, 5mA typical operating conditions
- Highly rolled LVCMOS edge rate option to meet regulatory requirements
- Cable reduction: 25:4 or greater
- Differential signaling:
  – –90dBm EMI when using CTL in lab conditions
  – Minimized shielding
  – Minimized EMI filter
  – Minimum susceptibility to external interference
- Up to 22 bits in either direction
- Up to 26MHz parallel interface operation
- Voltage translation from 1.65V to 3.6V
- High ESD protection: > 15kV HBM
- Parallel I/O power supply (V_{DDP}) range, 1.65V - 3.6V
- Can support Microcontroller or RGB pixel interface

Applications

- Image sensors
- Small displays
  – LCD, cell phone, digital camera, portable gaming, printer, PDA, video camera, automotive

FIN224AC to FIN24AC Comparison

- Up to 20% power reduction
- Double wide CKP pulse on FIN224AC, Mode 3
- Rolled edge rate for deserializer outputs on FIN224AC, for single display applications
- Same voltage range
- Same pinout and package

General Description

The FIN224AC µSerDes™ is a low-power Serializer/ Deserializer (SerDes) that can help minimize the cost and power of transferring wide signal paths. Through the use of serialization, the number of signals transferred from one point to another can be significantly reduced. Typical reduction is 4:1 to 6:1 for unidirectional paths. For bidirectional operation, using half duplex for multiple sources, it is possible to reach signal reduction close to 10:1. Through the use of differential signaling, shielding and EMI filters can also be minimized, further reducing the cost of serialization. The differential signaling is also important for providing a noise-insensitive signal that can withstand radio and electrical noise sources. Major reduction in power consumption allows minimal impact on battery life in ultra-portable applications. A unique word boundary technique assures that the actual word boundary is identified when the data is deserialized. This guarantees that each word is correctly aligned at the deserializer on a word-by-word basis through a unique sequence of clock and data that is not repeated except at the word boundary. It is possible to use a single PLL for most applications including bi-directional operation.

Ordering Information

Order Number	Package Number	Pb-Free	Package Description
FIN224ACGFX	BGA042	Yes	42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide (Slow LVCMOS Edge Rate)
FIN224ACMLX	MLP040	Yes	40-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square (Slow LVCMOS Edge Rate)

Pb-Free package per JEDEC J-STD-020B. BGA and MLP packages available in tape and reel only.

µSerDes™ is a trademark of Fairchild Semiconductor Corporation.

Basic Concept

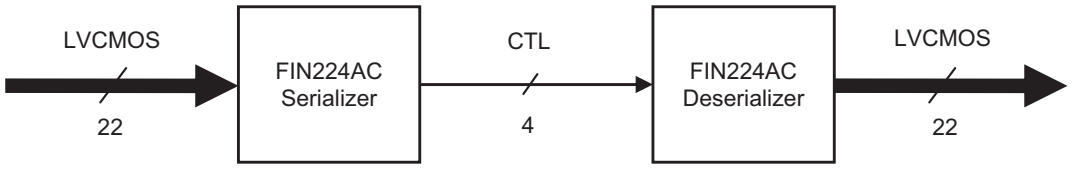


Figure 1. Conceptual Diagram

Functional Block Diagram

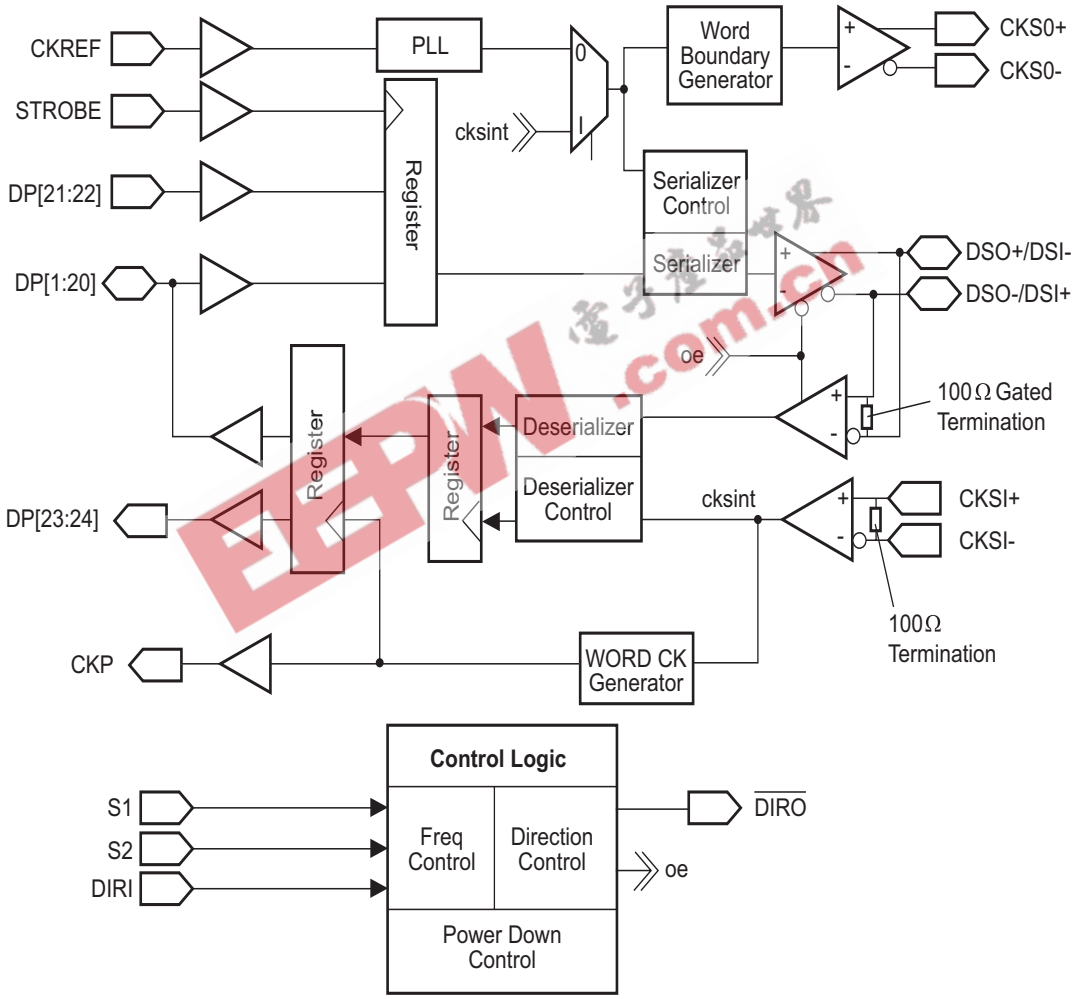


Figure 2. Block Diagram

Terminal Description

Terminal Name	I/O Type	Number of Terminals	Description of Signals
DP[1:20]	I/O	20	LVCMOS parallel I/O, Direction controlled by DIRI pin
DP[21:22]	I	2	LVCMOS parallel unidirectional inputs
DP[23:24]	O	2	LVCMOS unidirectional parallel outputs
CKREF	IN	1	LVCMOS clock input and PLL reference
STROBE	IN	1	LVCMOS strobe signal for latching data into the serializer
CKP	OUT	1	LVCMOS word clock output
DSO+ / DSI- DSO- / DSI+	DIFF-I/O	2	CTL differential serial I/O data signals(1) DSO: Refers to output signal pair DSI: Refers to input signal pair DSO(I)+: Positive signal of DSO(I) pair DSO(I)-: Negative signal of DSO(I) pair
CKSI+ CKSI-	DIFF-IN	2	CTL differential deserializer input bit clock CKSI: Refers to signal pair CKSI+: Positive signal of CKSI pair CKSI-: Negative signal of CKSI pair
CKSO+ CKSO-	DIFF-OUT	2	CTL differential serializer output bit clock CKSO: Refers to signal pair CKSO+: Positive signal of CKSO pair CKSO-: Negative signal of CKSO pair
S1	IN	1	LVCMOS mode selection terminals used to select frequency range for the reflect, CKREF
S2	IN	1	
DIRI	IN	1	LVCMOS control input used to control direction of data flow: DIRI = “1” Serializer DIRI = “0” Deserializer
$\overline{\text{DIRO}}$	OUT	1	LVCMOS control output inversion of DIRI
V_{DDP}	Supply	1	Power supply for parallel I/O and translation circuitry
V_{DDS}	Supply	1	Power supply for core and serial I/O
V_{DDA}	Supply	1	Power supply for analog PLL circuitry
GND	Supply	2	For ground signals (2 for µBGA, 1 for MLP)

Notes:
1. The DSO/DSI serial port pins have been arranged such that if one device is rotated 180 degrees with respect to the other device, the serial connections properly align without the need for any traces or cable signals to cross. Other layout orientation may require that traces or cables cross.

Connection Diagrams

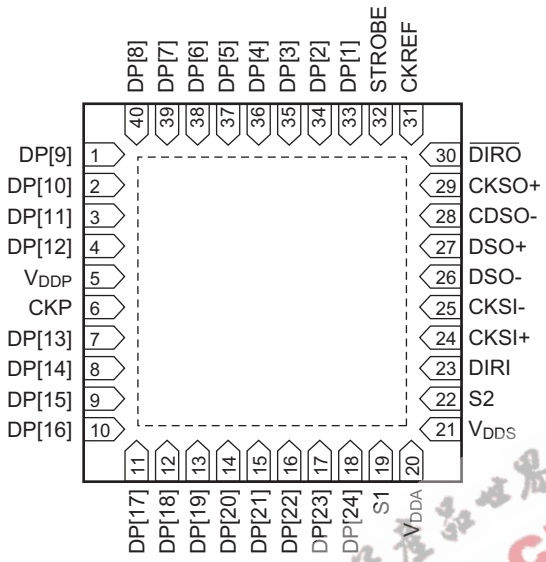
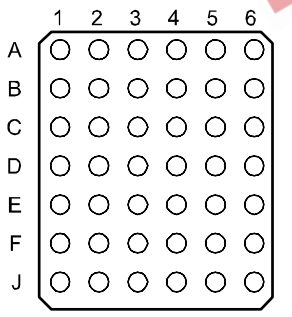


Figure 3. Terminal Assignments for µBGA (Top View)

42 MBGA Package
3.5mm x 4.5mm
(.5mm Pitch)
(Top View)



Pin Assignments

	1	2	3	4	5	6
A	DP[9]	DP[7]	DP[5]	DP[3]	DP[1]	CKREF
B	DP[11]	DP[10]	DP[6]	DP[2]	STROBE	$\overline{\text{DIRO}}$
C	CKP	DP[12]	DP[8]	DP[4]	CKSO+	CKSO-
D	DP[13]	DP[14]	VDDP	GND	DSO-/DSI+	DSO+/DSI-
E	DP[15]	DP[16]	GND	VDDS	CKSI+	CKSI-
F	DP[17]	DP[18]	DP[21]	VDDA	S2	DIRI
J	DP[19]	DP[20]	DP[22]	DP[23]	DP[24]	S1

Figure 4. Terminal Assignments for µBGA (Top View)

Control Logic Circuitry

The FIN224AC has the ability to be used as a 22-bit serializer or a 22-bit deserializer. Pins S1 and S2 must be set to accommodate the clock reference input frequency range of the serializer. Table 1 shows the pin programming of these options based on the S1 and S2 control pins. The DIRI pin controls whether the device is a serializer or a deserializer. When DIRI is asserted LOW, the device is configured as a deserializer. When the DIRI pin is asserted HIGH, the device is configured as a serializer. Changing the state on the DIRI signal reverses the direction of the I/O signals and generate the opposite state signal on DIRO. For unidirectional operation the DIRI pin should be hardwired to the HIGH or LOW state and the DIRO pin should be left floating. For bi-directional operation, the DIRI of the master device is driven by the system and the DIRO signal of the master is used to drive the DIRI of the slave device.

Serializer/Deserializer with Dedicated I/O Variation

The serialization and deserialization circuitry is set up for 24 bits. Because of the dedicated inputs and outputs, only 22 bits of data are ever serialized or deserialized. Regardless of the mode of operation, the serializer is always sending 24 bits of data plus 2 boundary bits and the deserializer is always receiving 24 bits of data and 2 word boundary bits. Bits 23 and 24 of the serializer always contain the value of zero and are discarded by the deserializer. DP[21:22] input to the serializer is deserialized to DP[23:24] respectively.

Turn-Around Functionality

The device passes and inverts the DIRI signal through the device asynchronously to the DIRO signal. Care must be taken by the system designer to ensure that no contention occurs between the deserializer outputs and the other devices on this port. Optimally the peripheral device driving the serializer should be put into a HIGH-impedance state prior to the DIRI signal being asserted. When a device with dedicated data outputs turns from a deserializer to a serializer, the dedicated outputs remain at the last logical value asserted. This value only changes if the device is once again turned around into a deserializer and the values are overwritten.

Power-Down Mode: (Mode 0)

Mode 0 is used for powering down and resetting the device. When both of the mode signals are driven to a LOW state, the PLL and references are disabled, differential input buffers are shut off, differential output buffers are placed into a HIGH-impedance state, LVCMOS outputs are placed into a HIGH-impedance state, and LVCMOS inputs are driven to a valid level internally. Additionally all internal circuitry is reset. The loss of CKREF state is also enabled to ensure that the PLL only powers-up if there is a valid CKREF signal.

In a typical application mode, signals of the device do not change states other than between the desired frequency range and the power-down mode. This allows for system-level power-down functionality to be implemented via a single wire for a SerDes pair. The S1 and S2 selection signals that have their operating mode driven to a “logic 0” should be hardwired to GND. The S1 and S2 signals that have their operating mode driven to a “logic 1” should be connected to a system-level power-down or reset signal.

Table 1. Control Logic Circuitry

Mode Number	S2	S1	DIRI	Description
0	0	0	x	Power-Down Mode
1	0	1	1	22-Bit Serializer 2MHz to 5MHz CKREF
	0	1	0	22-Bit Deserializer
2	1	0	1	22-Bit Serializer 5MHz to 15MHz CKREF
	1	0	0	22-Bit Deserializer
3	1	1	1	22-Bit Serializer 10MHz to 26MHz CKREF (Divide by 2 Serial Data) (Note: FIN224C required for RGB applications)
	1	1	0	22-Bit Serializer

Serializer Operation Mode

The serializer configurations are described in the following sections. The basic serialization circuitry works essentially identically in these modes, but the actual data and clock streams differ depending on if CKREF is the same as the STROBE signal or not. When it is stated that CKREF does not equal STROBE, each signal is distinct and CKREF must be running at a frequency high enough to avoid any loss of data condition. CKREF must never be a lower frequency than STROBE.

Serializer Operation: (Figure 5)
MODE 1 or MODE 2,
DIRI = 1,
CKREF = STROBE

The PLL must receive a stable CKREF signal to achieve lock prior to any valid data being sent. The CKREF signal can be used as the data STROBE signal provided that data can be ignored during the PLL lock phase.

Once the PLL is stable and locked, the device can begin to capture and serialize data. Data is captured on the rising edge of the STROBE signal and then serialized. The serialized data stream is synchronized and sent source synchronously with a bit clock with an embedded word boundary. When operating in this mode, the internal deserializer circuitry is disabled, including the serial clock, serial data input buffers, the bi-directional parallel outputs, and the CKP word clock. The CKP word clock is driven HIGH.

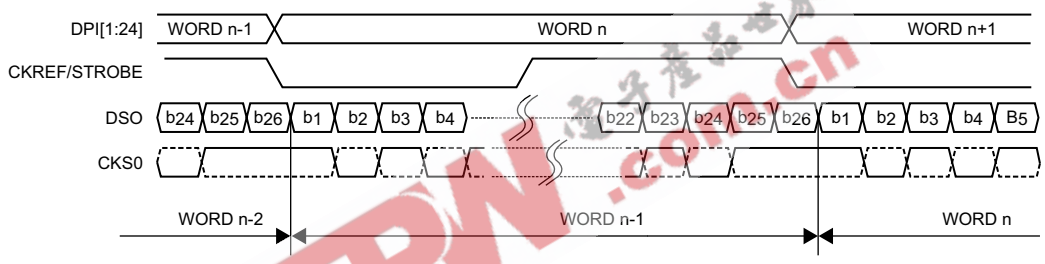


Figure 5. Serializer Timing Diagram (CKREF = STROBE)

Serializer Operation: (Figure 6),
DIRI = 1,
CKREF does not = STROBE

If the same signal is not used for CKREF and STROBE, the CKREF signal must be run at a higher frequency than the STROBE rate to serialize the data correctly. The actual serial transfer rate remains at 13 times the CKREF frequency. A data bit value of zero is sent when no valid data is present in the serial bit stream. The operation of the serializer otherwise remains the same.

The exact frequency that the reference clock needs to run at depends upon the stability of the CKREF and STROBE signal. If the source of the CKREF signal implements spread spectrum technology, the max frequency of the spread spectrum clock should be used in calculating the ratio of STROBE frequency to the CKREF frequency. Similarly, if the STROBE signal has significant cycle-to-cycle variation, the maximum cycle-to-cycle time needs to be factored into the selection of the CKREF frequency.

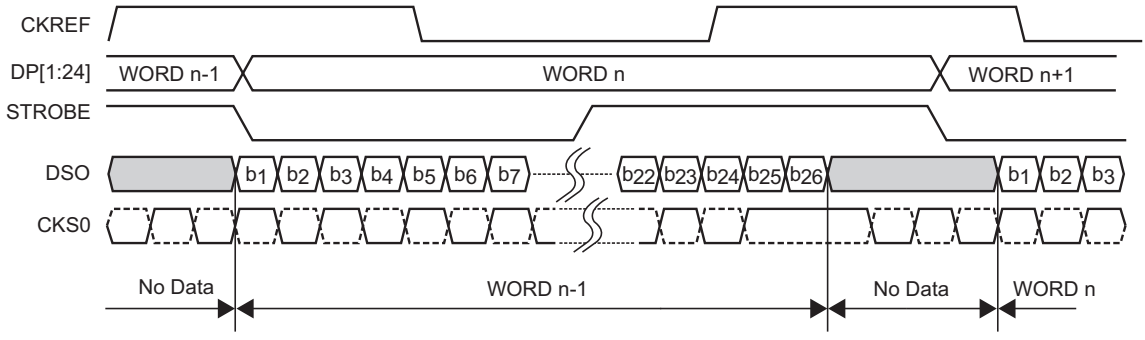


Figure 6. Serializer Timing Diagram (CKREF does not equal STROBE)

Serializer Operation Mode (Continued)

Serializer Operation: (Figure 7), MODE 3 (S1 = S2 = 1), DIRI = 1, CKREF Divide by 2 mode

When operating in mode 3, the effective serial speed is divided by two. This mode has been implemented to accommodate cases where the reference clock frequency is high compared to the actual strobe frequency. The actual strobe frequency must be less than or equal to 50% of the CKREF frequency for this mode to work properly. This mode, in all other ways, operates the same as described in the section where CKREF does not equal STROBE.

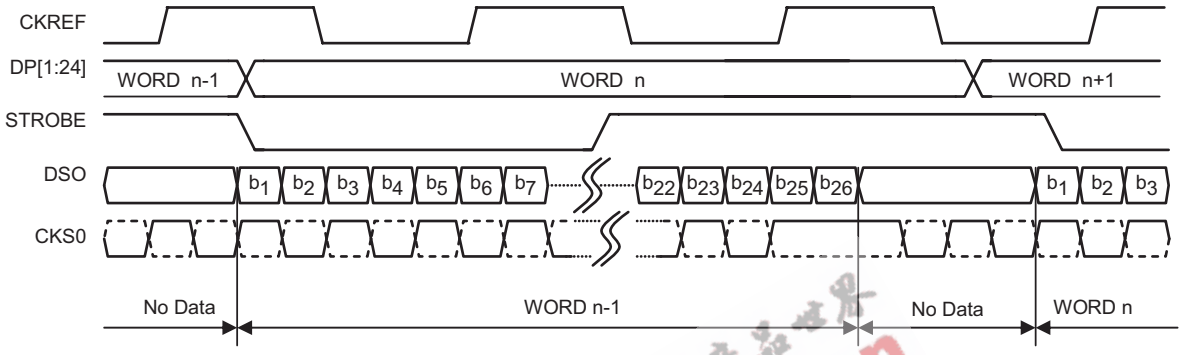


Figure 7. CKREF > 2x STROBE Frequency; Mode 3 Operation (S1 = S2 = 1)

Serializer Operation: (Figure 8), DIRI = 1, No CKREF

A third method of serialization can be acheived by providing a free-running bit clock on the CKSI signal. This mode is enabled by grounding the CKREF signal and driving the DIRI signal HIGH. At power-up, the device is configured to accept a serialization clock from CKSI. If a CKREF is received, this device enables the CKREF serialization mode. The device remains in this mode even if CKREF is stopped. To re-enable this mode, the device must be powered down and then powered back up with a “logic 0” on CKREF.

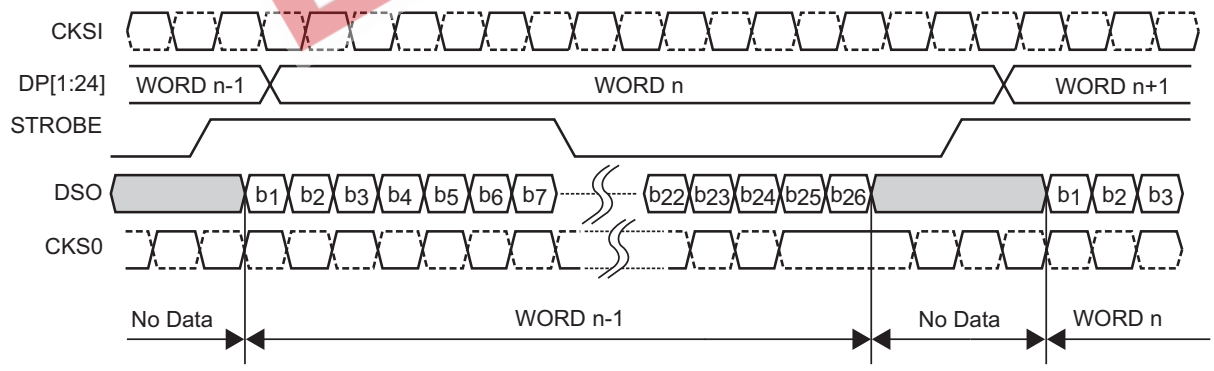


Figure 8. Serializer Timing Diagram Using Provided Bit Clock (No CKREF)

Deserializer Operation Mode

The operation of the deserializer is only dependent upon the data received on the DSI data signal pair and the CKSI clock signal pair. The following two sections describe the operation of the deserializer under two distinct serializer source conditions. References to the CKREF and STROBE signals refer to the signals associated with the serializer device used in generating the serial data and clock signals that are inputs to the deserializer. When operating in this mode, the internal serializer circuitry is disabled, including the parallel data input buffers. If there is a CKREF signal provided, the CKSO serial clock continues to transmit bit clocks. Upon device power-up (S1 or S2 = 1), all deserializer output data pins are driven LOW until valid data is passed through the deserializer.

Deserializer Operation: DIRI = 0 (Serializer Source: CKREF = STROBE)

When the DIRI signal is asserted LOW, the device is configured as a deserializer. Data is captured on the serial port and deserialized through use of the bit clock sent with the data. The word boundary is defined in the actual clock and data signal. Parallel data is generated at the time the word boundary is defined in the actual clock and data signal. Parallel data is generated at the time the word boundary is detected. The falling edge of CKP occurs approximately six bit times after the falling edge of CKSI. The rising edge of CKP goes HIGH approximately 13 bit times after CKP goes LOW. The rising edge of CKP is generated approximately 13 bit times later. When no embedded word boundary occurs, no pulse on CKP is generated and CKP remains HIGH.

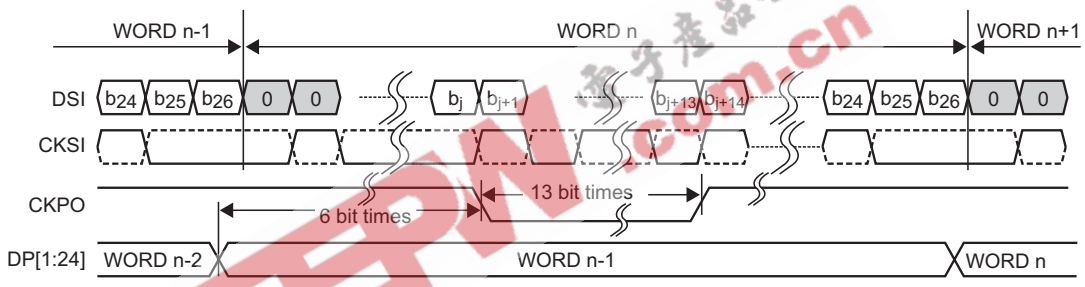


Figure 9. Deserializer Timing Diagram (Serializer Source: CKREF equals STROBE)

Deserializer Operation: DIRI = 0 (Serializer Source: CKREF does not = STROBE)

The logical operation of the deserializer remains the same if the CKREF is equal in frequency to the STROBE or at a higher frequency than the STROBE. The actual serial data stream presented to the deserializer is different because it has non-valid data bits sent between words. The duty cycle of CKP varies based on the ratio of the frequency of the CKREF signal to the STROBE signal. The frequency of the CKP signal is equal to the STROBE frequency. The falling edge of CKP occurs six bit times after the data transition. The LOW time of the CKP signal is equal to 13 serial bit times. In modes 1 and 2, the CKP LOW time equals half of the CKREF period of the serializer. In mode 3, the CKP LOW is equal to the CKREF period. The CKP HIGH time is approximately equal to the STROBE period, minus the CKP LOW time. Figure 10 is representative of a waveform that could be seen when CKREF is not equal to STROBE. If CKREF was significantly faster, additional non-valid data bits would occur between data words.

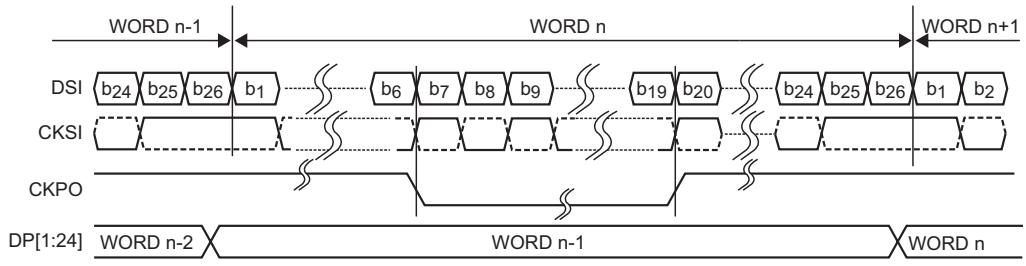


Figure 10. Deserializer Timing Diagram (Serializer Source: CKREF does not equal STROBE)

LVCMOS Data I/O

The LVCMOS input buffers have a nominal threshold value equal to half V_{DD}. The input buffers are only operational when the device is operating as a serializer. When the device is operating as a deserializer, the inputs are gated off to conserve power.

The LVCMOS 3-STATE output buffers are rated for a source / sink current of approximately 0.5mA at 1.8V. The outputs are active when the DIRI signal and either S1 or S2 is asserted HIGH. When the DIRI signal and either S1 or S2 is asserted LOW, the bi-directional LVCMOS I/Os is in a HIGH-Z state. Under purely capacitive load conditions, the output swings between GND and V_{DDP}. When S1 or S2 initially transitions HIGH, the initial state of the deserializer LVCMOS outputs is zero.

Unused LVCMOS input buffers must be either tied off to a valid logic LOW or a valid logic HIGH level to prevent static current draw due to a floating input. Unused LVCMOS output should be left floating. Unused bi-directional pins should be connected to GND through a high-value resistor. If a FIN224AC device is configured as an unidirectional serializer, unused data I/O can be treated as unused inputs. If the FIN224AC is hardwired as a deserializer, unused data I/O can be treated as unused outputs.

The FIN224AC family offers fast and slow LVCMOS edge rates to meet emissions and loading requirements.

Differential I/O Circuitry

The FIN224AC employs FSC proprietary Current Transistor Logic (CTL) Input / Output (I/O) technology. CTL is a low-power, low-EMI differential swing I/O technology. The CTL output driver generates a constant output source and sink current. The CTL input receiver senses the current difference and direction from the corresponding output buffer to which it is connected. This differs from LVDS, which uses a constant current source output, but a voltage sense receiver. Like LVDS, an input source termination resistor is required to properly terminate the transmission line. The FIN224AC device incorporates an internal termination resistor on the CKSI receiver and a gated internal termination resistor on the DS input receiver. The gated termination resistor ensures proper termination regardless of direction of data flow. The relative greater sensitivity of the current sense receiver of CTL allows it to work at much lower current drive and a much lower voltage.

During power down mode, the differential inputs are disabled and powered down and the differential outputs are placed in a HIGH-Z state. CTL inputs have an inherent failsafe capability that supports floating inputs. When the CKSI input pair of the serializer is unused, it can reliably be left floating. Alternately both of the inputs can be connected to ground. CTL inputs should never be connected to VDD. When the CKSO output of the deserializer is unused, it should be allowed to float.

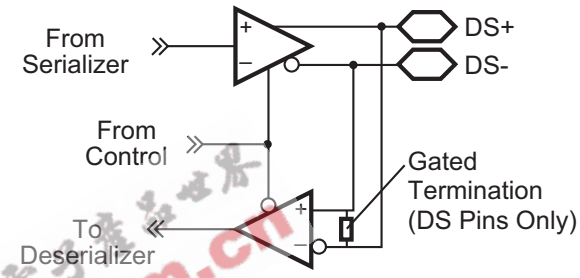


Figure 11. Bi-Directional Differential I/O Circuitry

Phase-Locked Loop (PLL) Circuitry

The CKREF input signal is used to provide a reference to the PLL. The PLL generates internal timing signals capable of transferring data at 13 times the incoming CKREF signal. The output of the PLL is a bit clock that is used to serialize the data. The bit clock is also sent source synchronously with the serial data stream. There are two ways to disable the PLL. The PLL can be disabled by entering the Mode 0 state (S1 = S2 = 0). The PLL disables immediately upon detecting a LOW on both the S1 and S2 signals. When any of the other modes are entered by asserting either S1 or S2 HIGH and by providing a CKREF signal, the PLL powers-up and goes through a lock sequence. One must wait the specified number of clock cycles prior to capturing valid data into the parallel port.

Application Mode Diagrams Unidirectional Data Transfer

Figure 14 shows a half duplex connectivity diagram with FIN224AC, which has similar functionality as FIN24AC. This connectivity allows for two unidirectional data streams to be sent across a single pair of SerDes. Data is sent on a frame-by-frame basis. For this mode of operation, there needs to be some synchronization between when the camera sends its data frame and when the LCD sends its data. One option is to have the LCD send data during the camera blanking period. External logic is needed for this mode of operation.

Devices alternate frames of data controlled by a direction control and a direction sense. When DIRI, on the right-hand FIN224AC is HIGH, data is sent from the camera to the camera interface at the base. When DIRI, on the right-hand FIN224AC, goes LOW, data is sent from the baseband process to the LCD. The direction is then changed at DIRO on the right-hand FIN224AC indicating to the left-hand FIN224AC to change direction. Data is sent from the base LCD unit to the LCD. The DIRO pin on the left-hand FIN24AC is used to indicate to the base control unit that the signals are changing direction and the LCD is available to be sent data. DIRI on the right-hand FIN224AC could typically use a timing reference signal, such as VSYNC from the camera interface, to indicate direction change. A derivative of this signal may be required to make sure that no data is lost in the final data transfer.

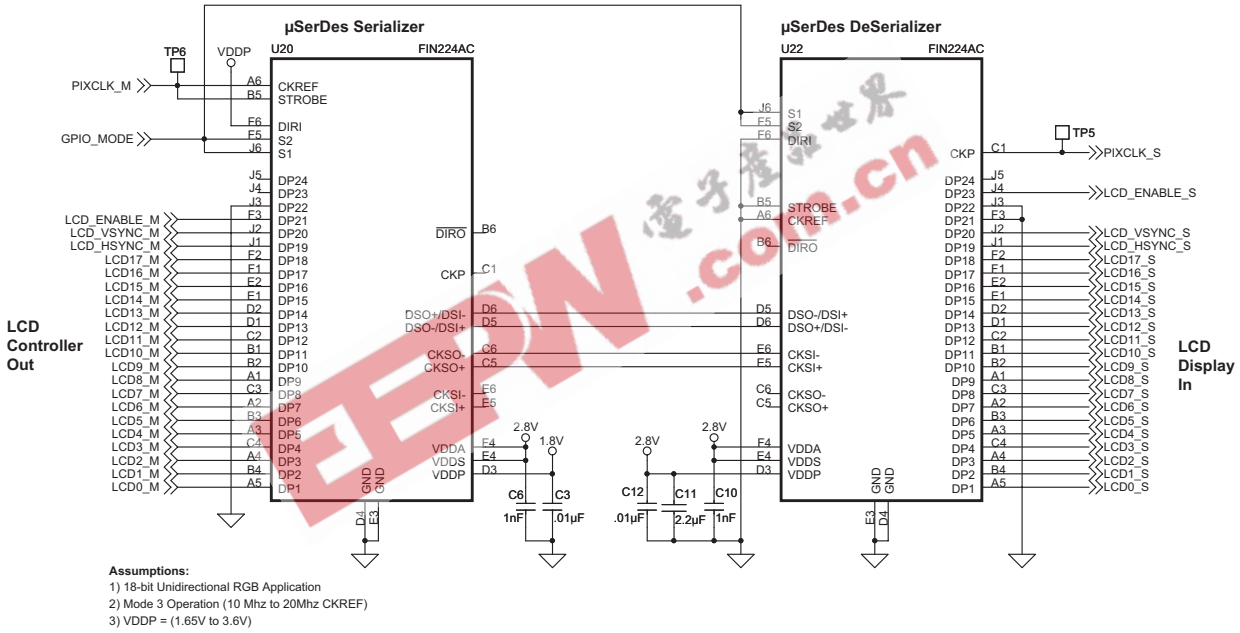


Figure 12. FIN224AC RGB

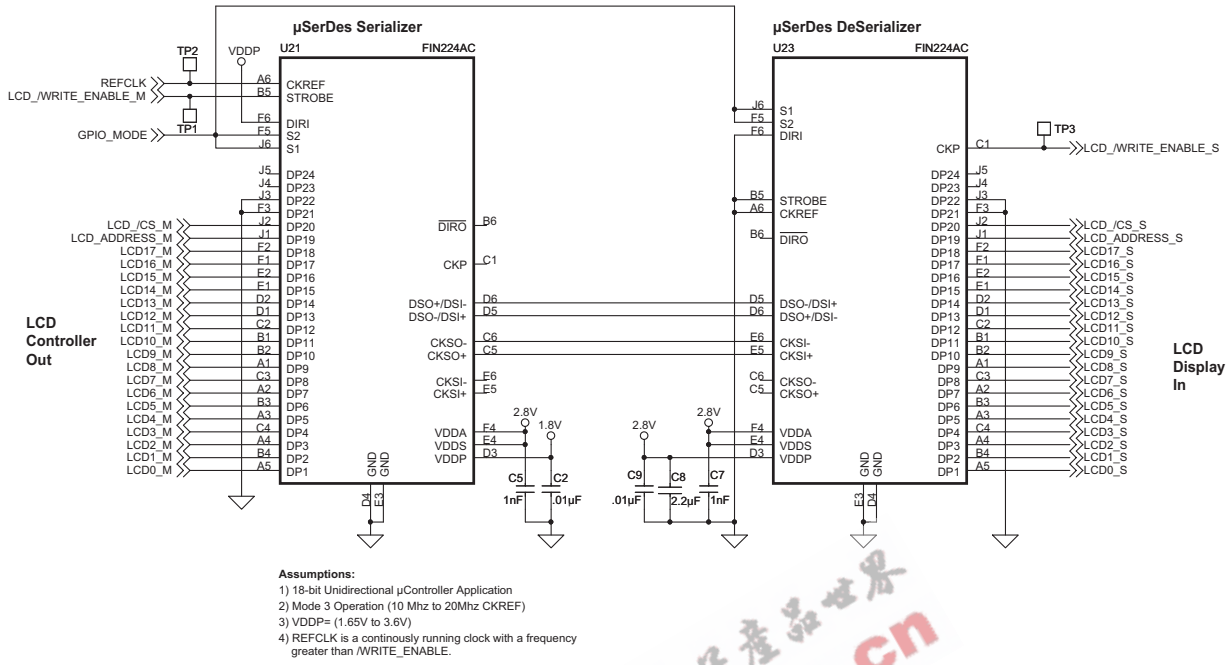


Figure 13. FIN224AC Microcontroller

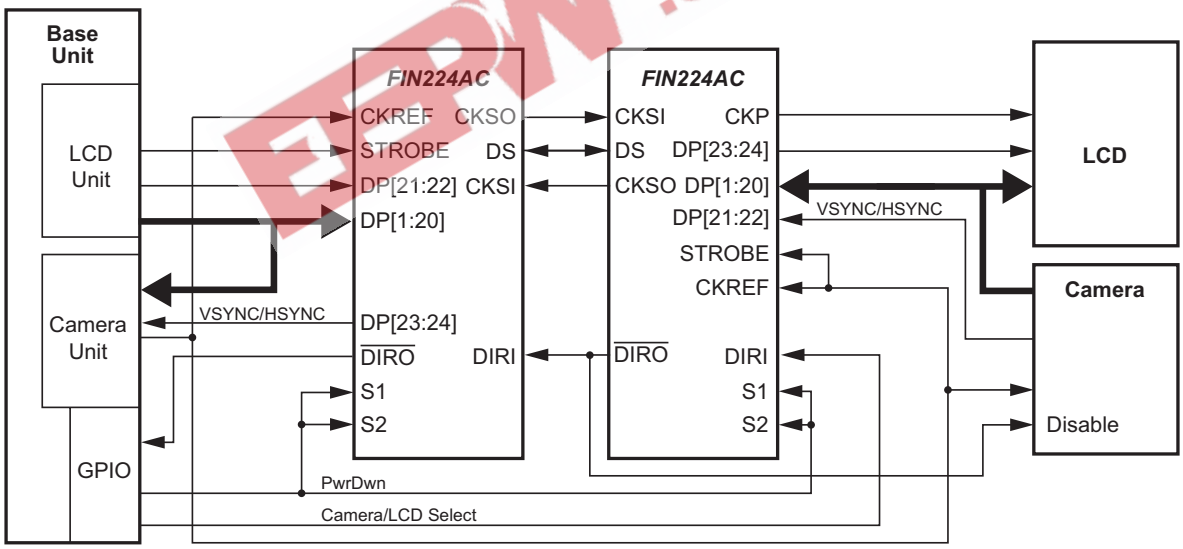


Figure 14. Multiple Units, Unidirectional Signals in Each Direction

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5	+4.6	V
	ALL input/Output Voltage	-0.5	+4.6	V
	CTL Output Short Circuit Duration	Continuous		
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
ESD	Human Body Model, 1.5KΩ, 100pF			
	All Pins		>2	kV
	S1, S2, CKSO, CKSI, DSO, DSI, VDDA, VDDS, VDDP (as specified in IEC61000-4-2)		>15	kV

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.5	3.0	V
V_{DDP}	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature[2]	-30	+70	°C
V_{DDA-PP}	Supply Noise Voltage		100	mVp-p

Notes:

2. Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specification should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

DC Electrical Characteristics

Over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.(3)	Max.	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			0.65 x V_{DDP}		V_{DDP}	
V_{IL}	Input Low Voltage			GND		0.35 x V_{DDP}	V
V_{OH}	Output High Voltage	I_{OH} = 2.0mA	V_{DDP} = 3.3±0.30	0.75 x V_{DDP}			V
			V_{DDP} = 2.5±-0.20				
			V_{DDP} = 1.8±0.18				
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	V_{DDP} = 3.3±0.30			0.25 x V_{DDP}	V
			V_{DDP} = 2.5±0.20				
			V_{DDP} = 1.8±0.18				
I_{IN}	Input Current	V_{IN} = 0V to 3.6V		-5.0		5.0	µA
DIFFERENTIAL I/O							
I_{ODH}	Output HIGH source current	V_{OS} = 1.0V			-1.75		µA
I_{ODL}	Output LOW sink current	V_{OS} = 1.0V			0.950		µA
I_{OS}	Short-Circuit Output Current	V_{OUT} = 0V	Driver Enabled				mA
			Driver Disabled			±5	µA
I_{OZ}	Disabled Output Leakage Current	CKSO, DSO = 0V to V_{DDS} S2 = S1 = 0V			±1	±5	µA
I_{TH}	Differential Input Threshold High Current	See Figure 6 and Table 2		50			µA
I_{TL}	Differential Input Threshold Low Current	See Figure 6 and Table 2				-50	µA
I_{IZ}	Disabled Input Leakage Current	CKSI, DSI = 0V to V_{DDS} S2 = S1 = 0V			±1	±5	uA
I_{IS}	Short-Circuit Input Current	Vout =V_{DDS}					mA
V_{ICM}	Input Common Mode Range	V_{DDS} = 2.775 ±5%		0.5		V_{DDS-1}	V
R_{TRM}	CKSI, DS Internal Receiver Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0 | $CKSI^+$ – $CKSI^-$ | = V_{ID}			100		Ω

Notes:

3. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into the device and negative values refer to the current flowing out of the pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).

Power Supply Currents

Symbol	Parameter	Test Conditions			Min.	Typ.(4)	Max.	Unit
IDDA1	VDDA Serializer Static Supply Current	All DP and Control Inputs at 0V or NOCKREF, S2 = 0, S1 = 1, DIR = 1				450		µA
IDDA2	VDDA Deserializer Static Supply Current	All DP and Control Inputs at 0V or NOCKREF, S2 = 0, S1 = 1, DIR = 0				550		µA
IDDS1	VDDS Serializer Static Supply Current	All DP and Control Inputs at 0V or NOCKREF, S2 = 0, S1 = 1, DIR = 1				4		mA
IDDS2	VDDS Deserializer Static Supply Current	All DP and Control Inputs at 0V or NOCKREF, S2 = 0, S1 = 1, DIR = 0				4.5		mA
IDD_PD	VDD Power-Down Supply Current IDD_PD = IDDA	S1 = S2 = 0 All Inputs at GND or VDD				0.1		µA
IDD_SER1	26:1 Dynamic Serializer Power Supply Current IDD_SER1 = IDDA+IDDS+IDDP	CKREF = STROBE DIRI = H	S2 = 0 S1 = 1	2MHz		9		mA
				5MHz		14		
			S2 = 1 S1 = 0	5MHz		9		
				15MHz		17		
			S2 = 1 S1 = 1	10MHz		9		
				26MHz		16		
IDD_DES1	26:1 Dynamic Deserializer Power Supply Current IDD_DES1 = IDDA+IDDS+IDDP	CKREF = STROBE DIRI = L	S2 = 0 S1 = 1	2MHz		5		mA
				5MHz		6		
			S2 = 1 S1 = 0	5MHz		4		
				15MHz		5		
			S2 = 1 S1 = 1	10MHz		7		
				26MHz		11		
IDD_SER2	26:1 Dynamic Serializer Power Supply Current IDD_SES2 = IDDA+IDDS+IDDP	NO CKREF STROBE Active CKSI = 15x STROBE DIRI = H		2MHz		8		mA
				5MHz		8		
				10MHz		10		
				15MHz		12		

Notes:

4. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into the device and negative values refer to the current flowing out of the pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).

AC Electrical Characteristics

Characteristics at recommended over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.(5)	Max.	Units
Serializer Input Operating Conditions							
t_{TCP}	CKREF Clock Period (2MHz – 20MHz)	CKREF = STROBE See Figure 15	S2=0 S1=1 S2=1 S1=0 S2=1 S1=1	200 66 38.5	T	500 200 100	ns
f_{REF}	CKREF Frequency Relative to STROBE	CKREF does not = STROBE	S2=0 S1=1	2.25 x f_{STROBE}			MHz
t_{CPWH}	CKREF Clock High Time			0.2	0.5		T
t_{CPWL}	CKREF Clock Low Time			0.2	0.5		T
t_{CLKT}	LVCMOS Input Transition Time	See Figure 17				90.0	ns
t_{SPWH}	STROBE Pulse Width HIGH/LOW	See Figure 17		(Tx4)/26		(Tx22)/26	ns
f_{MAX}	Maximum Serial Data Rate	CKREF x 26	S2=0 S1=1 S2=1 S1=0 S2=1 S1=1	52 130 260		130 390 676	Mb/s
t_{STC}	$DP_{(n)}$ Setup to STROBE	DIRI = 1		2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE			2.0			ns
Serializer AC Electrical Characteristics							
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	CKREF = STROBE		33a+1.5		35a+6.5	ns
t_{SPOS}	CKSO Position Relative to DS(6)			-50.0		250	ps
PLL AC Electrical Characteristics							
t_{TPLLS0}	Serializer Phase Lock Loop Stabilization Time	See Figure 19				200	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock	See Figure 22				30.0	µs
t_{TPLLD1}	PLL Power-Down Time(7)	See Figure 23				20.0	ns
Deserializer Input Operating Conditions							
t_{S_DS}	Serial Port Setup Time, DS-to-CKSI(8)			1.4			ns
t_{H_DS}	Serial Port Hold Time, DS-to-CKS(8)			-250			ps
Deserializer AC Electrical Characteristics							
t_{RCOP}	Deserializer Clock Output (CKP OUT) Period(9)	See Figure 18		50.0	T	500	ns
t_{RCOL}	CKP OUT Low Time	See Figure 18 (Rising Edge STROBE)(9) Serializer source STROBE = CKREF		13a-3		13a+3	ns
t_{RCOH}	CKP OUT High Time			13a-3		13a+3	ns
t_{PDV}	Data Valid to CKP LOW	See Figure 18 (Rising Edge STROBE)		8a-6		8a+1	ns
t_{ROLH} (FIN224AC)	Output Rise Time (20% to 80%)	C_L = 8pF See Figure 15			18		ns
t_{ROHL} (FIN224AC)	Output Fall Time (20% to 80%)	C_L = 8pF See Figure 15			18		ns

Notes:

5. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into device and negative values means current flowing out of the pins. Voltages are referenced to GROUND unless otherwise specified (except DVOD and VOD).
6. Skew is measured from either the rising or falling edge of CKSO clock to the rising or falling edge of data (DSO). Signals are edge aligned. Both outputs should have identical load conditions for this test to be valid.
7. The power-down time is a function of the CKREF frequency prior to CKREF being stopped HIGH or LOW and the state of the S1/S2 mode pins. The specific number of clock cycles required for the PLL to be disabled varies dependent upon the operating mode of the device.
8. Signals are transmitted from the serializer source synchronously. Note that, in some cases, data is transmitted when the clock remains at a HIGH state. Skew should only be measured when data and clock are transitioning at the same time. Total measured input skew would be a combination of output skew from the serializer, load variations, and ISI and jitter effects.
9. **(a = (1/f)/13)** Rising edge of CKP appears approximately 13 bit times after the falling edge of the CKP output. Falling edge of CKP occurs approximately eight bit times after a data transition or six bit times after the falling edge of CKSO. Variation of the data with respect to the CKP signal is due to internal propagation delay differences of the data and CKP path and propagation delay differences on the various data pins. Note that if the CKREF is not equal to STROBE for the serializer, the CKP signal does not maintain a 50% duty cycle.The low time of CKP remains 13 bit times.

Control Logic Timing Controls

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI-to-$\overline{DIRO}$	DIRI LOW-to-HIGH or HIGH-to-LOW			17.0	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI-to-DP	DIRI LOW-to-HIGH			25.0	ns
t_{PZL}, t_{PZH}	Propagation Delay DIRI-to-DP	DIRI HIGH-to-LOW			25.0	ns
t_{PLZ}, t_{PHZ}	Deserializer Disable Time: S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 24			25.0	ns
t_{PZL}, t_{PZH}	Deserializer Enable Time: S0 or S1 to DP	DIRI = 0,(10) S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 24			2.0	µs
t_{PLZ}, t_{PHZ}	Serializer Disable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) = 0 and S2(1) = HIGH-to-LOW Figure 23			25.0	ns
t_{PZL}, t_{PZH}	Serializer Enable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) and S2(1) = LOW-to-HIGH Figure 23			65.0	ns

Notes:

10. Deserializer Enable Time includes the amount of time required for internal voltage and current references to stabilize. This time is significantly less than the PLL Lock Time and therefore does not limit overall system startup time.

Capacitance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Capacitance of Input Only Signals, CKREF, STROBE, S1, S2, DIRI	DIRI = 1, S1 = S2 = 0, V_{DD} = 2.5V		2.0		pF
C_{IO}	Capacitance of Parallel Port Pins $DP_{1:12}$	DIRI = 1, S1 = S2 = 0, V_{DD} = 2.5V		2.0		pF
$C_{IO-DIFF}$	Capacitance of Differential I/O Signals	DIRI = 0, S1 = S2 = 0, V_{DD} = 2.775V		2.0		pF

AC Loading and Waveforms

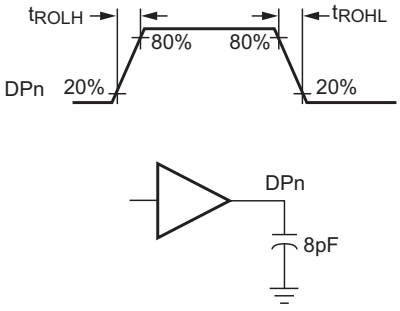
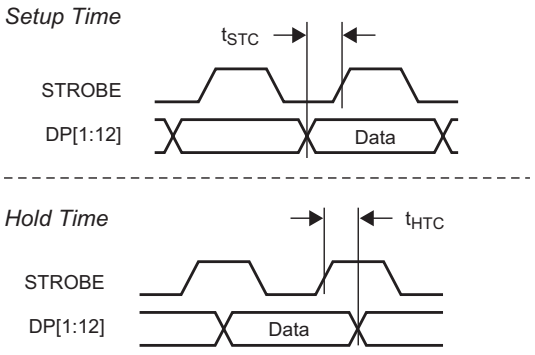


Figure 15. LVCMOS Output Load and Transition Times



Setup: MODE0 = “0” or “1”, MODE1 = “1”, SER/$\overline{DES}$ = “1”

Figure 16. Serial Setup and Hold Time

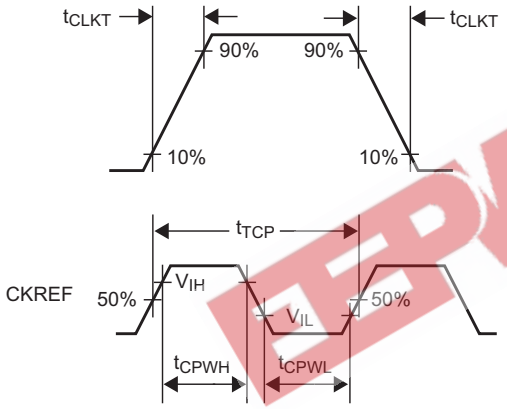
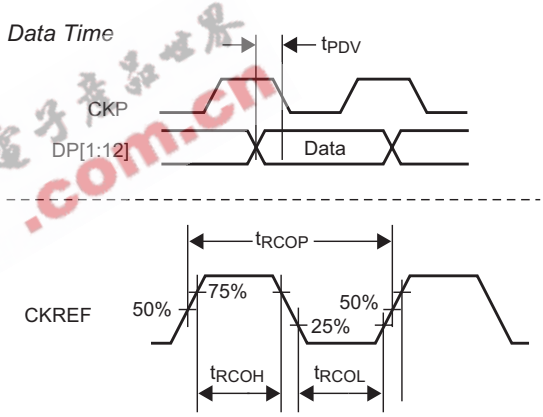
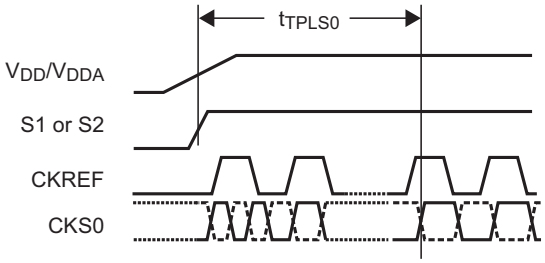


Figure 17. LVCMOS Clock Parameters



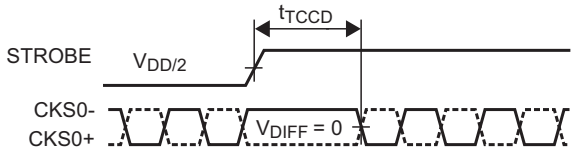
Setup: EN_DES = “1”, CKSI and DSI are valid signals

Figure 18. Deserializer Data Valid Window Time and Clock Output Parameters



Note: CKREF Signal is free running.

Figure 19. Serializer PLL Lock Time



Note: STROBE = CKREF

Figure 20. Serializer Clock Propagation Delay

AC Loading and Waveforms (Continued)

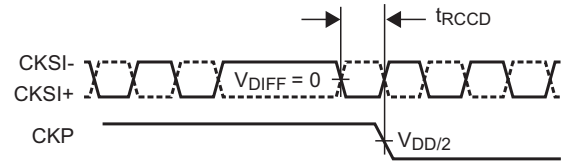
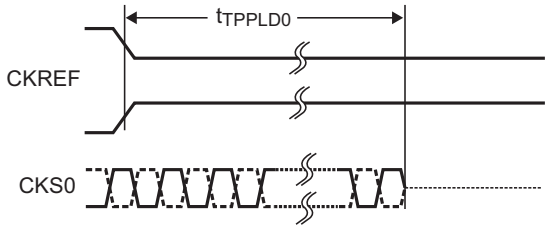


Figure 21. Deserializer Clock Propagation Delay



Note: CKREF Signal can be stopped either High or LOW

Figure 22. PLL Loss of Clock Disable Time

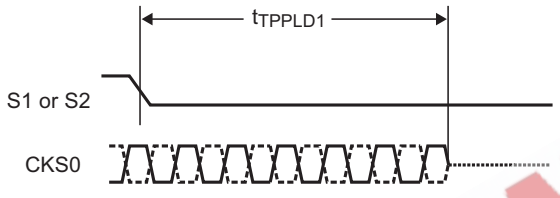
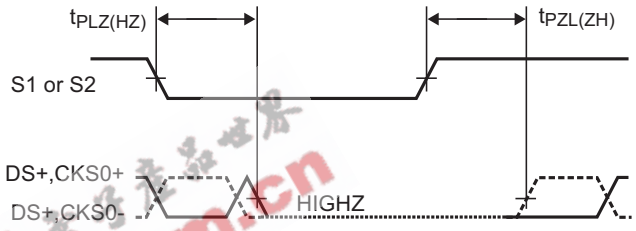
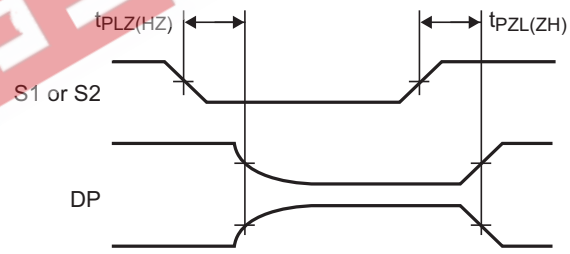


Figure 23. PLL Power-Down Time



Note: CKREF must be active and PLL must be stable

Figure 24. Serializer Enable and Disable Time



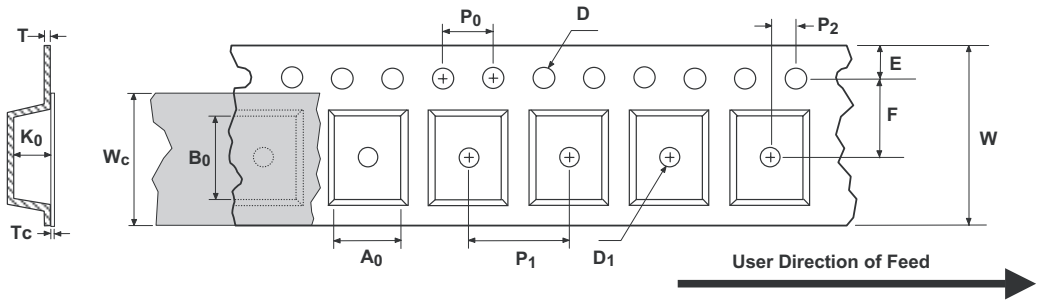
Note: If S1(2) transitioning then S2(1) must = 0 for test to be valid

Figure 25. Deserializer Enable and Disable Times

Tape and Reel Specification

BGA Embossed Tape Dimension

Dimensions are in millimeters.

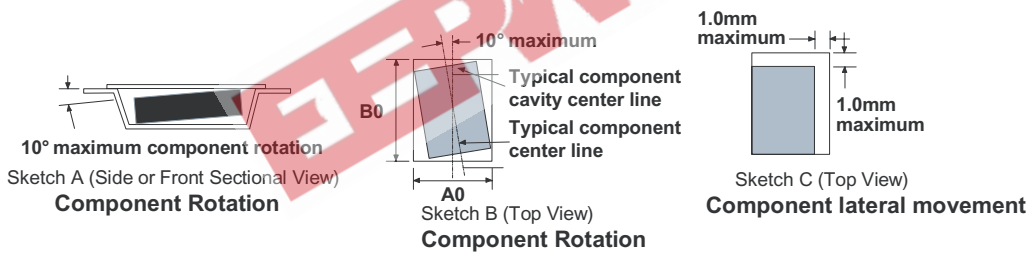


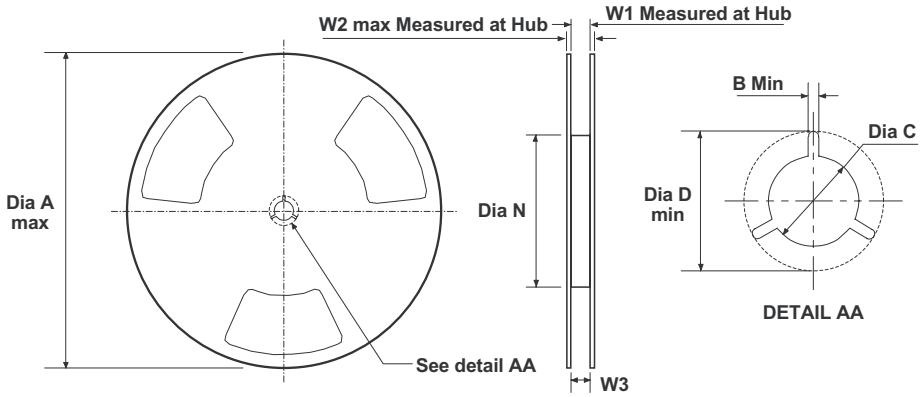
Package	A_0	B_0	D	D_1	E	F	K_0	P_1	P_0	P_2	T	T_C	W	W_C
3.5 x 4.5	TBD ±0.1	TBD ±0.1	1.55 ±0.05	1.5 Min.	1.75 ±0.1	5.5 ±0.1	1.1 ±0.1	8.0 Typ.	4.0 Typ.	2.0 ±0/05	0.3 Typ.	0.07 ±0.005	12.0 ±0.3	9.3 Typ.

Notes:
A0, B0, and K0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Shipping Reel Dimensions

Dimensions are in millimeters.



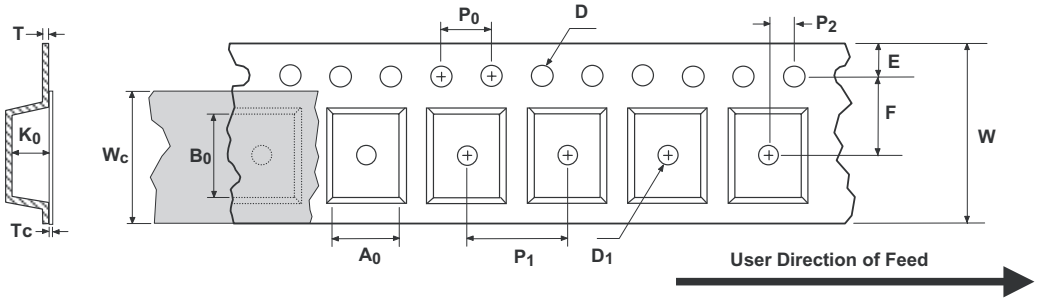


Tape Width	Dia A	Dim B	Dia C	Dia D	Dim N	Dim W1	Dim W2	Dim W3 (LSL–USL)
8	330 Max.	1.5 Min.	13.0 +0.5/–0.2	20.2 Min.	178 Min.	8.4 +2.0/–0	14.4 Max.	7.9 ~ 10.4
12							18.4 Max.	11.9 ~ 15.4
16							22.4 Max.	15.9 ~ 19.4

Tape and Reel Specification (Continued)

MLP Embossed Tape Dimension

Dimensions are in millimeters.

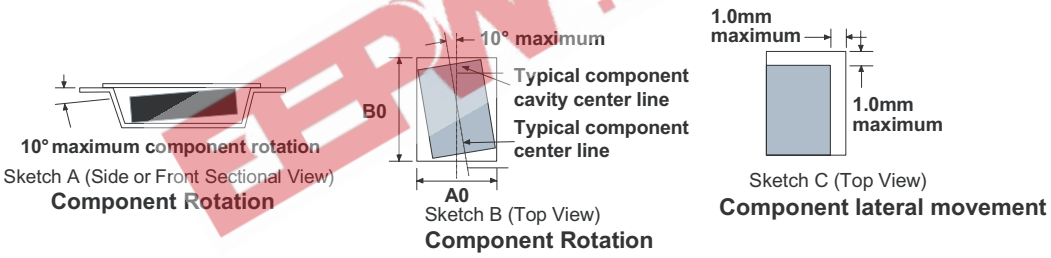


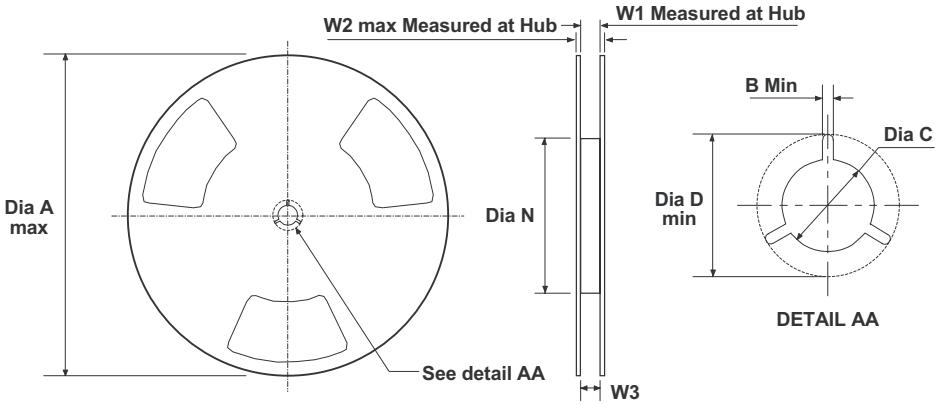
Package	A_0	B_0	D	D_1	E	F	K_0	P_1	P_0	P_2	T	T_C	W	W_C
5 x 5	5.35 ±0.1	5.35 ±0.1	1.55 ±0.05	1.5 Min.	1.75 ±0.1	5.5 ±0.1	1.4 ±0.1	8 Typ.	4 Typ.	2.0 ±0.05	0.3 Typ.	0.07 ±0.005	12 ±0.3	9.3 Typ.
6 x 6	6.30 ±0.1	6.30 ±0.1												

Notes:
Ao, Bo, and Ko dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Shipping Reel Dimension

Dimensions are in millimeters.

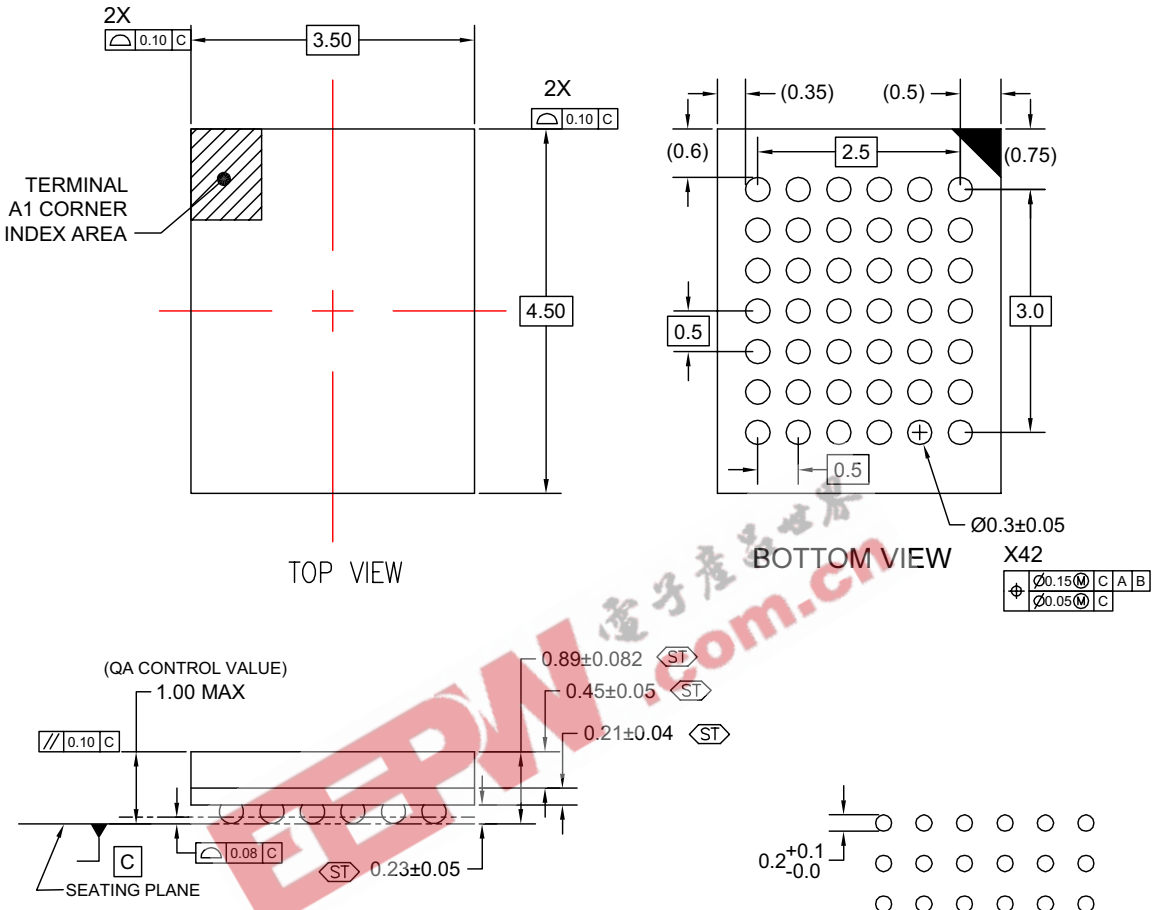




Tape Width	Dia A	Dim B	Dia C	Dia D	Dim N	Dim W1	Dim W2	Dim W3 (LSL–USL)
8	330 Max.	1.5 Min.	13.0 +0.5/–0.2	20.2 Min.	178 Min.	8.4 +2.0/–0	14.4 Max.	7.9 ~ 10.4
12							18.4 Max.	11.9 ~ 15.4
16							22.4 Max.	15.9 ~ 19.4

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

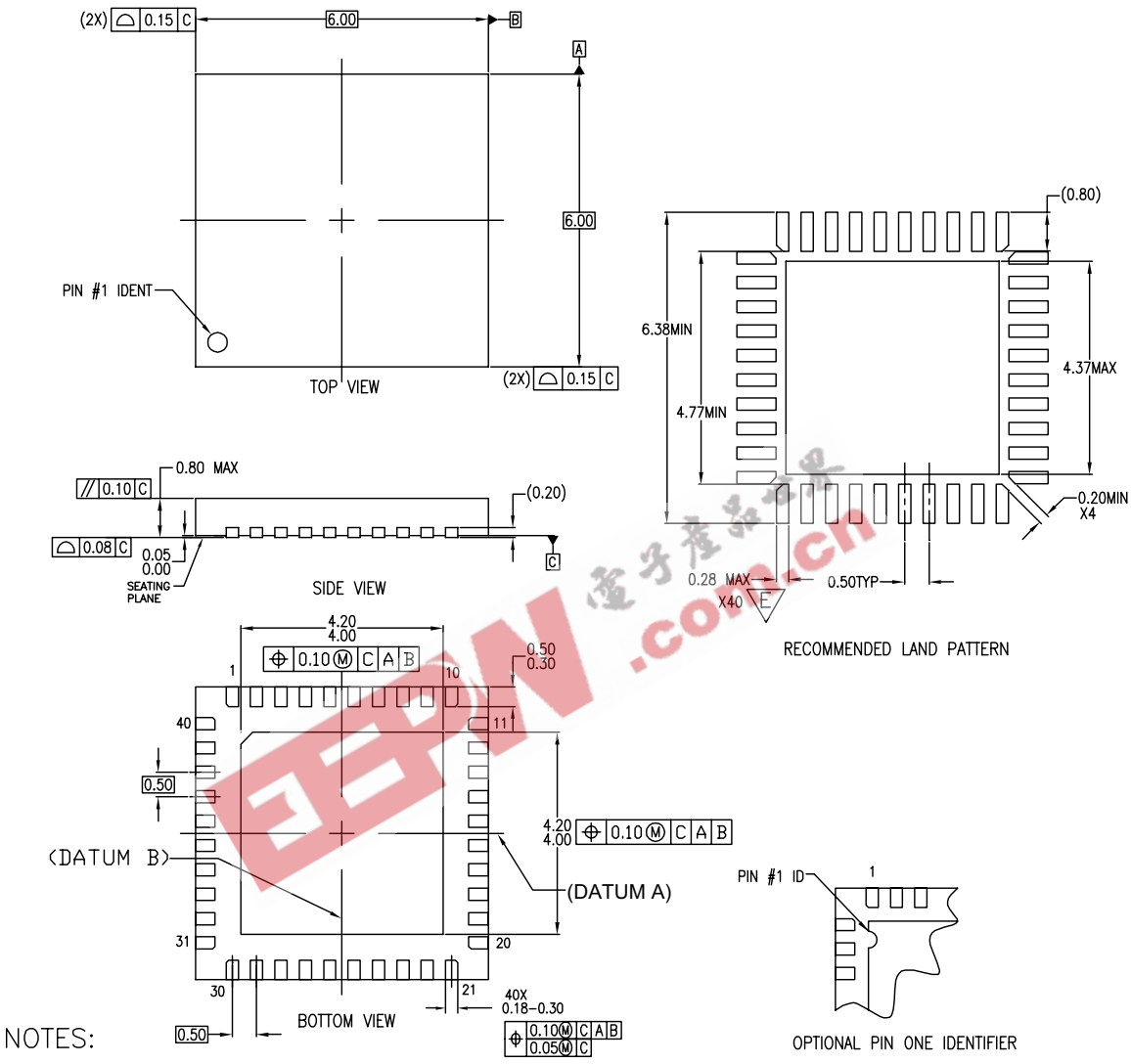
A. CONFORMS TO JEDEC REGISTRATION MO-195,
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. STATISTICAL TOLERANCING FOR REFERENCE REFER TO MAX DIMENSION FOR QA INSPECTION
E. LAND PATTERN RECOMENDATION PER IPC-7351 TABLE14-15 LAND PATTERN NAME PER TABLE 3-15: BGA50P+6X7-42

BGA42ArevB

Figure 26. Pb-Free 42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WJJD-2 WITH EXCEPTION THIS IS A SAWN VERSION.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER

D. LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

G. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, NOR TIE BAR PROTRUSIONS.

MLP40Arev2

Figure 27. Pb-Free 40-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square

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CROSSVOLT™	*i-Lo*™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
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E^2CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT™	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC™	
Programmable Active Droop™				

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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