FAIRCHILD SEMICONDUCTOR TM

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FDS6675

Single P-Channel, Logic Level, PowerTrench™ MOSFET

General Description

This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- -11 A, -30 V. $R_{DS(ON)}$ = 0.014 Ω @ V_{GS} = -10 V,
  $R_{DS(ON)}$ = 0.020 Ω @ V_{GS} = -4.5 V.
- Low gate charge (30nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
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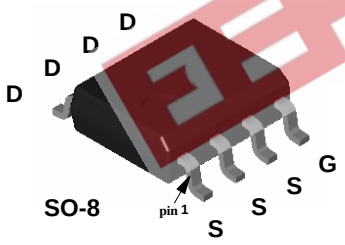
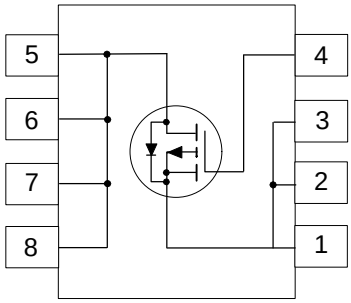




Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

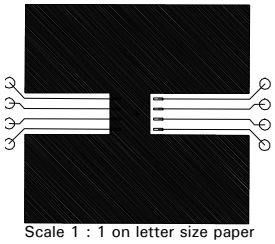
Symbol	Parameter		FDS6675	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	-11	A
	- Pulsed		-50	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

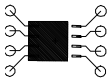
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		-22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.7	-3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		4.3		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -11 A		0.011	0.014	Ω
		T_J =125°C		0.016	0.023	
		V_{GS} = -4.5 V, I_D = -9 A		0.015	0.02	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-50			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -11 A		32		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		3000		pF
C_{oss}	Output Capacitance			870		pF
C_{rss}	Reverse Transfer Capacitance			360		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DS} = -15 V, I_D = -1 A		12	22	ns
t_r	Turn - On Rise Time	V_{GEN} = -10 V, R_{GEN} = 6 Ω		16	27	ns
$t_{D(off)}$	Turn - Off Delay Time			50	80	ns
t_f	Turn - Off Fall Time			100	140	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D = -11 A,		30	42	nC
Q_{gs}	Gate-Source Charge	V_{GS} = -5 V		9		nC
Q_{gd}	Gate-Drain Charge			11		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		-0.72	-1.2	V

Notes:

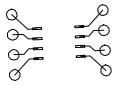
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W on a 1 in² pad of 2oz copper.



b. 105°C/W on a 0.04 in² pad of 2oz copper.



c. 125°C/W on a 0.006 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

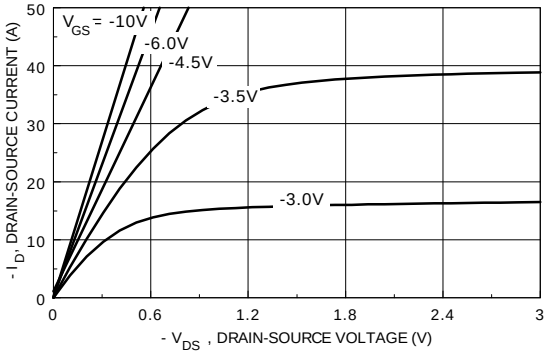


Figure 1. On-Region Characteristics.

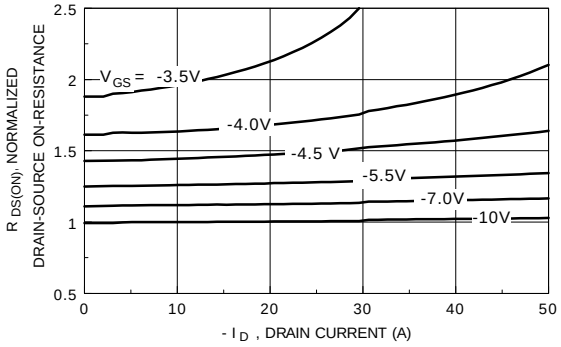


Figure 2. On-Resistance Variation with Dain Current and Gate Voltage.

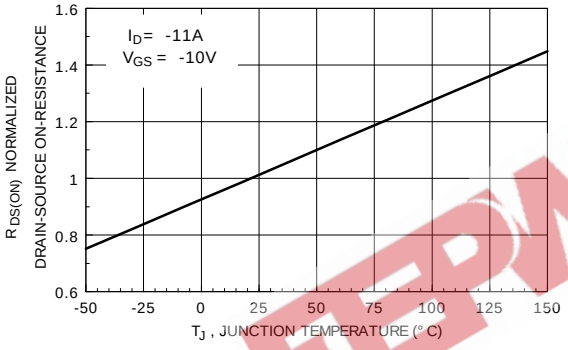


Figure 3. On-Resistance Variation with Temperature.

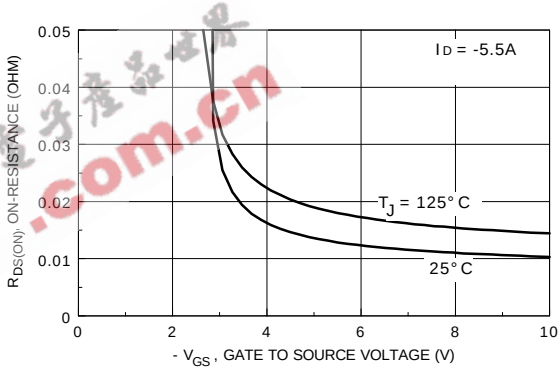


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

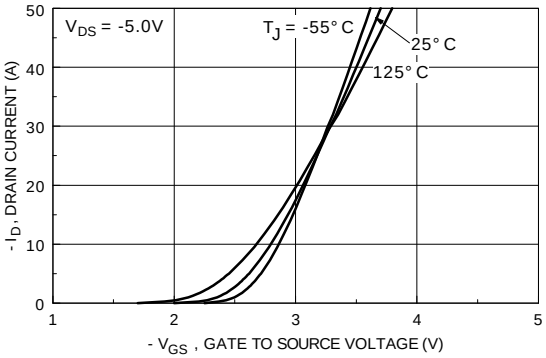


Figure 5. Transfer Characteristics.

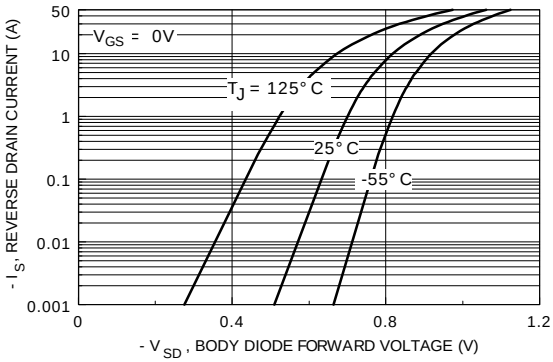


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

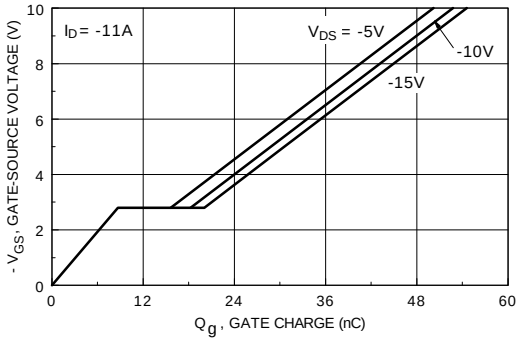


Figure 7. Gate Charge Characteristics.

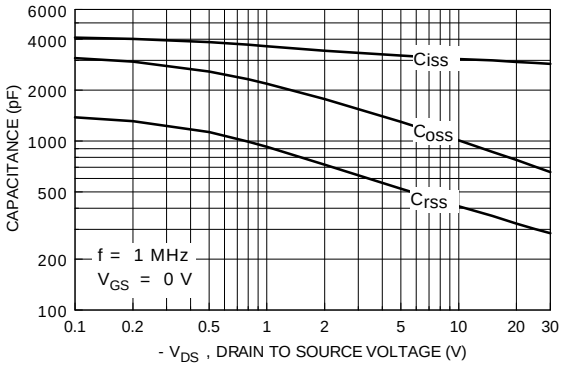


Figure 8. Capacitance Characteristics.

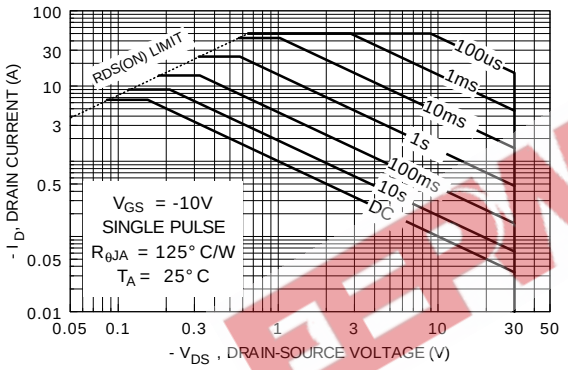


Figure 9. Maximum Safe Operating Area.

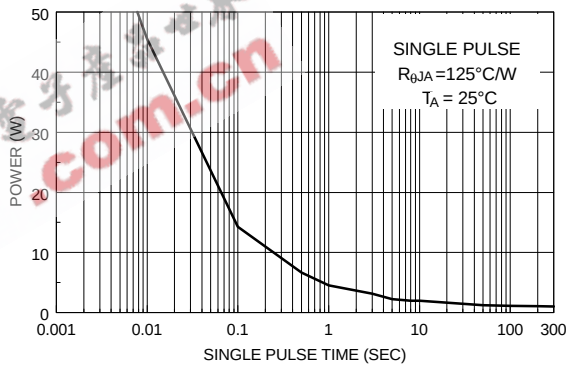


Figure 10. Single Pulse Maximum Power Dissipation.

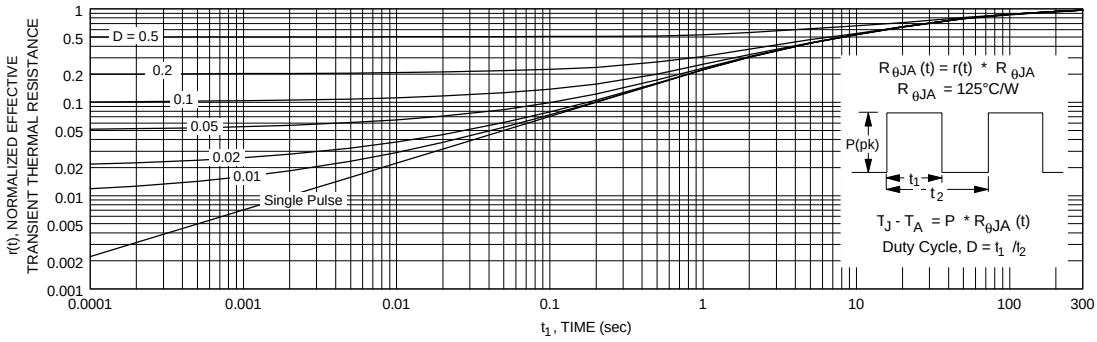


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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