National Semiconductor

August 1990

F100329
Low Power Octal ECL/TTL Bidirectional Translator with Register

General Description

The F100329 is an octal registered bidirectional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of the translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

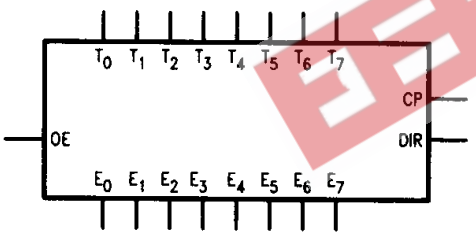
The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces the termination power and prevents loss of low state noise margin when several loads share the bus.

The F100329 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

Features

- Bidirectional translation
- ECL high impedance outputs
- Registered outputs
- FAST TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V

Logic Symbol



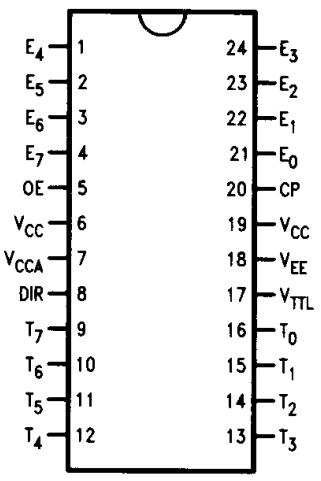
TL/F/10583–1

Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input (Active Rising Edge)
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

Connection Diagrams

24-Pin DIP



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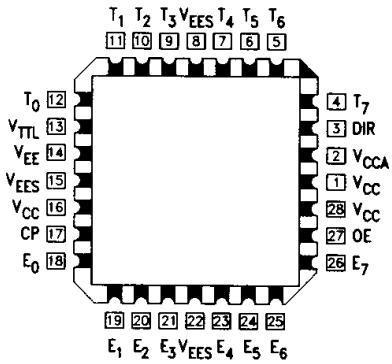
28-Pin PCC



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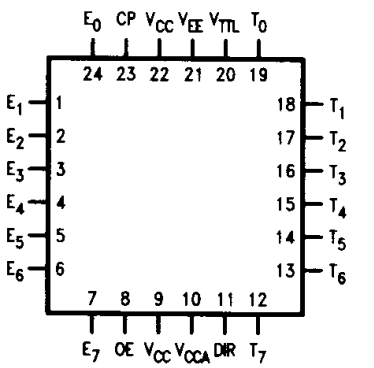
24-Pin Quad Cerpak



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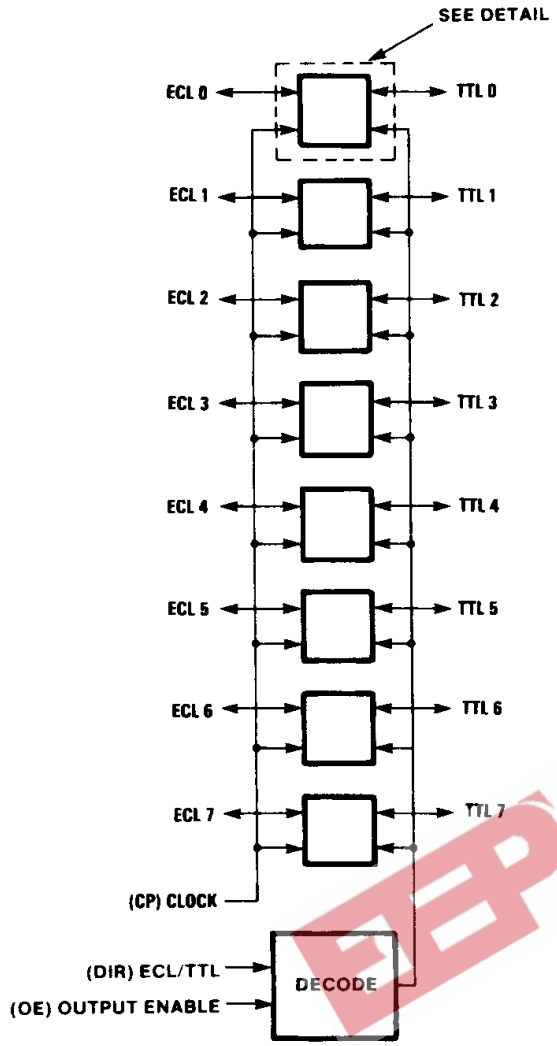
Functional Diagram



Note: DIR and OE use ECL logic levels

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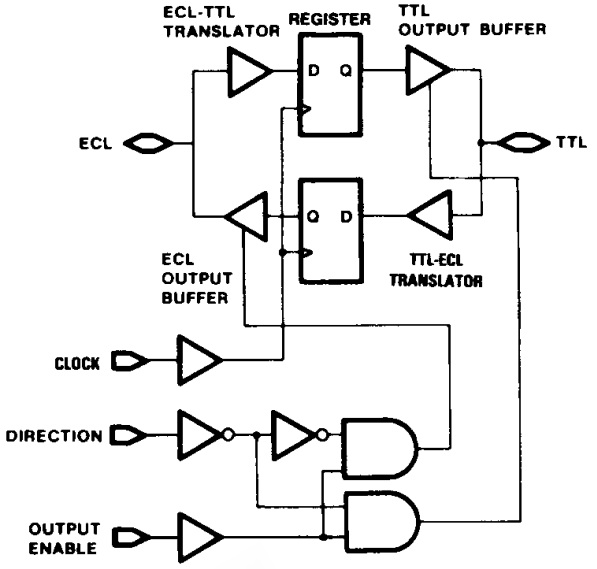
Detail



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Truth Table

OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	1, 3
L	H	X	LOW (Cut-Off)	Input	2, 3
H	L	⌐	L	L	1
H	L	⌐	H	H	1
H	L	L	X	NC	1, 3
H	H	⌐	L	L	2
H	H	⌐	H	H	2
H	H	L	NC	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition
NC = No Change

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before CP.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_j)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	+6.0V to −0.5V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 4)	−0.5V to +7.0V
TTL Input Current (Note 4)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	
Commercial	−5.7V to −4.2V
Military	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	
Commercial	+4.5V to +5.5V
Military	+4.5V to +5.5V

Commercial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min) Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	
	Cutoff Voltage		−2000	−1950	mV	OE or DIR LOW, V_{IN} = V_{IH} (Max) or V_{IL} (Min), Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point HIGH	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max) Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point LOW			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			70	μA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−189 −199		−94 −94	mA	LE LOW, OE and DIR HIGH Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

Commercial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output Low Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input High Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input Low Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input High Current			350	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input Low Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−700			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150		−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			74 49 67	mA mA mA	TTL Outputs Low TTL Outputs High TTL Outputs in TRI-STATE

Ceramic Dual-In-Line Package TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	350		350		350		MHz	
t_{PLH} t_{PHL}	CP to E_n	1.7	3.6	1.7	3.7	1.9	3.9	ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.3	4.2	1.5	4.4	1.7	4.8	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	*Figures 1 & 2*
t_{set}	T_n to CP	1.1		1.1		1.1		ns	*Figures 1 & 2*
t_{hold}	T_n to CP	2.1		2.1		2.1		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width CP	2.1		2.1		2.1		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

Commercial Version (Continued)

Ceramic Dual-In-Line Package ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	125		125		125		MHz	
t_{PLH} t_{PHL}	CP to T_n	3.1	7.2	3.1	7.2	3.3	7.7	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	*Figures 3 & 6*
t_{set}	E_n to CP	1.1		1.1		1.1		ns	*Figures 3 & 4*
t_{hold}	E_n to CP	2.1		2.1		2.6		ns	*Figures 3 & 4*
t_{pw}(H)	Pulse Width CP	4.1		4.1		4.1		ns	*Figures 3 & 4*

PCC and Cerpak TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	350		350		350		MHz	
t_{PLH} t_{PHL}	CP to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.3	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1 & 2*
t_{set}	T_n to CP	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to CP	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width CP	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

Commercial Version (Continued)

PCC and Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	125		125		125		MHz	
t_{PLH} t_{PHL}	CP to T_n	3.1	7.0	3.1	7.0	3.3	7.5	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3 & 6*
t_{set}	E_n to CP	1.0		1.0		1.0		ns	*Figures 3 & 4*
t_{hold}	E_n to CP	2.0		2.0		2.5		ns	*Figures 3 & 4*
t_{pw}(H)	Pulse Width CP	4.0		4.0		4.0		ns	*Figures 3 & 4*

Military Version-Preliminary

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR LOW		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
I_{IH}	Input HIGH Current		70	μA	−55°C to +125°C	V_{IN} = +2.7V		1, 2, 3
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125°C	I_{IN} = −18 mA		1, 2, 3
I_{EE}	V_{EE} Supply Current	−210 −220	−70 −70	mA	−55°C to +125°C	LE LOW, OE and DIR HIGH Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Military Version-Preliminary (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5 2.4		mV	−55°C to +125°C	I_{OH} = −1 mA, V_{TTL} = 4.50V I_{OH} = −3 mA, V_{TTL} = 4.50V	1, 2, 3
V_{OL}	Output LOW Voltage		0.5	mV	−55°C to +125°C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current		350	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)	1, 2, 3
			500	μA	−55°C		
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)	1, 2, 3
I_{OZHT}	TRI-STATE Current Output High		70	μA	−55°C to +125°C	V_{OUT} = +2.7V	1, 2, 3
I_{OZLT}	TRI-STATE Current Output Low		−1.0	mA	−55°C to +125°C	V_{OUT} = +0.5V	1, 2, 3
I_{OS}	Output Short-Circuit Current	−150	−60	mA	−55°C to +125°C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	1, 2, 3
I_{TTL}	V_{TTL} Supply Current		75 50 70	mA mA mA	−55°C to +125°C	TTL Outputs Low TTL Outputs High TTL Outputs in TRI-STATE	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version-Preliminary (Continued)

Ceramic Dual-In-Line Package TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Toggle Frequency	250		250		250		MHz		4
t_{PLH} t_{PHL}	CP to E_n	1.3	3.8	1.6	3.7	1.9	4.3	ns	*Figures 1 & 2*	1, 2, 3
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.0	4.3	1.5	4.4	1.7	5.1	ns	*Figures 1 & 2*	
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	5.0	1.6	4.5	1.6	5.0	ns	*Figures 1 & 2*	
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.7	ns	*Figures 1 & 2*	
t_{set}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	4
t_{hold}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{pw}(H)	Pulse Width CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1 & 2*	

Ceramic Dual-In-Line Package ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Toggle Frequency	200		200		100		MHz		4
t_{PLH} t_{PHL}	CP to T_n	3.1	8.0	3.1	7.3	3.3	8.0	ns	*Figures 3 & 4*	1, 2, 3
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.7	9.1 9.5	3.7 4.0	9.0 9.3	4.0 4.3	10.1 10.4	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	10.0 9.8	3.3 3.4	9.0 8.8	3.5 4.1	9.3 10.4	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	9.5 8.7	2.8 3.1	8.8 8.0	3.0 4.0	9.0 9.6	ns	*Figures 3 & 6*	
t_{set}	E_n to CP	2.5		2.0		2.5		ns	*Figures 3 & 4*	4
t_{hold}	E_n to CP	3.0		2.5		3.0		ns	*Figures 3 & 4*	
t_{pw}(H)	Pulse Width CP	2.5		2.5		5.0		ns	*Figures 3 & 4*	

Military Verison-Preliminary (Continued)

Cerpak TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Toggle Frequency	250		250		250		MHz		4
t_{PLH} t_{PHL}	CP to E_n	1.3	3.8	1.6	3.7	1.9	4.3	ns	*Figures 1 & 2*	1, 2, 3
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.0	4.3	1.5	4.4	1.7	5.1	ns	*Figures 1 & 2*	
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	5.0	1.6	4.5	1.6	5.0	ns	*Figures 1 & 2*	
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.7	ns	*Figures 1 & 2*	
t_{set}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	4
t_{hold}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{pw}(H)	Pulse Width CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1 & 2*	

Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Toggle Frequency	200		200		100		MHz		4
t_{PLH} t_{PHL}	CP to T_n	3.1	8.0	3.1	7.3	3.3	8.0	ns	*Figures 3 & 4*	1, 2, 3
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.7	9.1 9.5	3.7 4.0	9.0 9.3	4.0 4.3	10.1 10.4	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	10.0 9.8	3.3 3.4	9.0 8.8	3.5 4.1	9.3 10.4	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	9.5 8.7	2.8 3.1	8.8 8.0	3.0 4.0	9.0 9.6	ns	*Figures 3 & 6*	
t_{set}	E_n to CP	2.5		2.0		2.5		ns	*Figures 3 & 4*	4
t_{hold}	E_n to CP	3.0		2.5		3.0		ns	*Figures 3 & 4*	
t_{pw}(H)	Pulse Width CP	2.5		2.5		5.0		ns	*Figures 3 & 4*	

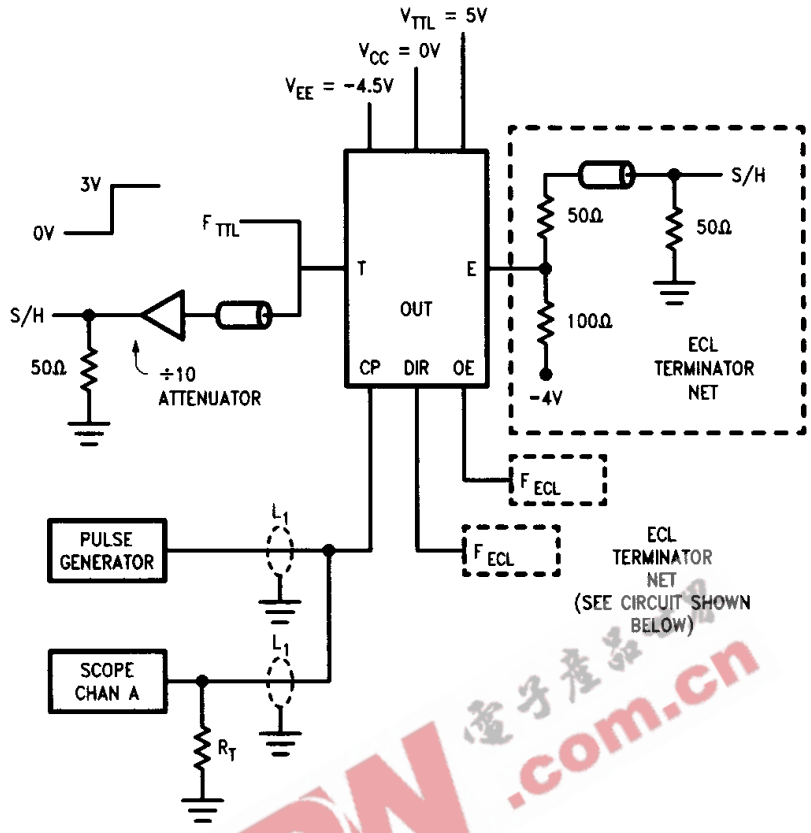
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature latched only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuitry



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R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines

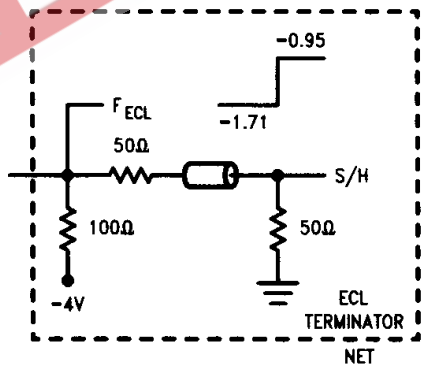

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FIGURE 1. TTL to ECL AC Test Circuit

Switching Waveforms

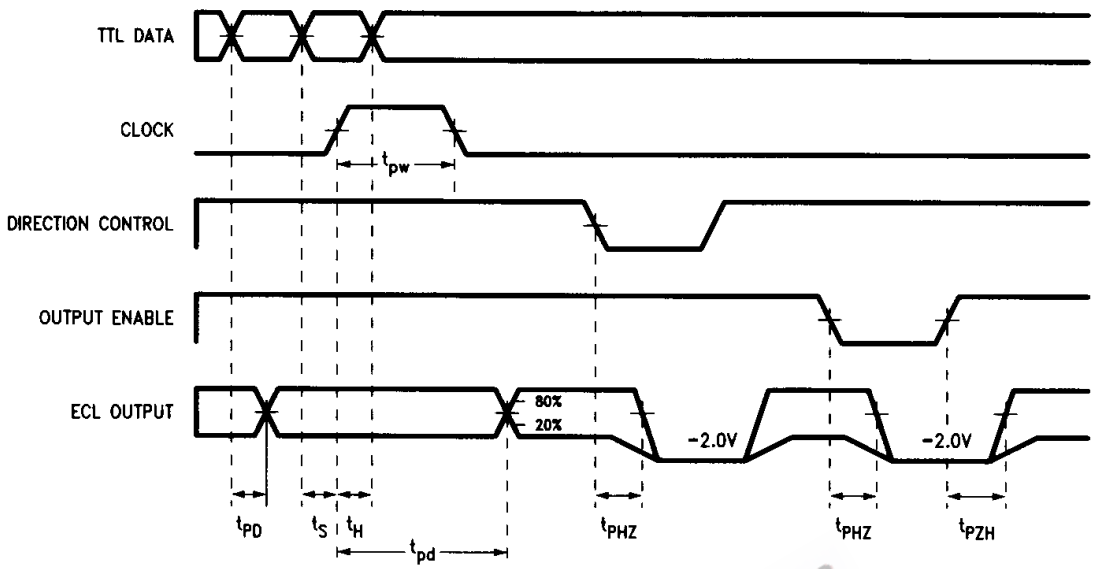

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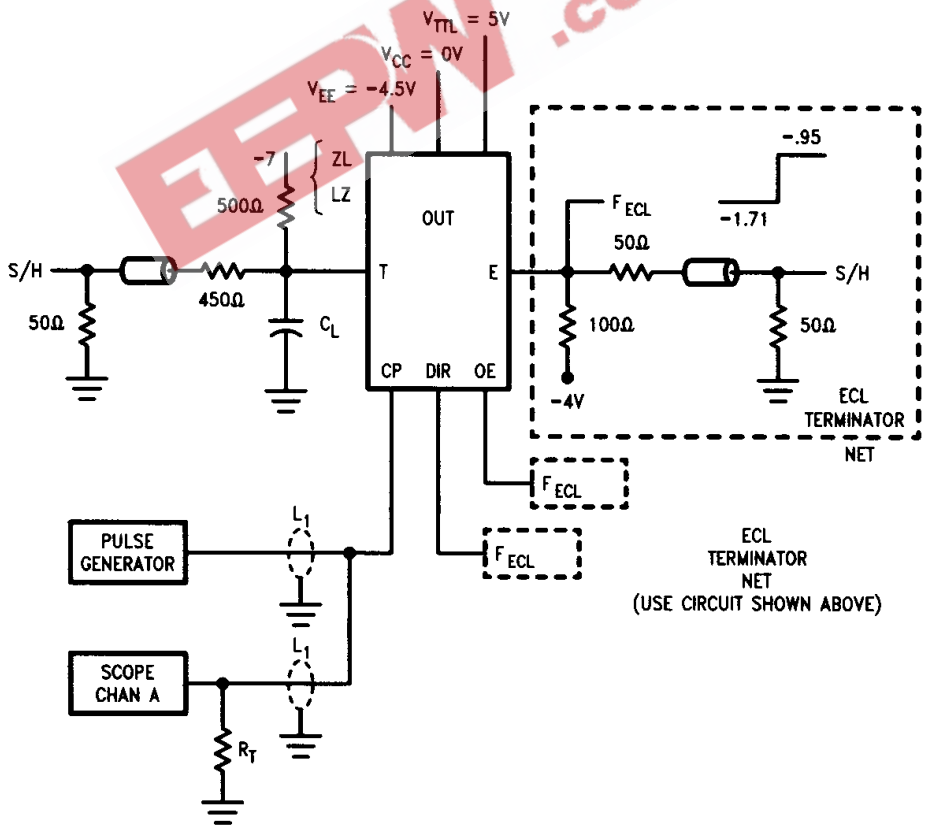
FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuit



TL/F/10583–10

R_T = 50Ω termination of scope

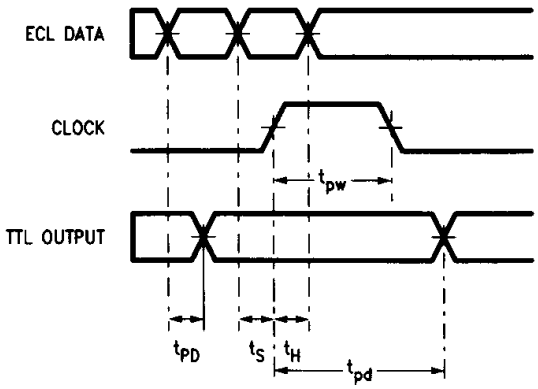
L_1 = 50Ω impedance lines

C_L = 50 pF including stray and jig capacitance.

Note: 50Ω to ground termination must be included on ECL I/O pins not monitored by a 50Ω scope to prevent oscillatory feedback.

FIGURE 3. ECL-to-TTL AC Test Circuit

Switching Waveforms



Note: DIR is LOW, OE is HIGH

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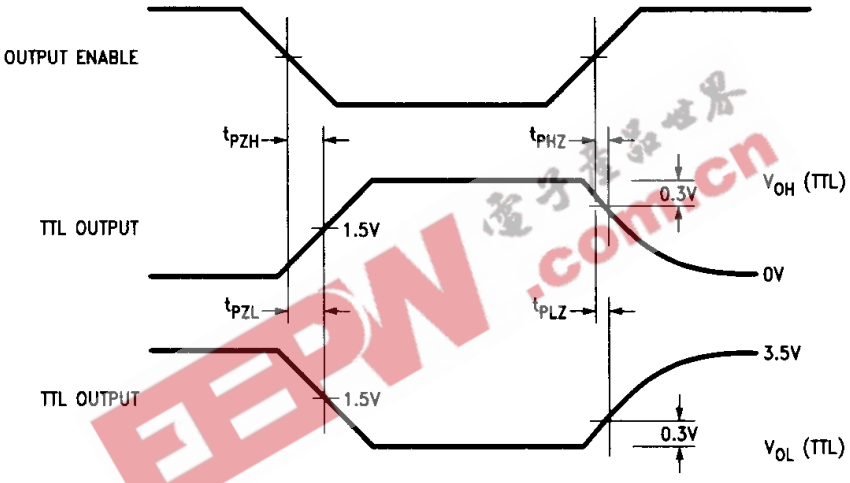
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



Note: DIR is LOW

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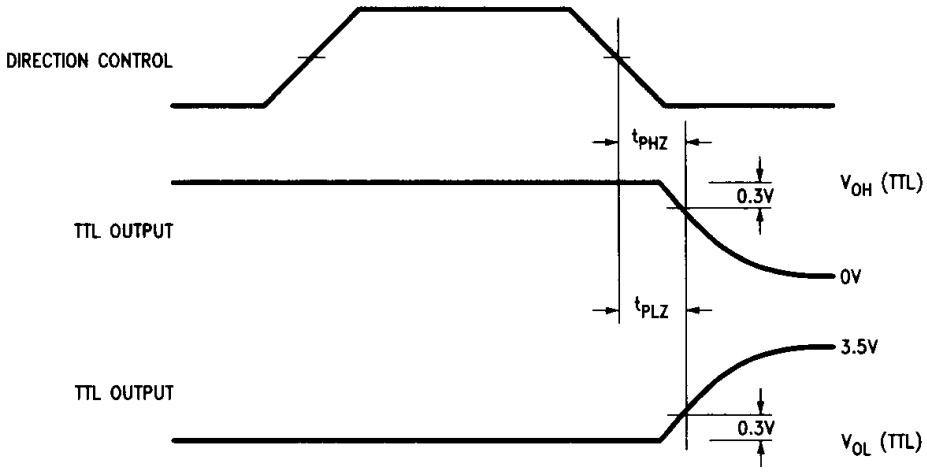
FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times



Note: OE is HIGH

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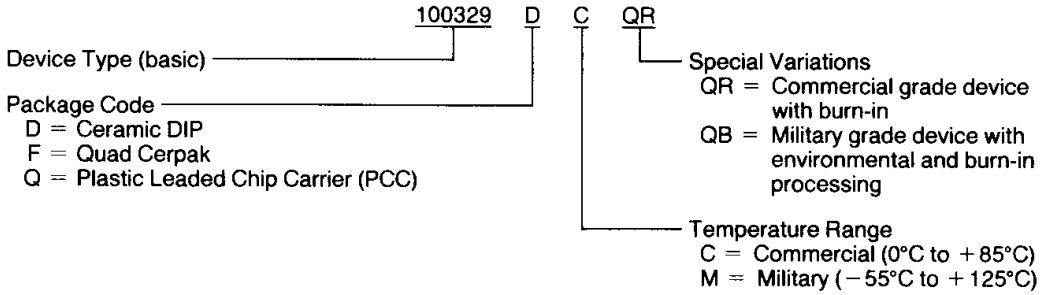
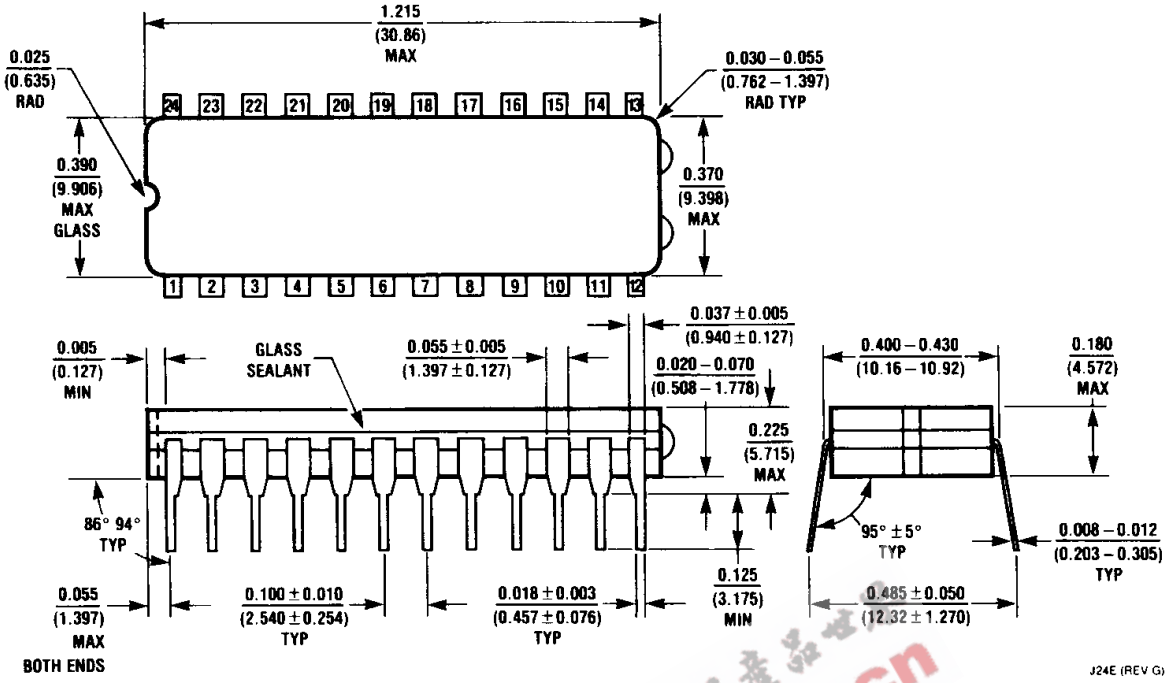
FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

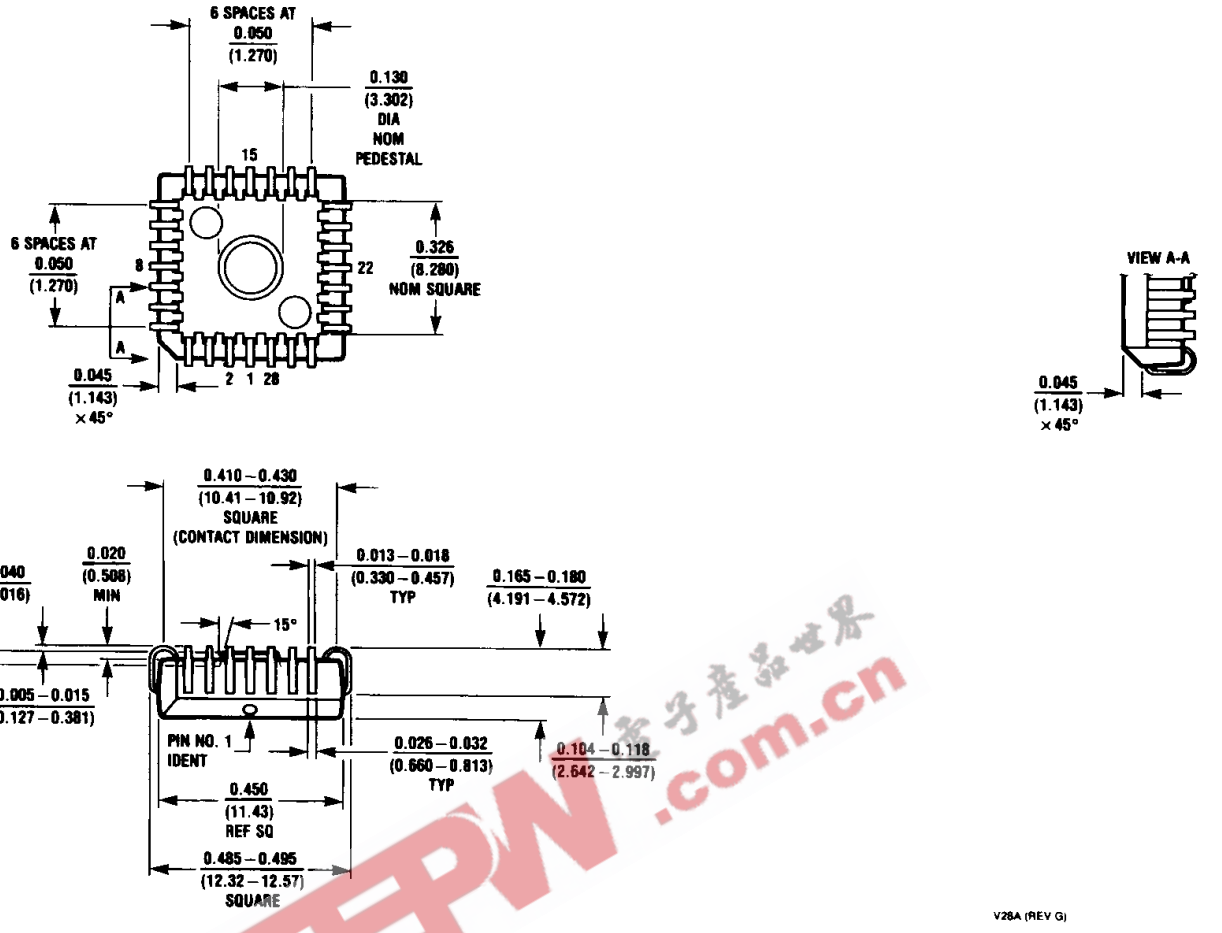


Physical Dimensions inches (millimeters)



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E

Physical Dimensions inches (millimeters) (Continued)

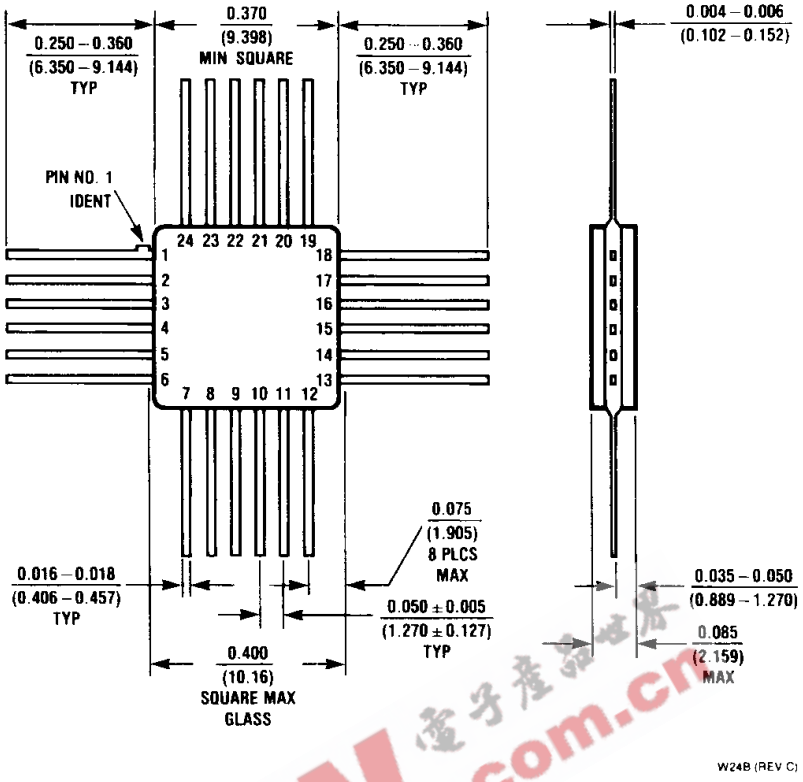


Note: Pedestal as shown on base is not available for F1000K ECL products

28-Lead Plastic Chip Carrier (Q)
NS Package Number V28A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114910



24-Lead Quad Cerpak (F)
NS Package Number W24B

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-299-7001
FAX: 3-299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semicondutores Do Brasil Ltda.
Av. Brig. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Fax: (55/11) 211-1181 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victory, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458