National Semiconductor

F100135
Triple J-K Flip-Flop

General Description

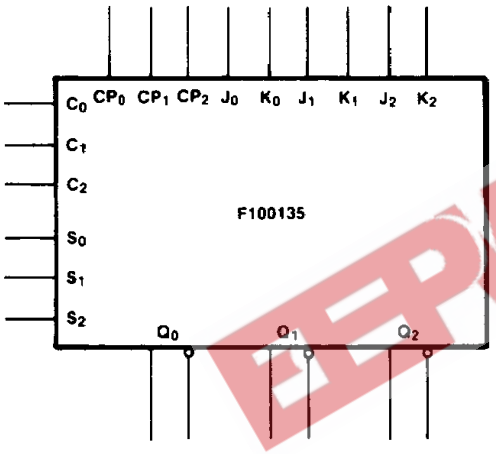
The F100135 contains three J-K, edge-triggered master-slave flip-flops with true and complement outputs. All have individual Clock (CP_n), Clear (C_n), and Set (S_n) inputs. Clocking occurs on the rising edge of CP_n. All inputs have 50 kΩ pull-down resistors.

Features

- Toggle frequency 750 MHz Typical
- Propagation delay 2.2 ns max
- Outputs specified to drive a 50Ω load

Ordering Code: See Section 8

Logic Symbol



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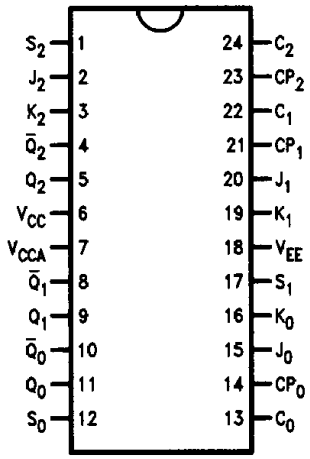
Pin Names	Description
J_0–J_2	J Inputs
K_0–K_2	K Inputs
S_0–S_2	Direct Set Inputs
C_0–C_2	Direct Clear Inputs
CP_0–CP_2	Clock Inputs
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



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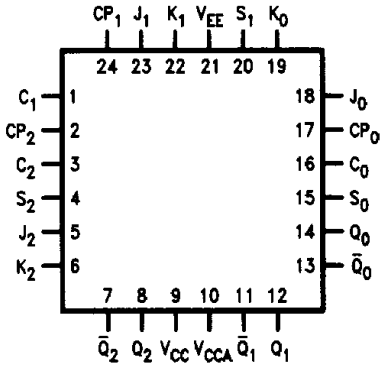
24-Pin Quad Cerpak



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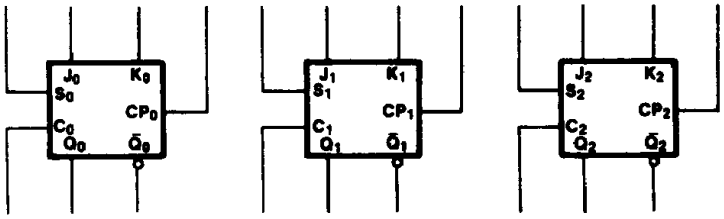
Logic Diagram



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Truth Tables (Each Flip-Flop)

Synchronous Operation

Inputs					Outputs
J_n	K_n	CP_n	S_n	C_n	$Q_n(t+1)$
L	L	⌐	L	L	$Q_n(t)$
L	H	⌐	L	L	L
H	L	⌐	L	L	H
H	H	⌐	L	L	$\overline{Q_n(t)}$
X	X	H	L	L	$Q_n(t)$
X	X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs					Outputs
J_n	K_n	CP_n	S_n	C_n	Q_n
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t + 1 = Time after CP Positive Transition
⌐ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−195	−150	−90	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

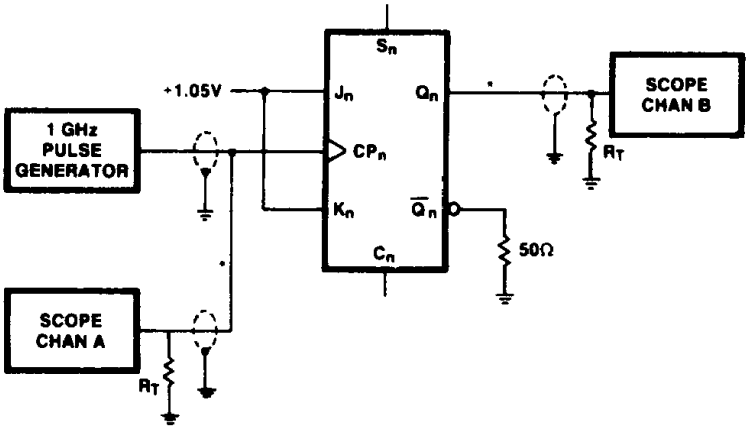
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	600		600		600		MHz	*Figure 1*
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.20	0.70	2.00	0.70	2.20	ns	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay C_n, S_n to Output	0.90	1.80	0.90	2.00	0.90	2.40	ns	CP_n = L, CP_n = H
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.40	0.30	1.40	0.30	1.40	ns	
t_S	Setup Time J_n, K_n to CP_n C_n, S_n (Release Time)	0.90 1.50		0.70 1.30		0.90 1.50		ns	*Figures 2* and *3*
t_H	Hold Time J_n, K_n to CP_n	0.80		0.80		0.80		ns	
$t_{pw}(H)$	Pulse Width HIGH CP_n, C_n, S_n	2.00		2.00		2.00		ns	

Cerpak AC Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	650		650		650		MHz	*Figure 1*
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.00	0.70	1.80	0.70	2.00	ns	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay C_n, S_n to Output	0.90	1.60	0.90	1.80	0.90	2.20	ns	CP_n = L, CP_n = H
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.30	0.30	1.30	0.30	1.30	ns	
t_S	Setup Time J_n, K_n to CP_n C_n, S_n (Release Time)	0.80 1.40		0.60 1.20		0.80 1.40		ns	*Figures 2* and *3*
t_H	Hold Time J_n, K_n to CP_n	0.70		0.70		0.70		ns	
$t_{pw}(H)$	Pulse Width HIGH CP_n, C_n, S_n	2.00		2.00		2.00		ns	



Notes:
$V_{CC} = V_{CCA} = +2V$
$V_{EE} = -2.5V$
* = equal electrical length 50Ω lines
$R_T = 50\Omega$ termination
Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Load all unused outputs with 50Ω to GND
Set pulse generator output level for 740 mV p-p at a frequency of 10 MHz as measured at the clock input pin of the device under test. Do not readjust this voltage for frequencies up to f_{max}. The pad isolates the generator output for D.U.T. input impedance variations. Signal voltage measured at the D.U.T. input will vary as input impedance varies with frequency.

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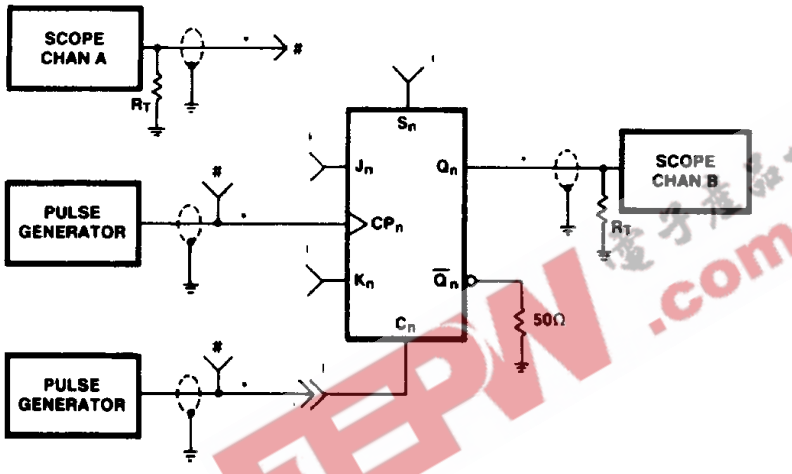
FIGURE 1. Toggle Frequency Test Circuit



Notes:
$V_{CC} = V_{CCA} = +2V$
$V_{EE} = -2.5V$
Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND
$R_T = 50\Omega$ termination
Load all unused outputs with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
* = equal electrical length 50Ω lines
# = Connect Scope CHAN A to pulse generator as required
† = Connect pulse generator to input under test; else connect input to voltage source set to +1.05 volts for logic HIGH or +0.31 volts for logic LOW
Consult truth table for appropriate logical condition

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FIGURE 2. AC Test Circuit

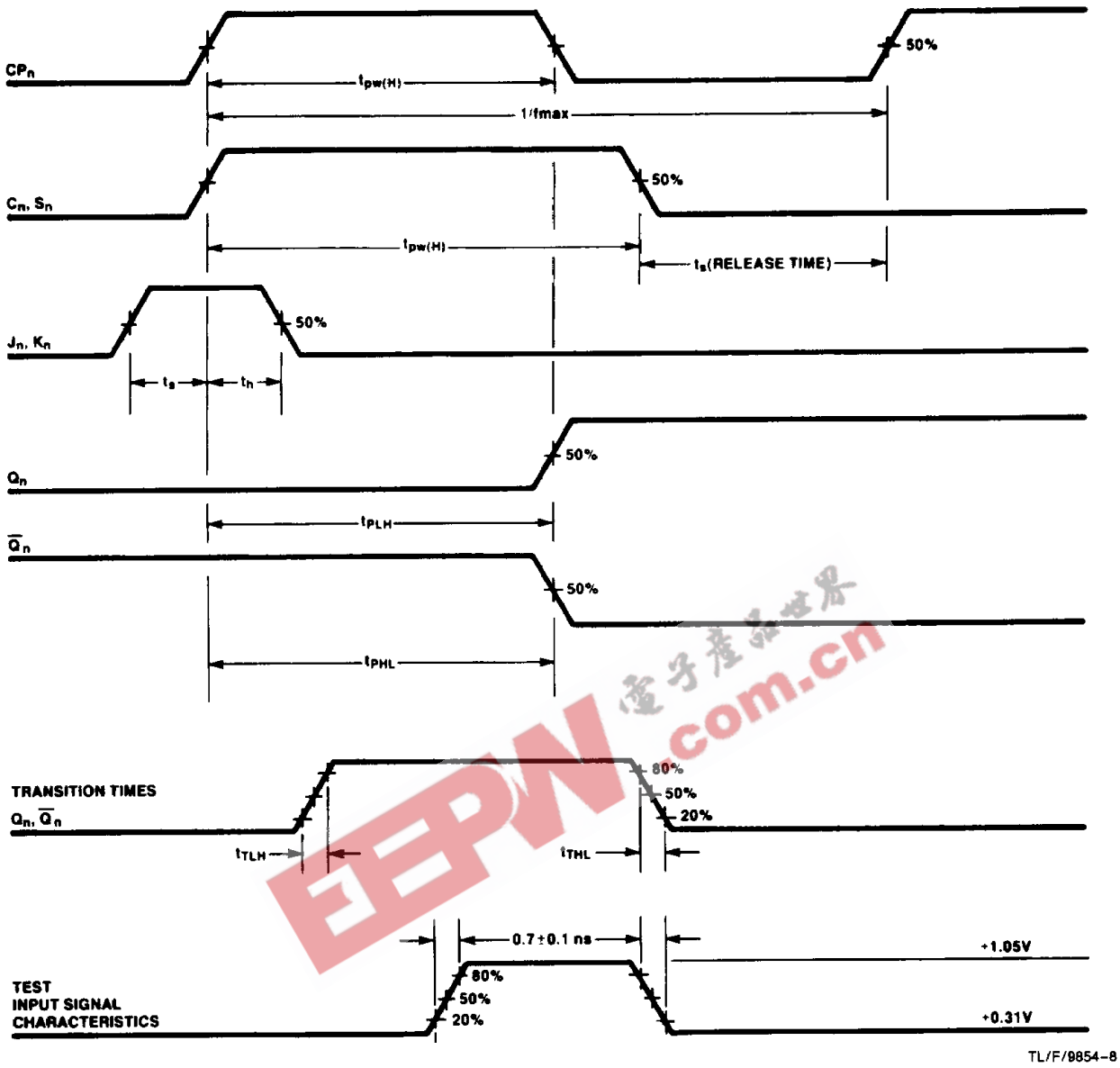

FIGURE 3. Propagation Delays and Setup and Hold Time