

July 1999

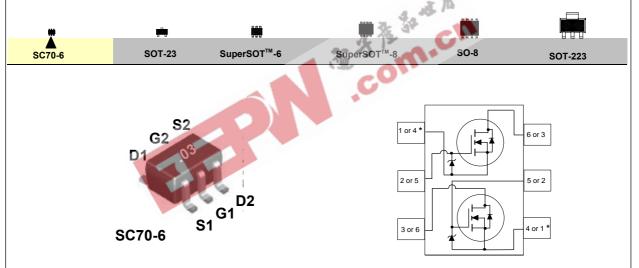
FDG6303N Dual N-Channel, Digital FET

General Description

These dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs.

Features

- $\label{eq:rescaled} \begin{array}{c} \bullet & 25 \text{ V}, \, 0.50 \text{ A continuous}, \, 1.5 \text{ A peak}. \\ & \mathsf{R}_{\mathsf{DS(ON)}} = 0.45 \ \Omega \ @ \ \mathsf{V}_{\mathsf{GS}} = 4.5 \text{ V}, \\ & \mathsf{R}_{\mathsf{DS(ON)}} = 0.60 \ \Omega \ @ \ \mathsf{V}_{\mathsf{GS}} = 2.7 \text{ V}. \end{array}$
- Very low level gate drive requirements allowing direct operation in 3 V circuits (V_{GS(th)} < 1.5 V).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.



 $\ensuremath{^*}$ The pinouts are symmetrical; pin 1 and 4 are interchangeable.

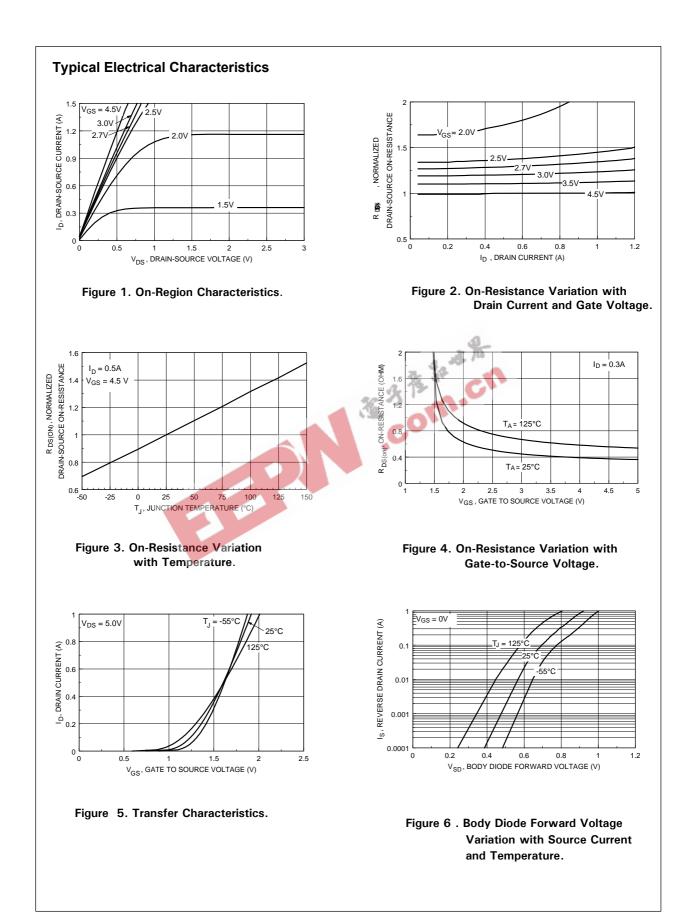
Units inside the carrier can be of either orientation and will not affect the functionality of the device.

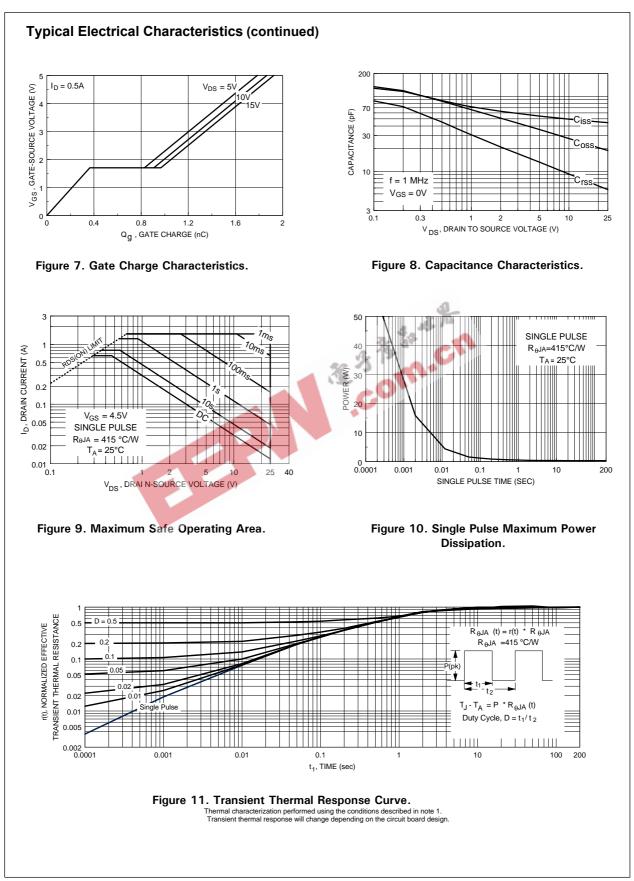
Absolute Maximum Ratings $T_A = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	FDG6303N	Units
V _{DSS}	Drain-Source Voltage	25	V
V _{GSS}	Gate-Source Voltage	8	V
I _D	Drain/Output Current - Continuous	0.5	А
	- Pulsed	1.5	
P _D	Maximum Power Dissipation (Note 1)	0.3	W
T_,,T _{stg}	Operating and Storage Temperature Range	-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100 pF / 1500 Ω)	6.0	kV
THERMA	L CHARACTERISTICS		·
R _{eja}	Thermal Resistance, Junction-to-Ambient	415	°C/W

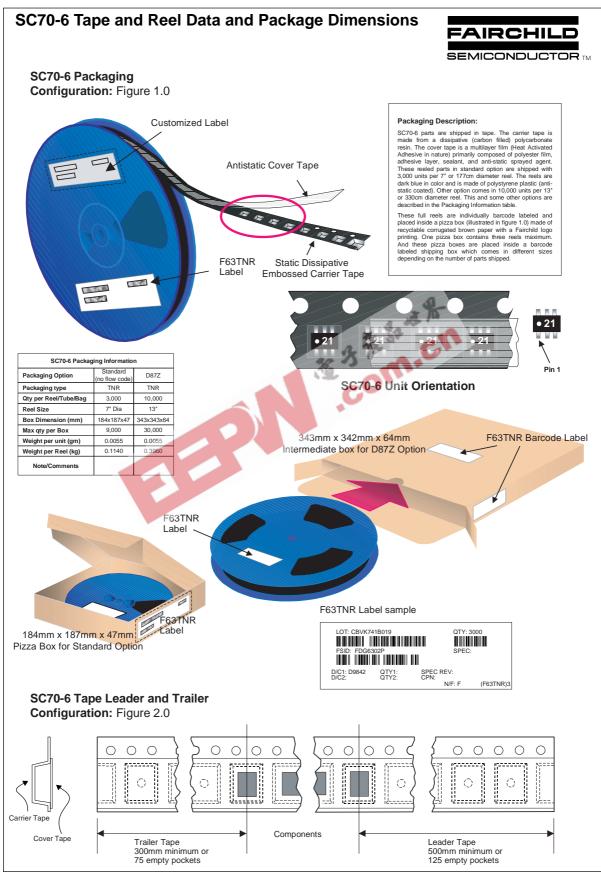
Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHAR	ACTERISTICS	•		1		1
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 V, I_{D} = 250 \mu A$	25			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	$I_{D} = 250 \ \mu\text{A}$, Referenced to 25°C		26		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$				1	μA
		$T_{J} = 55^{\circ}C$			10	μA
I _{GSS}	Gate - Body Leakage Current	$V_{GS} = 8 V, V_{DS} = 0 V$			100	nA
ON CHARAC	TERISTICS (Note 2)			•		•
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.65	0.8	1.5	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temp.Coefficient	$I_D = 250 \ \mu$ A, Referenced to 25° C		-2.6		mV/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_{D} = 0.5 \text{ A}$		0.34	0.45	Ω
		T _J =125°C		0.55	0.77	
		$V_{GS} = 2.7 \text{ V}, I_{D} = 0.2 \text{ A}$		0.44	0.6	
I _{D(ON)}	On-State Drain Current	$V_{GS} = 2.7 \text{ V}, V_{DS} = 5 \text{ V}$	0.5			А
9 _{FS}	Forward Transconductance	$V_{DS} = 5 V, I_{D} = 0.5 A$	-	1.45		S
DYNAMIC CI	HARACTERISTICS	4.15 10				_
C _{iss}	Input Capacitance	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$ f = 1.0 MHz		50		pF
C _{oss}	Output Capacitance	f = 1.0 MHZ		28		pF
C _{rss}	Reverse Transfer Capacitance			9		pF
SWITCHING	CHARACTERISTICS (Note 2)		T	1		
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 5 V, I_D = 0.5 A,$		3	6	ns
t _r	Turn - On Rise Time	$V_{GS} = 4.5 \text{ V}, \text{ R}_{GEN} = 50 \Omega$		8.5	18	ns
t _{D(off)}	Turn - Off Delay Time			17	30	ns
t _r	Turn - Off Fall Time			13	25	ns
Q _g	Total Gate Charge	$V_{DS} = 5 V, I_{D} = 0.5 A,$ $V_{GS} = 4.5 V$		1.64	2.3	nC
Q _{gs}	Gate-Source Charge	$v_{GS} = 4.3 v$		0.38		nC
Q_{gd}	Gate-Drain Charge			0.45		nC
DRAIN-SOU	RCE DIODE CHARACTERISTICS AND MAXIMI	UM RATINGS	1	1		1
l _s	Maximum Continuous Source Current				0.25	A
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \ I_{S} = 0.25 \text{ A} \text{ (Note 2)}$		0.8	1.2	V

R_{pub} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{pub} is guaranteed by design while R_{pub} is determined by the user's board design. R_{pub} = 415°C/W on minimum pad mounting on FR-4 board in still air.
Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

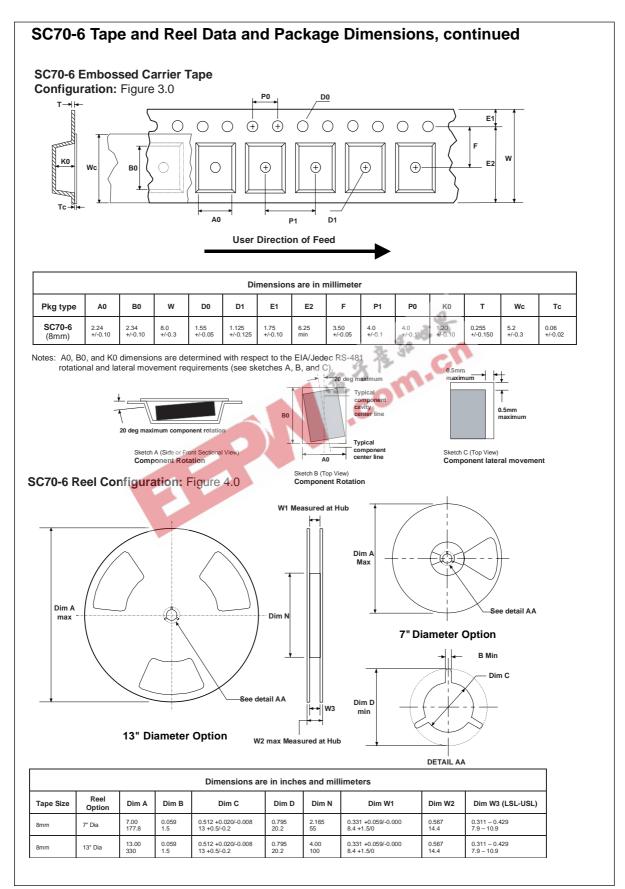


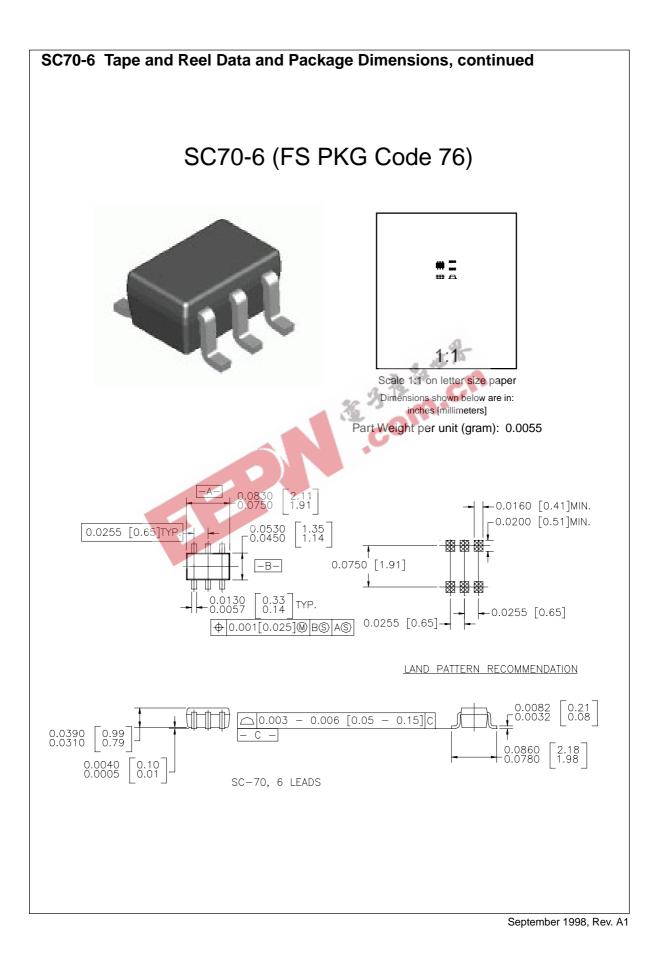


FDG6303N Rev.E1



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